N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.003 @ V_{GS} = 10 V	25
	0.004 @ V_{GS} = 4.5 V	22

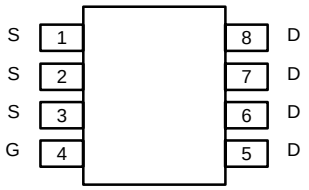
FEATURES

- TrenchFET® Gen II
- Ultra Low On-Resistance Using High Density TrenchFET Power MOSFET Technology

APPLICATIONS

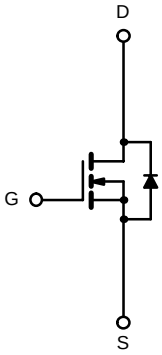
- Synchronous Buck Low-Side
  - Notebook
  - Server
  - Workstation
- Synchronous Rectifier-POL

SO-8



Top View

Ordering Information: Si4320DY
Si4320DY-T1 (with Tape and Reel)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	25	17	A
	T_A = 70°C		20	13	
Pulsed Drain Current (10 μs Pulse Width)		I_{DM}	70		
Continuous Source Current (Diode Conduction)[a]		I_S	2.9	1.3	
Avalanch Current		i_{AS}	50		
Maximum Power Dissipation[a]	T_A = 25°C	P_D	3.5	1.6	W
	T_A = 70°C		2.2	1	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	29	35	°C/W
	Steady State		67	80	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	13	16	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

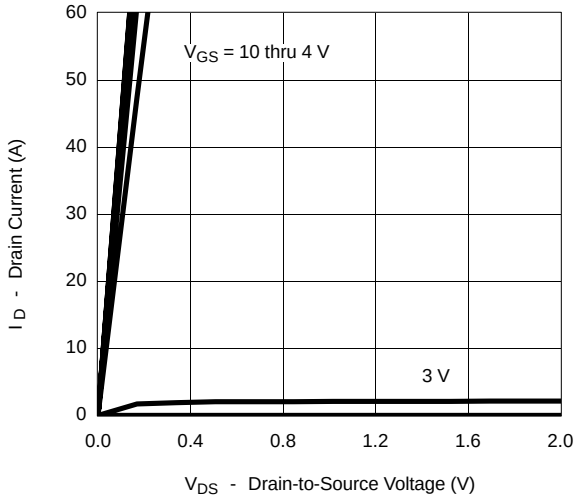
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.0		3.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 55°C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	30			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 25 A		0.0024	0.003	Ω
		V_{GS} = 4.5 V, I_D = 22 A		0.0032	0.004	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 25 A		110		S
Diode Forward Voltage[a]	V_{SD}	I_S = 2.9 A, V_{GS} = 0 V		0.72	1.1	V
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 20 A		6500		pF
Output Capacitance	C_{oss}			930		
Reverse Transfer Capacitance	C_{rss}			610		
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 20 A		45	70	nC
Gate-Source Charge	Q_{gs}	V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 20 A		20		nC
Gate-Drain Charge	Q_{gd}			16		
Gate Resistance	R_G	f = 1.0 MHz		1.1		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		27	40	ns
Rise Time	t_r			21	35	
Turn-Off Delay Time	$t_{d(off)}$			107	160	
Fall Time	t_f			43	65	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.9 A, di/dt = 100 A/μs		45	70	

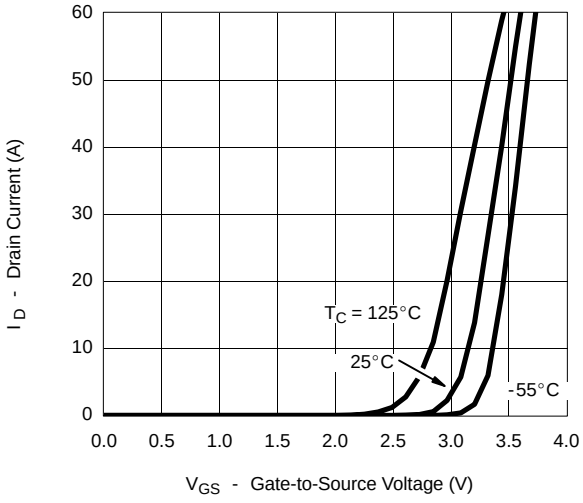
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics



Transfer Characteristics



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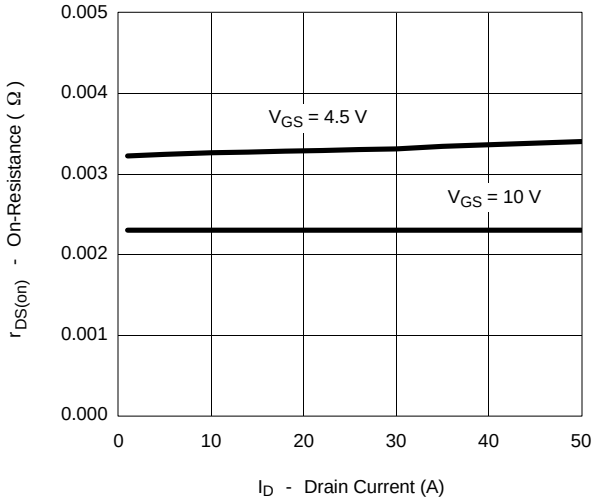
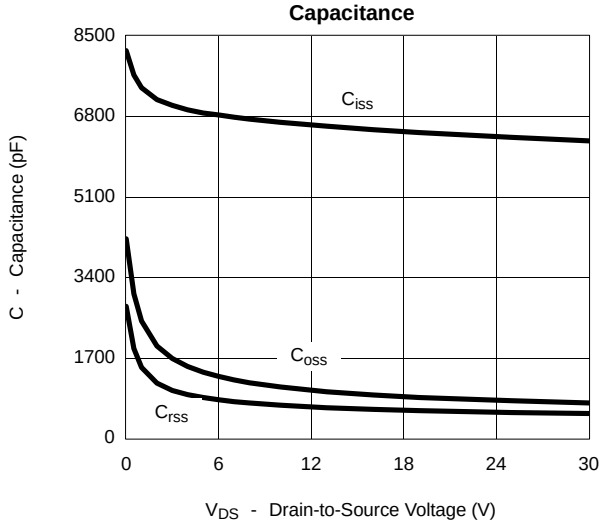
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

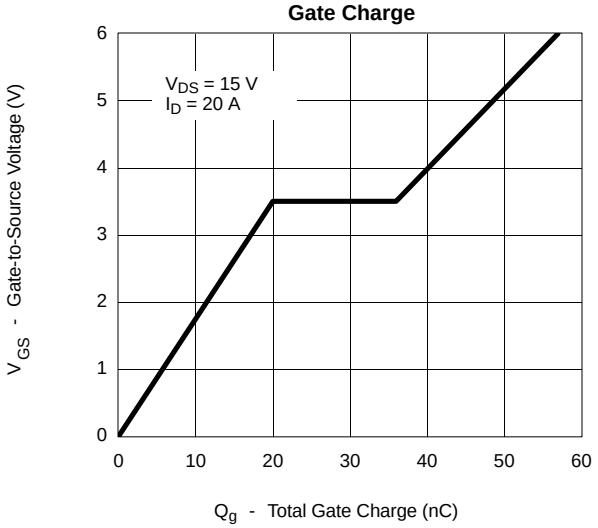
On-Resistance vs. Drain Current



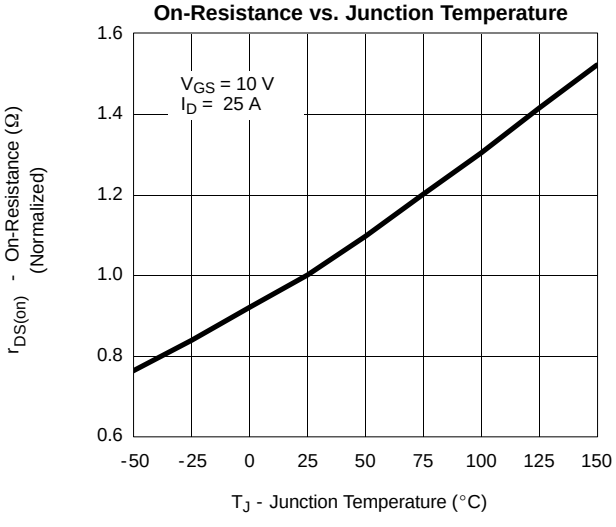
Capacitance



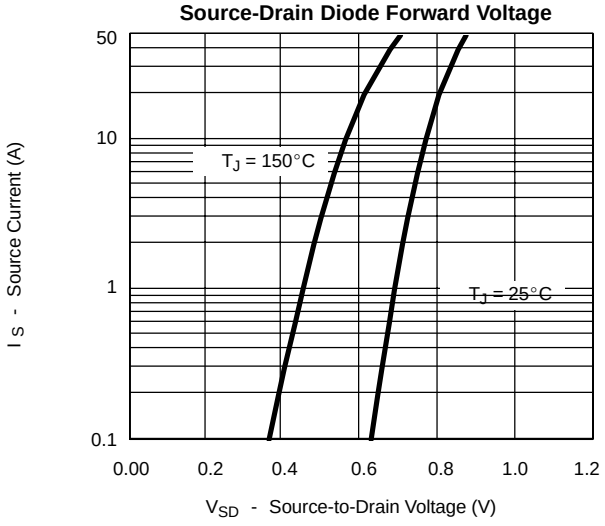
Gate Charge



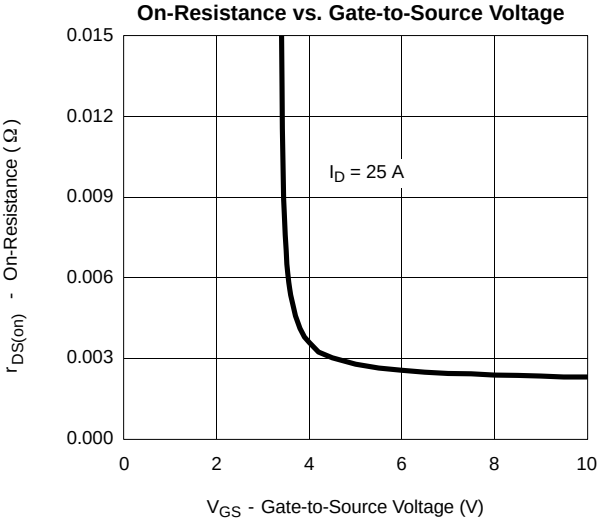
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



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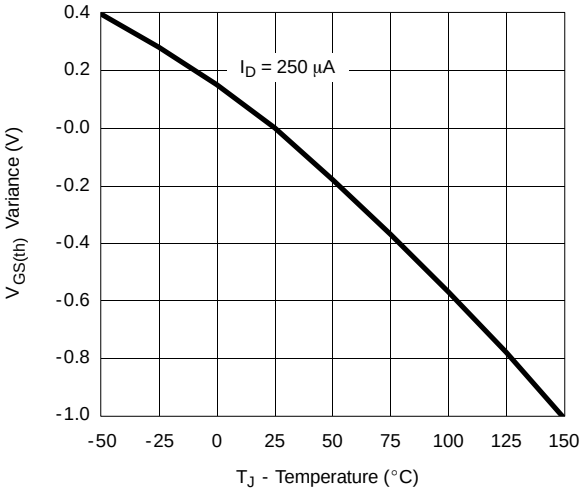
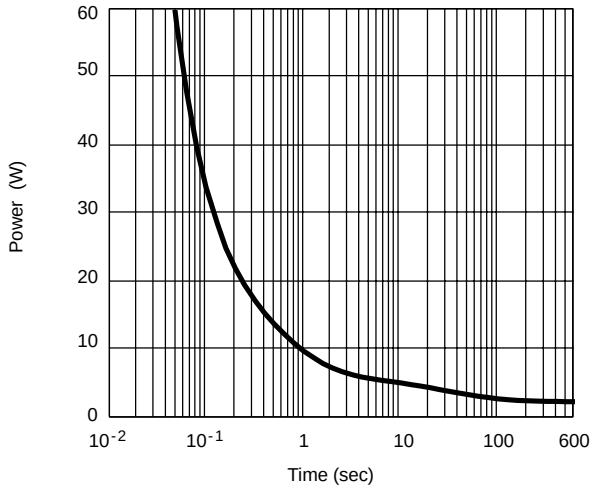
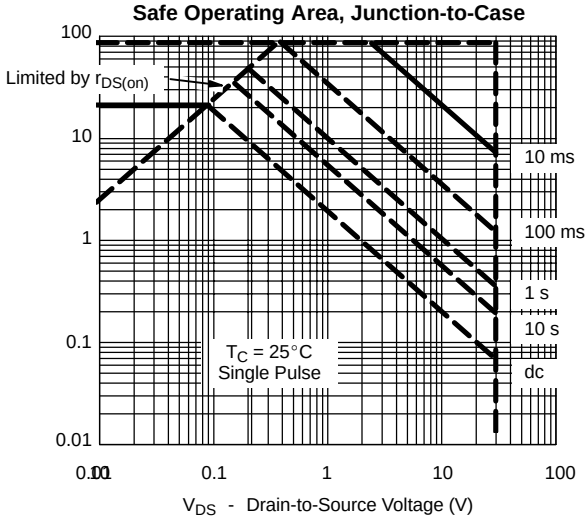
Threshold Voltage



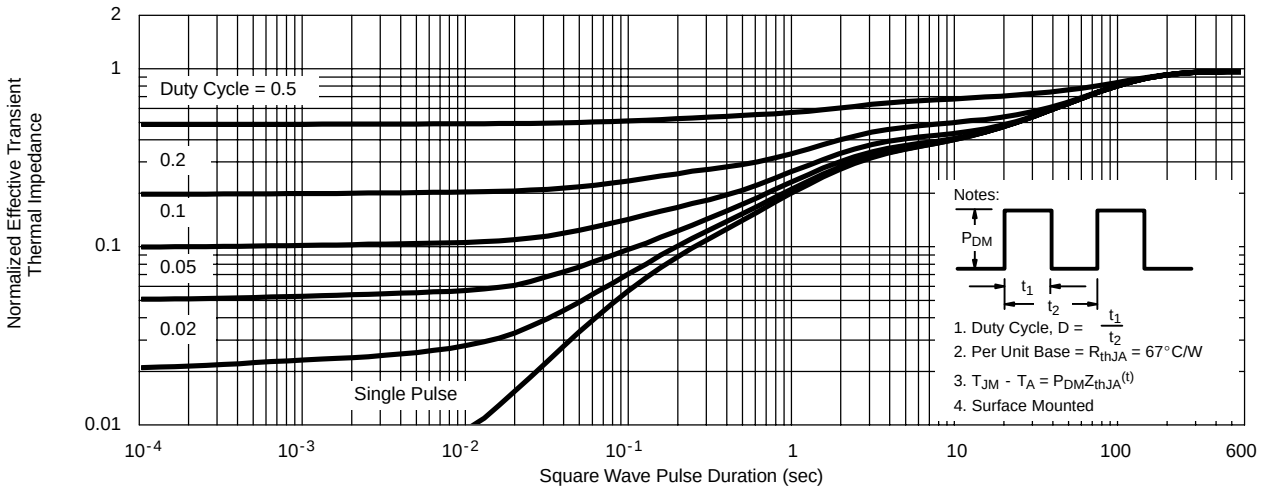
Single Pulse Power



Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)