MCM32257B

256K x 32 Bit Fast Static RAM Module

The MCM32257B is an 8M bit static random access memory module organized as 262,144 words of 32 bits. The module is a 64–lead zig–zag in–line package (ZIP) of eight MCM6229 fast static RAMs packaged in 28–lead SOJ packages and mounted on a printed circuit board along with eight decoupling capacitors.

The MCM6229 is a high–performance CMOS fast static RAM organized as 262,144 words of 4 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM32257B is equipped with output enable ($\overline{G}$) and four separate byte enable ($\overline{E1}$ – $\overline{E4}$) inputs, allowing for greater system flexibility. The $\overline{G}$ input, when high, will force the outputs to high impedance. $\overline{Ex}$ high will do the same for byte x.

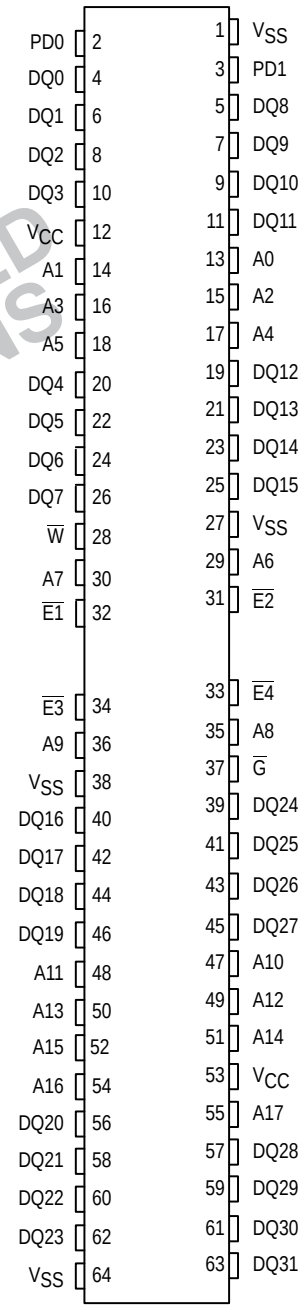
PD0 and PD1 are reserved for density identification. PD0 and PD1 are connected to ground. These pins can be used to identify the density of the memory module.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 15/20/25 ns
- Three–State Outputs
- Fully TTL Compatible
- JEDEC Standard Pinout
- Power Requirement: 960/880/840 mA Maximum, Active AC
- High Board Density ZIP Package
- Byte Operation: Four Separate Chip Enables, One for Each Byte (Eight Bits)
- High Quality Four–Layer FR4 PWB with Separate Internal Power and Ground Planes
- Incorporates Motorola's State–of–the–Art Fast Static RAMs

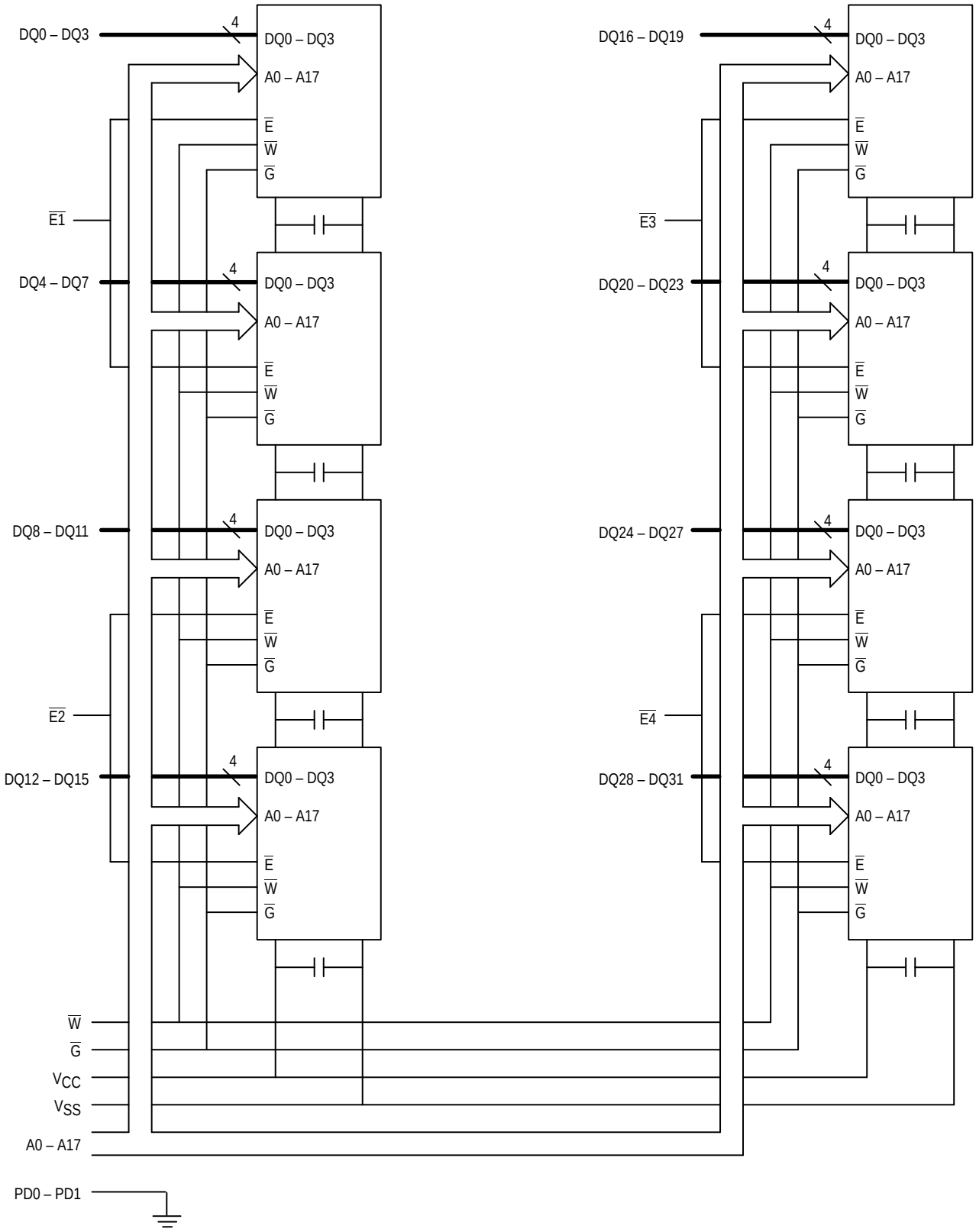
PIN NAMES	
A0 – A17	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$ – $\overline{E4}$	Byte Enables
DQ0 – DQ31	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
PD0 – PD1	Package Density

For proper operation of the device, V_{SS} must be connected to ground.

PIN ASSIGNMENT
TOP VIEW
64 LEAD ZIP — CASE 871–01



FUNCTIONAL BLOCK DIAGRAM
256K x 32 MEMORY MODULE



TRUTH TABLE

$\overline{Ex}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1} or I_{SB2}	High–Z	—
L	H	H	Read	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	8.8	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperatrue	T_{stg}	– 25 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	0.8	V

* V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)
** V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 8	µA
Output Leakage Current ($\overline{G}$, $\overline{Ex}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 8	µA
AC Active Supply Current ($\overline{G}$, $\overline{Ex}$ = V_{IL}, I_{out} = 0 mA, Cycle time ≥ t_{AVAV} min)	MCM32257B–15: t_{AVAV} = 15 ns MCM32257B–20: t_{AVAV} = 20 ns MCM32257B–25: t_{AVAV} = 25 ns	I_{CCA}	— — —	960 880 840	mA
AC Standby Current ($\overline{Ex}$ = V_{IH}, Cycle time ≥ t_{AVAV} min)		I_{SB1}	—	320	mA
CMOS Standby Current ($\overline{Ex}$ ≥ V_{CC} – 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)		I_{SB2}	—	40	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	(All pins except DQ0 – DQ31 and $\overline{E1}$ – $\overline{E4}$) ($\overline{E1}$ – $\overline{E4}$)	C_{in}	48 14	pF
Input/Output Capacitance	(DQ0 – DQ31)	C_{out}	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Output Timing Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V

Output Load . . . . . See Figure 1A Unless Otherwise Noted
Input Rise/Fall Time . . . . . 3 ns

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM32257B–15		MCM32257B–20		MCM32257B–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	3
Address Access Time	t_{AVQV}	—	15	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	—	15	—	20	—	25	ns	
Output Enable Access Time	t_{GLQV}	—	8	—	9	—	10	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	ns	4,5,6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	0	6	0	7	0	8	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	8	ns	4,5,6
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	15	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}). See Read Cycle 1.

AC TEST LOADS

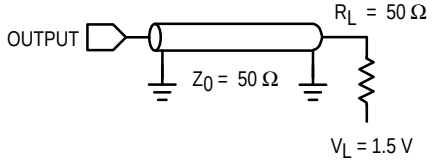


Figure 1A

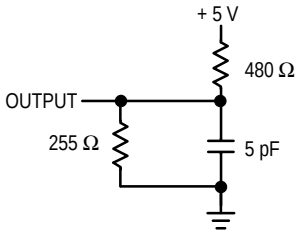
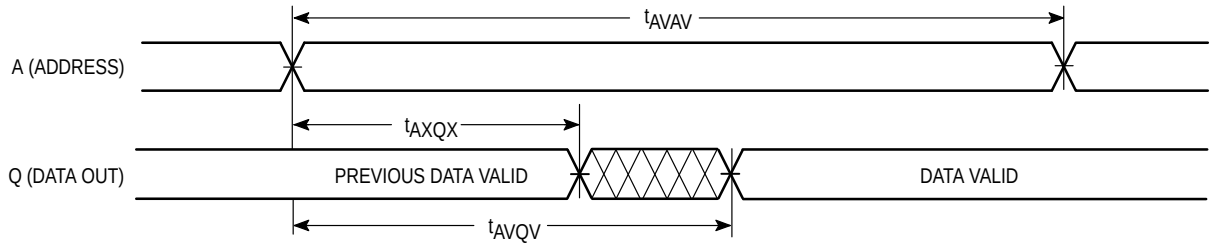


Figure 1B

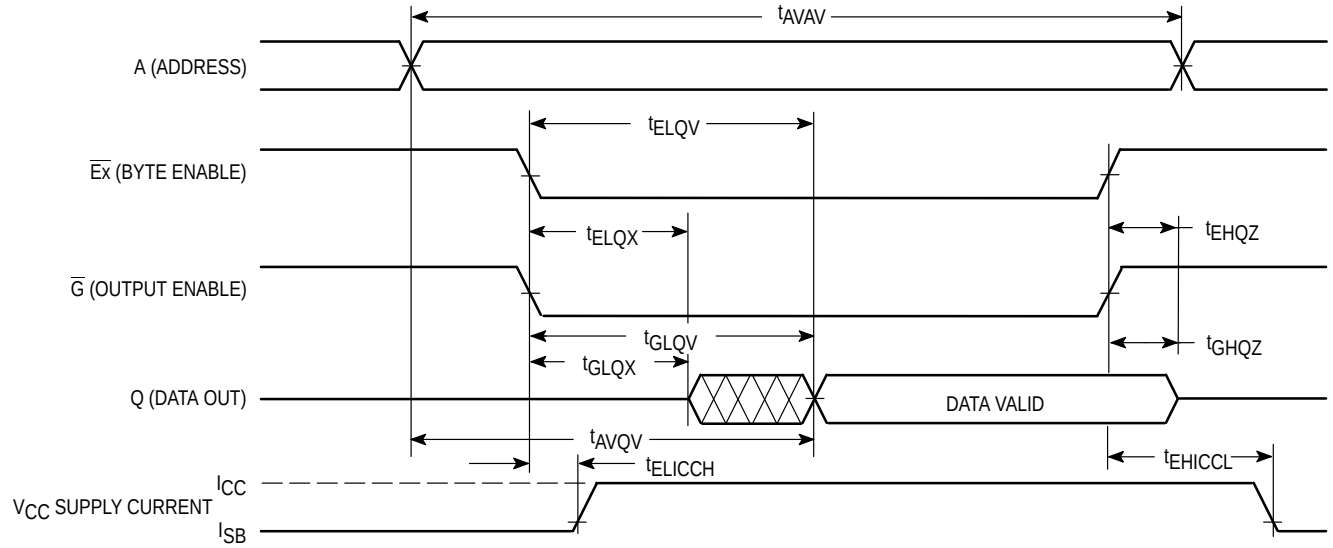
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7 Above)



READ CYCLE 2 (See Note)



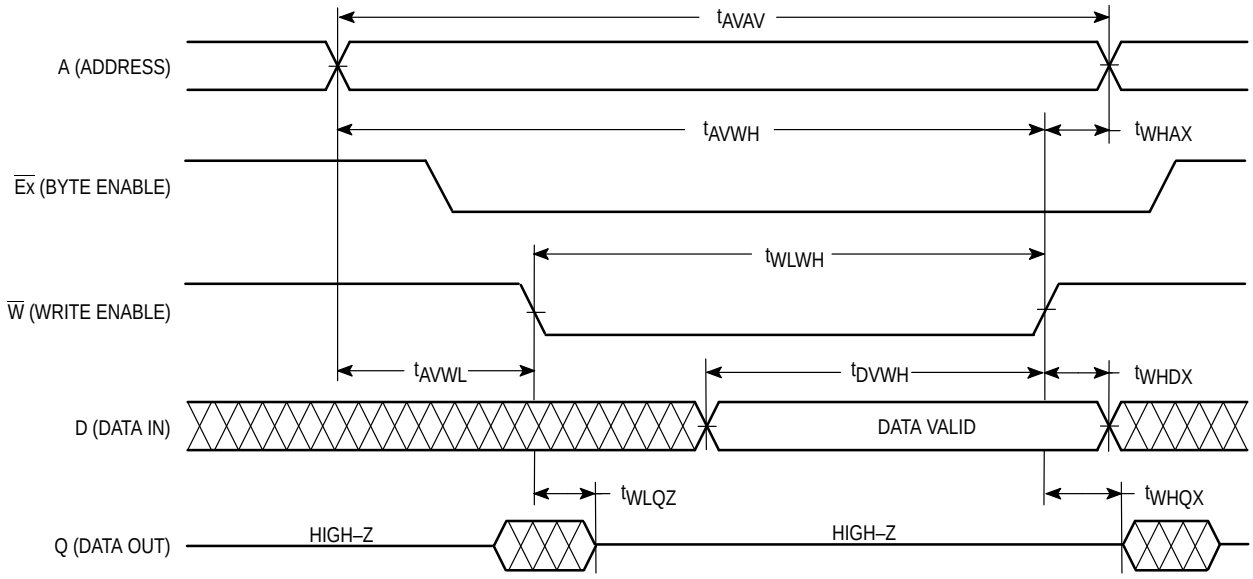
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM32257B–15		MCM32257B–20		MCM32257B–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	15	—	17	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	15	—	17	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	6	0	7	0	8	ns	4,5,6
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

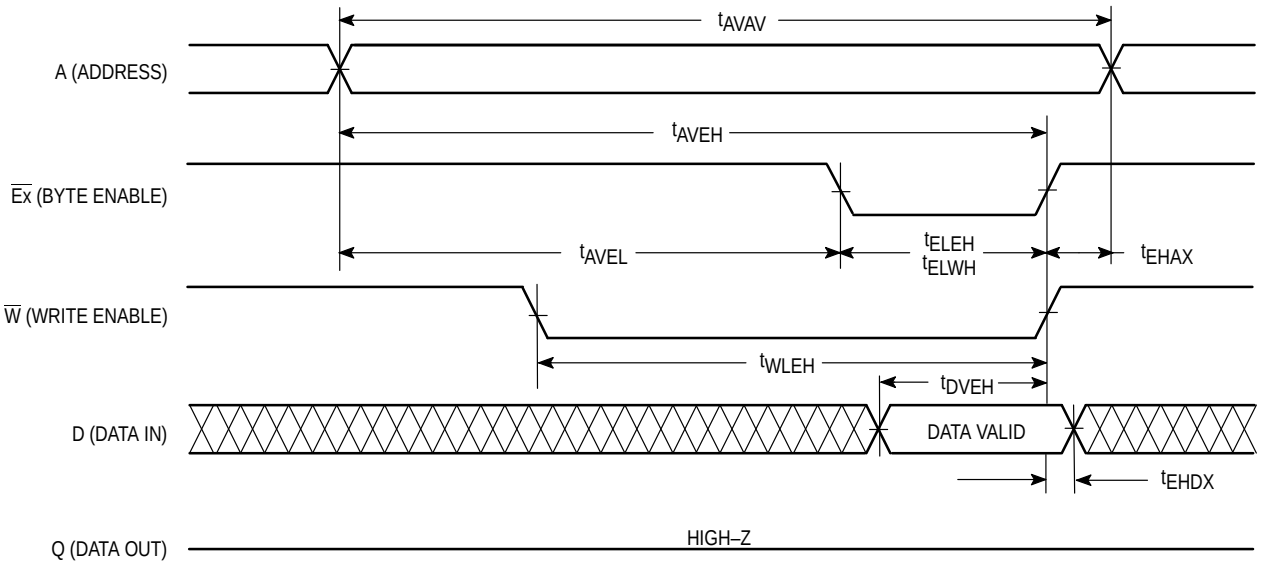


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

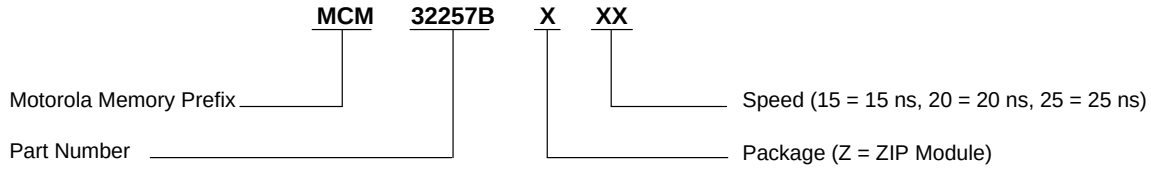
Parameter	Symbol	MCM32257B–15		MCM32257B–20		MCM32257B–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	15	—	17	—	ns	
Enable to End of Write	t_{ELEH}	10	—	12	—	15	—	ns	4,5
Enable to End of Write	t_{ELWH}	10	—	12	—	15	—	ns	
Write Pulse Width	t_{WLEH}	10	—	12	—	15	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	8	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



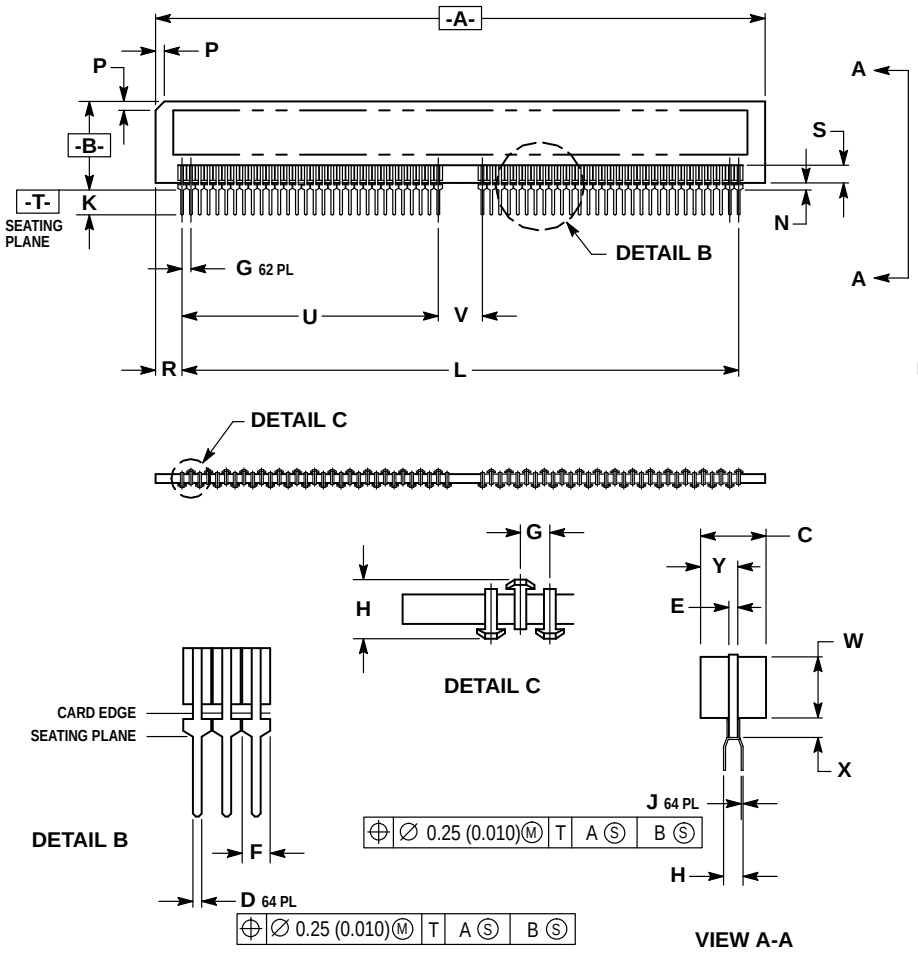
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM32257BZ15 MCM32257BZ20 MCM32257BZ25

PACKAGE DIMENSIONS

64 LEAD
ZIP PACKAGE
CASE 871–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	3.640	3.660	92.46	92.96
B	—	0.550	—	13.97
C	—	0.370	—	9.40
D	0.015	0.025	0.38	0.64
E	0.035	0.055	0.89	1.40
F	0.040	0.055	1.02	1.40
G	0.050 BSC		1.27 BSC	
H	0.100 BSC		2.54 BSC	
J	0.008	0.014	0.20	0.36
K	0.120	0.160	3.05	4.06
L	3.345	3.355	84.96	85.22
N	0.010	0.055	0.25	1.40
P	0.045	0.055	1.14	1.40
R	0.135	0.165	3.43	4.19
S	—	0.100	—	2.54
U	1.550 REF		39.37 REF	
V	0.250 REF		6.35 REF	
W	—	0.345	—	8.76
X	—	0.150	—	3.81

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