Integrated Circuit Systems, Inc.

Frequency Generator for High-Speed Applications

General Description

The **ICS9111-05/-06** is a high-speed clock generator designed to support high-speed workstations. The **ICS9111-05** generates a single copy of the 132.44 MHz from a 14.318 crystal. The **ICS9111-06** provides a second copy of the 132.44 MHz clock.

Features

- Generates one or two 132.44 MHz clocks from a 14.318 MHz crystal (-05 and -06, respectively)

- Less than 50ps one sigma jitter

- Less than ±150ps absolute jitter

- Rise/fall times less than 2.2ns driving 20pF

- On-chip loop filter components

- 3.0V - 5.5V supply range

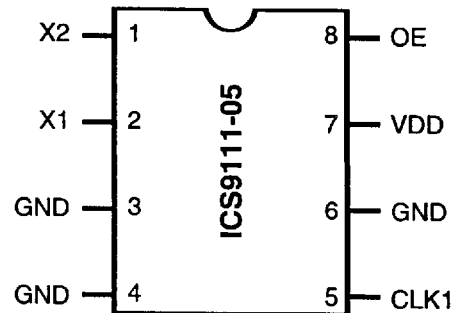- 8-pin, 150-mil SOIC package

Applications

- Specifically designed to support the high-speed clocking requirements of fiber channel systems
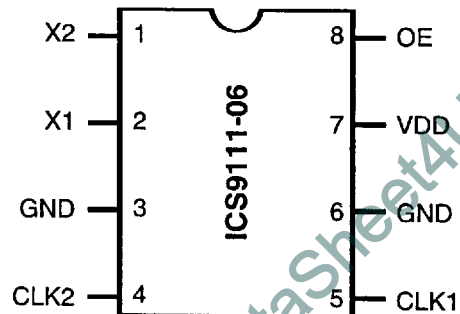
Block Diagram
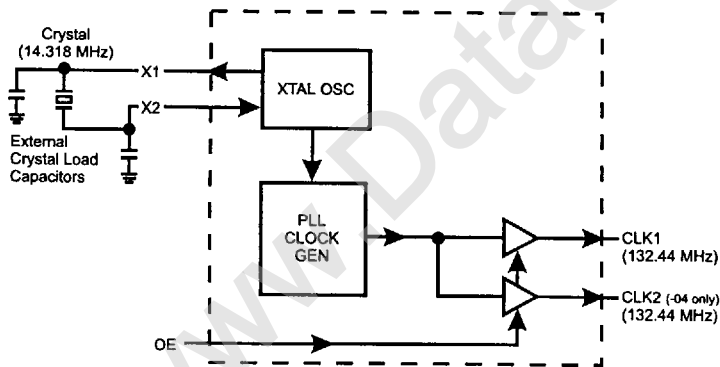
8-Pin SOIC

Functionality

X1, X2 (MHz)	OE	CLK (1:2)
14.318	1	132.44
14.318	0	Tristate

8-Pin SOIC

4825758 0002629 883

Pin Description ICS9111-05

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	X2	OUT	XTAL output, which includes XTAL load capacitors.
2	X1	OUT	XTAL or external reference frequency input. This input includes XTAL load capacitors and feedback bias.
3, 4, 6	Vss	PWR	Ground
5	CLK1	OUT	132.44MHz output when using 14.318 MHz XTAL
7	VDD	PWR	Power
8	OE	IN	Outut enable tristates all outputs when low. This input has an internal pull-up

Pin Description ICS9111-06

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	X2	OUT	XTAL output, which includes XTAL load capacitors.
2	X1	OUT	XTAL or external reference frequency input. This input includes XTAL load capacitors and feedback bias.
3, 6	Vss	PWR	Ground
4	CLK2	OUT	132.44MHz output when using 14.318MHz XTAL
5	CLK1	OUT	132.44MHz output when using 14.318MHz XTAL
7	VDD	PWR	Power
8	OE	IN	Output enable tristates all outputs when low. This input has an intenjal pull-up

Absolute Maximum Ratings

Supply Voltage ....7.0 V

Logic Inputs ....GND - 0.5 V to VDD + 0.5 V

Ambient Operating Temperature .... 0 to +70 C

Storage Temperature ....-65 to +150 C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stess specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3 V

V_{DD} = 3.0 - 3.7 V, T_A = 0 - 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.2V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	V_{IN} = 0 V	5	0.4	-	mA
Input High Current	I_{IH}	V_{IN} = V_{DD}	-2.0	-	2.0	mA
Output Low Current[1]	I_{OL}	V_{OL} = 0.8 V	30.0	47.0	-	mA
Output High Current[1]	I_{OH}	V_{OL}=2.0V	-	-66.0	-42.0	mA
Output Low Voltage[1]	V_{OL}	I_{OL}=15 mA	-	0.3	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=30 mA	2.4	2.8	-	V
Supply Current	I_{DD}	All outputs unloaded	-	22	50	mA

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

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Electrical Characteristics at 3.3 V

$V_{DD} = 3.0 - 3.7V, T_A = 0 - 70°C$ unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	T_{r1}	20pF load, 0.8 to 2.0V	-	0.8	1.6	ns
Fall Time[1]	T_{f1}	20pF load, 2.0 to 0.8V	-	0.6	1.3	ns
Rise Time[1]	T_{r2}	20pF load, 20% to 80%	-	1.4	2.2	ns
Fall Time[1]	T_{f2}	20pF load, 80% to 20%	-	1.0	1.6	ns
Duty Cycle[1]	D_{t1}	15pF load, 50% of V_{DD}	45	52	55	ps
Duty Cycle[1]	D_{t2}	15pF load @ $V_{OUT} = 1.4$ V	50	55	60	%
Jitter, One Sigma[1]	T_{j1s}	Load=15pF	-	18	50	ps
Jitter, Absolute[1]	T_{jab}	Load=15pF	-150	78	150	ps
Input Frequency[1]	F_j		50	14.318	16.0	MHz
Logic Input Capacitance[1]	C_{IN}	Logic input pin and X1, X2	-	5	-	pF
Power-on Time[1]	t_{on}	From V_{DD}=1.6V to 1st crossing of 132.44 MHz, V_{DD} supply ramp < 40 ms	-	0.185	1.0	ms
Frequency Settling Time[1]	t_s	From 1st crossing of acquisition to < 1% settling	-	49	500	μs

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 5.0 V

$V_{DD} = 4.5 - 5.5\ V, T_A = 0 - 70\ °C$ unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2.4	-	-	V
Input Low Current	I_{IL}	$V_{IN} = 0\ V$	-5	0.4	-	μA
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-2.0	-	2.0	μA
Output Low Current[1]	I_{OL}	$V_{OL} = 0.8\ V;$	36.0	62.0	-	mA
Output High Current[1]	I_{OH}	$V_{OL} = 2.0\ V;$	-	-152	-90.0	mA
Output Low Voltage[1]	V_{OL}	$I_{OL} = 20\ mA;$	-	0.25	0.4	V
Output High Voltage[1]	V_{OH}	$I_{OH} = -70\ mA;$	2.4	4.0	-	V
Supply Current[1]	I_{DD}	All outputs unloaded	-	47.0	70.0	mA

**Note 1:** Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 5.0 V

$V_{DD} = 4.5 - 5.5\,V, T_A = 0 - 70\,^{\circ}C$ unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	T_{r1}	20pF load, 0.8 to 2.0V	-	0.5	1.0	ns
Fall Time[1]	T_{f1}	20pF load, 2.0 to 0.8V	-	0.4	0.7	ns
Rise Time[1]	T_{r2}	20pF load, 20% to 80%	-	1.2	1.7	ns
Fall Time[1]	T_{f2}	20pF load, 80% to 20%	-	1.0	1.5	ns
Duty Cycle[1]	D_{t1}	15pF load @ $V_{OUT} = 50\%$ of V_{DD}	45	53	55	%
Duty Cycle[1]	D_{t2}	15pF load @ $V_{OUT} = 1.4\,V$	55	61	65	%
Jitter, One Sigma[1]	T_{jis1}	PCLK & BCLK Clocks; Load=20pF	-	15	30	ps
Jitter, Absolute[1]	T_{jab1}	PCLK & BCLK Clocks; Load=20pF	-150	77	150	ps
Input Frequency[1]	F_i		5.0	14.318	16.0	MHz
Logic Input Capacitance[1]	C_{IN}	Logic input pin and X1, X2	-	5	-	pF
Power-on Time[1]	t_{on}	From V=1.6V to 1st crossing of 132.44 MHz, V_{DD} supply ramp < 40 ms	-	0.2	1.0	ms
Frequency Settling Time[1]	t_s	From 1st crossing of acquisition to < 1% settling	-	59	500	µs

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.
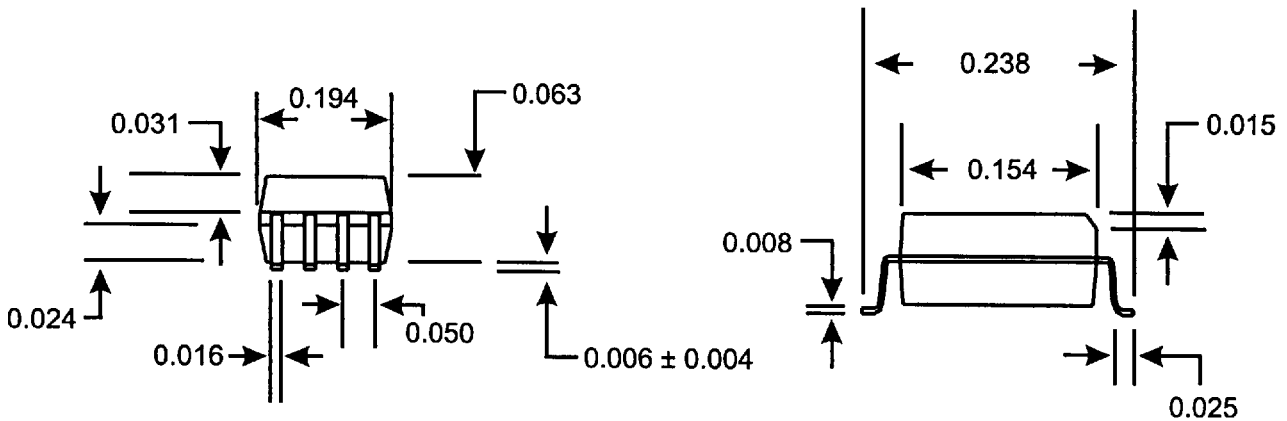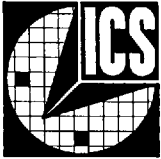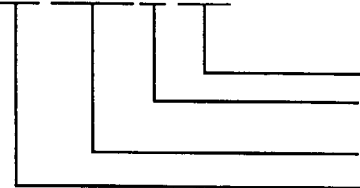
Ordering Information

ICS9111M-05, ICS9111M-06

Example:

ICS XXXX M-PPP

Pattern Number (2 or 3-digit number for parts with ROM code pattern)
Package Type
  M = SOIC
Device Type (consists of 3 or 4-digit numbers)
Prefix
  ICS, AV=Standard Device