Integrated Circuit Systems, Inc.

ICS9111-03/-04

Frequency Generator for Fibre Channel Systems

General Description

The **ICS9111-03/-04** is a high-speed clock generator designed to support fibre channel system requirements. The **ICS9111-03** generates a single copy of the 106.25 MHz from a 17 MHz crystal. The **ICS9111-04** provides a second copy of the 106.25 MHz clock.

An exact frequency multiplying ratio ensures better than ±100 ppm frequency accuracy using a standard AT crystal with external load capacitors (typically 33pF±5% for an 18pF load crystal). Achieving ±100 ppm over four years requires the crystal to have ±20 ppm initial accuracy, ±30 ppm temperature and ±5 ppm/year aging coefficients.

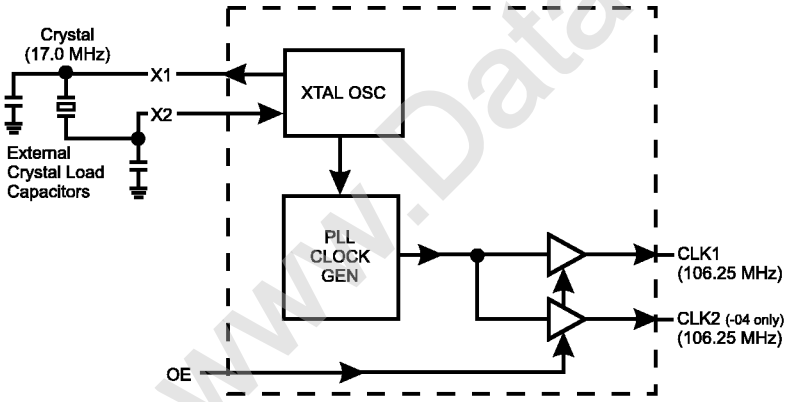
Features

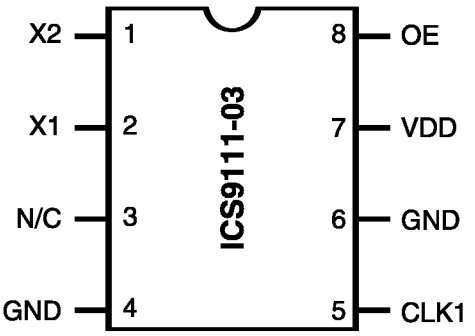
- Generates one or two 106.25 MHz clocks from a 17 MHz crystal (-03 and -04, respectively)
- Less than 65ps one sigma jitter
- Less than ±200ps absolute jitter
- Rise/fall times less than 2.2ns driving 20pF
- On-chip loop filter components
- 3.0V - 5.5V supply range
- 8-pin, 150-mil SOIC package

Applications

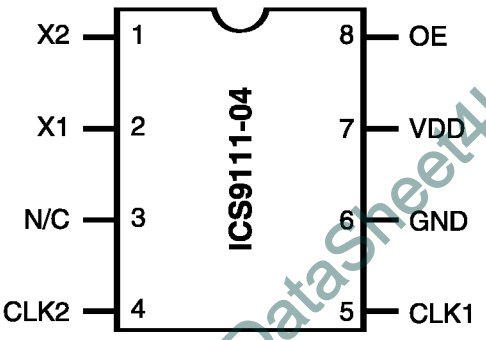
- Specifically designed to support the high-speed clocking requirements of fiber channel systems

Block Diagram





8-Pin SOIC



8-Pin SOIC

Functionality

X1, X2 (MHz)	OE	CLK (1:2)
17.0	1	106.25
17.0	0	Tristate

Pin Description ICS9111-03

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	X2	OUT	XTAL output, which includes XTAL load capacitors.
2	X1	OUT	XTAL or external reference frequency input. This input includes XTAL load capacitors and feedback bias.
3	N/C	-	Not connected
4,6	V_{SS}	PWR	Ground
5	CLK1	OUT	106.25MHz output when using 17MHz XTAL
7	V_{DD}	PWR	Power
8	OE	IN	Output enable tristates all outputs when low. This input has an internal pull-up

Pin Description ICS9111-04

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	X2	OUT	XTAL output, which includes XTAL load capacitors.
2	X1	OUT	XTAL or external reference frequency input. This input includes XTAL load capacitors and feedback bias.
3	N/C	-	Not connected
4	CLK2	OUT	106.25MHz output when using 17MHz XTAL
5	CLK1	OUT	106.25MHz output when using 17MHz XTAL
6	V_{SS}	PWR	Ground
7	V_{DD}	PWR	Power
8	OE	IN	Output enable tristates all outputs when low. This input has an internal pull-up

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V
Logic Inputs ..... GND - 0.5 V to VDD + 0.5 V
Ambient Operating Temperature ..... 0 to +70 C
Storage Temperature ..... -65 to +150 C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stess specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3 V

V_{DD} = 3.0 - 3.7 V, T_A = 0 - 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.2V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	V_{IN} = 0 V	5	0.4	-	mA
Input High Current	I_{IH}	V_{IN} = V_{DD}	-2.0	-	2.0	mA
Output Low Current[1]	I_{OL}	V_{OL} = 0.8 V	30.0	47.0	-	mA
Output High Current[1]	I_{OH}	V_{OL}=2.0V	-	-66.0	-42.0	mA
Output Low Voltage[1]	V_{OL}	I_{OL}=15 mA	-	0.3	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=30 mA	2.4	2.8	-	V
Supply Current	I_{DD}	All outputs unloaded	-	25	33	mA

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3 V

V_{DD} = 3.0 - 3.7 V, T_A = 0 - 70°C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	T_{r1}	20pF load, 0.8 to 2.0V	-	0.9	1.6	ns
Fall Time[1]	T_{f1}	20pF load, 2.0 to 0.8V	-	0.7	1.3	ns
Rise Time[1]	T_{r2}	20pF load, 20% to 80%	-	1.6	2.2	ns
Fall Time[1]	T_{f2}	20pF load, 80% to 20%	-	1.2	1.6	ns
Duty Cycle[1]	D_{t1}	15pF load, 50% of V_{DD}	45	52	55	ps
Duty Cycle[1]	D_{t2}	15pF load @ V_{OUT} = 1.4 V	50	54	60	%
Jitter, One Sigma[1]	T_{j1s}	Load=15pF	-	24	50	ps
Jitter, Absolute[1]	T_{jab}	Load=15pF	-200	95	200	ps
Input Frequency[1]	F_j		10.0	17.0	20	MHz
Logic Input Capacitance[1]	C_{IN}	Logic input pin and X1, X2	-	5	-	pF
Power-on Time[1]	t_{on}	From V_{DD}=1.6V to 1st crossing of 106.25 MHz, V_{DD} supply ramp < 40 ms	-	0.325	1.0	ms
Frequency Settling Time[1]	t_s	From 1st crossing of acquisition to < 1% settling	-	10	500	µs

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 5.0 V

V_{DD} = 4.5 - 5.5 V, T_A = 0 - 70 °C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2.4	-	-	V
Input Low Current	I_{IL}	V_{IN} = 0 V	-5	0.4	-	mA
Input High Current	I_{IH}	V_{IN} = V_{DD}	-2.0	-	2.0	mA
Output Low Current[1]	I_{OL}	V_{OL} = 0.8 V;	36.0	62.0	-	mA
Output High Current[1]	I_{OH}	V_{OL} = 2.0 V;	-	-152	-90.0	mA
Output Low Voltage[1]	V_{OL}	I_{OL} = 20 mA;	-	0.25	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH} = -70 mA;	2.4	4.0	-	V
Supply Current[1]	I_{DD}	All outputs unloaded	-	43.0	70.0	mA

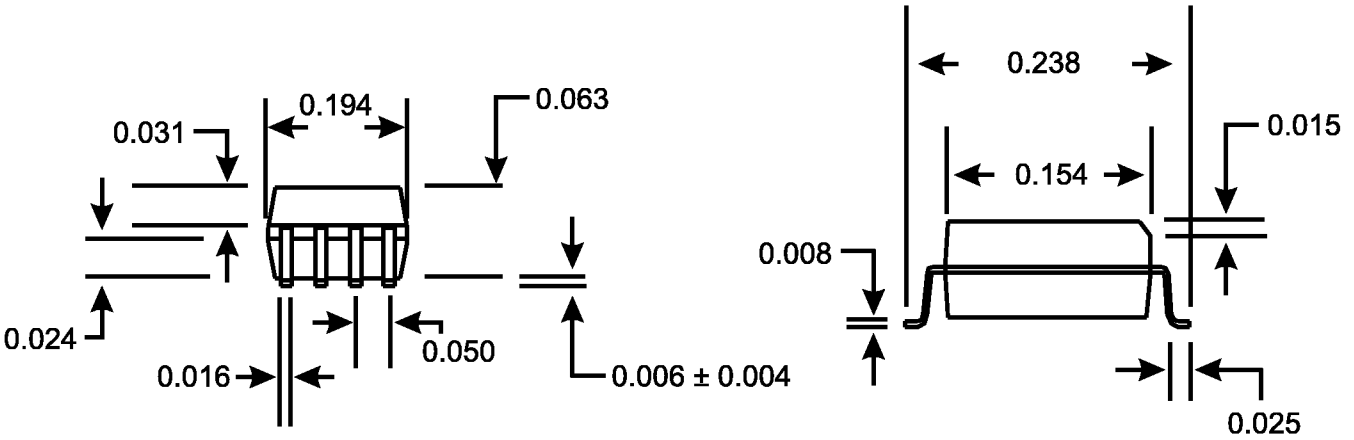
Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 5.0 V

V_{DD} = 4.5 - 5.5 V, T_A = 0 - 70 °C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	T_{r1}	20pF load, 0.8 to 2.0V	-	0.7	1.2	ns
Fall Time[1]	T_{f1}	20pF load, 2.0 to 0.8V	-	0.4	0.8	ns
Rise Time[1]	T_{r2}	20pF load, 20% to 80%	-	1.5	2.0	ns
Fall Time[1]	T_{f2}	20pF load, 80% to 20%	-	1.1	1.6	ns
Duty Cycle[1]	D_{t1}	15pF load @ V_{OUT} = 50% of V_{DD}	45	53	55	%
Duty Cycle[1]	D_{t2}	15pF load @ V_{OUT} = 1.4 V	50	59	65	%
Jitter, One Sigma[1]	T_{j1s}	PCLK & BCLK Clocks; Load=20pF	-	31	65	ps
Jitter, Absolute[1]	T_{jab}	PCLK & BCLK Clocks; Load=20pF	-200	110	200	ps
Input Frequency[1]	F_i		10.0	17.00	30	MHz
Logic Input Capacitance[1]	C_{IN}	Logic input pin and X1, X2	-	5	-	pF
Power-on Time[1]	t_{on}	From V=1.6V to 1st crossing of 106.25 MHz, V_{DD} supply ramp < 40 ms	-	.325	1.0	ms
Frequency Settling Time[1]	t_s	From 1st crossing of acquisition to < 1% settling	-	10	500	µs

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.



8-Pin SOIC Package

Ordering Information

ICS9111M-03, ICS9111M-04

Example:

ICS XXXX M-PPP

Pattern Number(2 or 3 digit number for parts with ROM code patterns)

M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS=Standard Device