AT1367A/B/C/D

Preliminary Product Information

1MHz, 800mA Synchronous Buck Converter With Power Good Detector & LDO

Features

- Operation Voltage 2.5V~6.0V
- Oscillation frequency 1MHz
- Output Current Maximum 800mA（DC-DC Converter）
- Built-In 400mA/LDO
- Power Good Indicator with Time Delay Adjustable
- Built-In Current Limit
- Built-In UVLO
- Built-In Thermal ShutDown
- Built-In LDO ON/OFF Control（Metal Option）

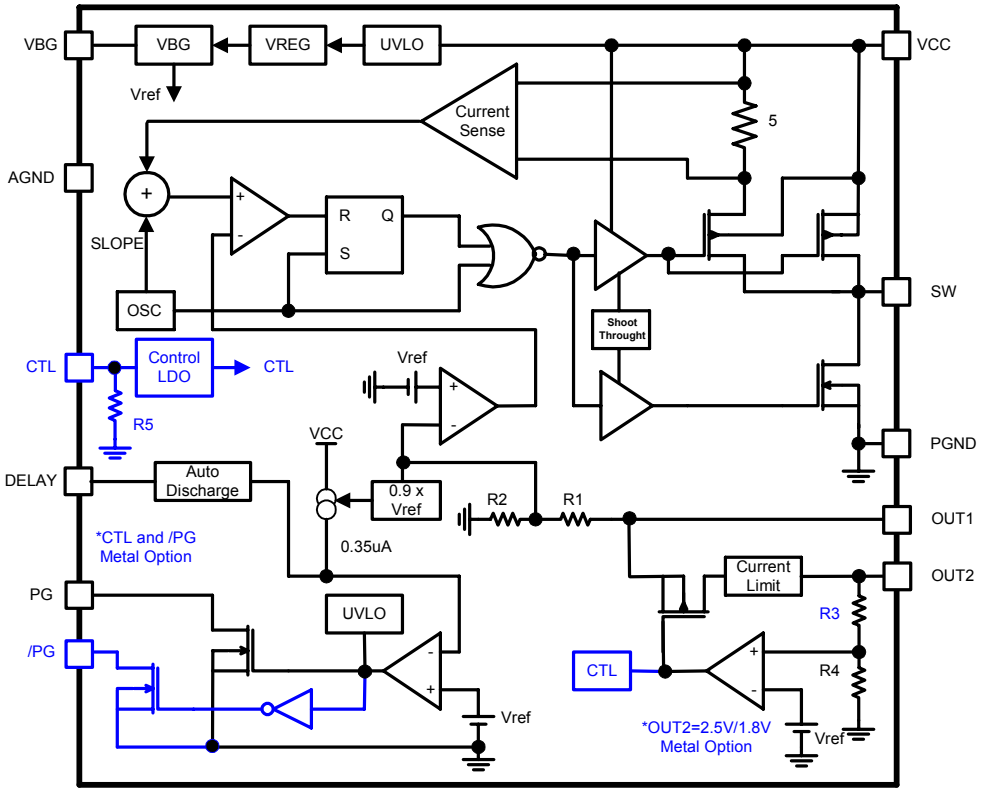
Applications

- Power Supply for Slim Type devices

General Description

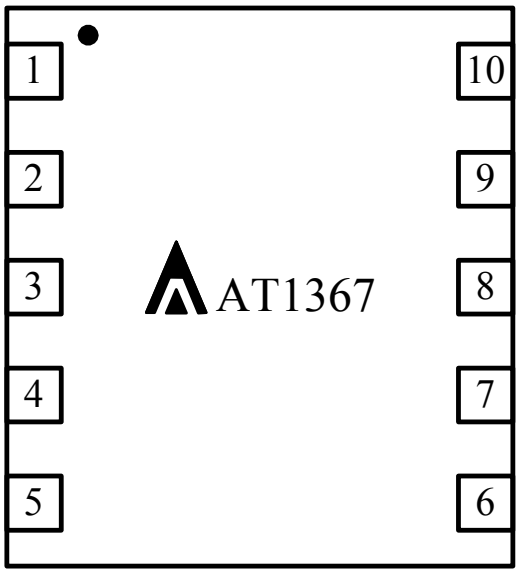
The AT1367A/B/C/D provides complete control for a DC/DC converter optimized for hight-performance microprocessor applications. It consists of a synchronous step-down DC/DC converter and a high-speed LDO regulator connected in series with the DC/DC converter output. A power good detector and LDO ON/OFF control is also built-in(metal option). DC/DC converter is operated on current mode architecture for excellent line and load transient response. 1MHz operation frequency is allowing the use of small surface mount inductor and capacitor. The internal synchronous switch increases efficiency and eliminates the need for an external schottky diode. The AT1367A/B/C/D is a family of low-noise synchronous step-down DC/DC converters that is ideally suited for systems powered form a 1-cell Li-ion battery or from a 3-cell to 4-cell NiCd, NiMH, or alkaline battery. It can also be used to USB-based power system.

Block Diagram



Aimtron reserves the right without notice to change this circuitry and specifications.

Pin Assignment



DFN10 (TOP VIEW)

AT1367A	AT1367B	AT1367C	AT1367D
/PG	/PG	CTL	CTL
LDO 2.5V	LDO 1.8V	LDO 2.5V	LDO 1.8V

Ordering Information

Part Number	Package	Marking
1367□N	DFN10,Green	□□□□□□

□： A:1367AN B:1367BN C:1367CN D:1367DN

□□□□□□： Date Code

**For more marking information, contact our sales representative directly.*

Pin Description

Symbol	Pin No.	Descript
PG	1	Power Good Indicator Output(Ative Hi)
/PG or CTL	2	/Power Good Output (Ative Lo) or LDO ON/OFF Control (Metal Option)
VCC	3	Power Supply
SW	4	OUT1 Inductor Node
PGND	5	Power Ground
VBG	6	Reference Output Voltage
AGND	7	Analog Ground
DELAY	8	The capacitor connection terminal for a reset delay time setup
OUT1	9	LDO Intput and DC/DC Output
OUT2	10	LDO Output

Absolute Maximum Ratings*1

Parameter	Symbol	Rated Value		Unit
		Min.	Max.	
Power Supply Voltage	VCC	-0.3	+6.5	V
Input Pin Voltage	CTL, OUT1, OUT2	-0.3	VCC	V
	SW, PG, /PG	-0.3	VCC+0.3	V
P-Channel Switch Source Current (DC)	—	-	1	A
N-Channel Switch Sink Current (DC)	—	-	1	A
Peak SW Sink and Source Current	—	-	1.5	A
Thermal Resistance from Junction to Ambient θ_{JA}	DFN10	-	35.25	^{0}C/W
Thermal Resistance from Junction to Case θ_{JC}	DFN10	-	3	^{0}C/W
Operating temperature T_A	—	-35	+85	^{0}C
Storage temperature	—	-55	+150	^{0}C
ESD Susceptibility*2	HBM	-	2	KV
	MM	-	200	V

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Device are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.

Recommended Operating Conditions

(Ta=+25^{0}C)

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{IN}	2.5	--	6.0	V
Operating temperature*	T_{OP}	-20	+25	+85	°C
Operating junction temperature	T_J	-	-	+150	°C

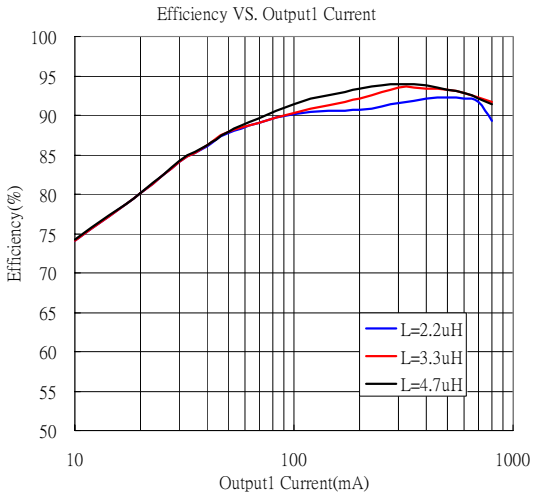
***Using X5R or X7R input capacitors.**

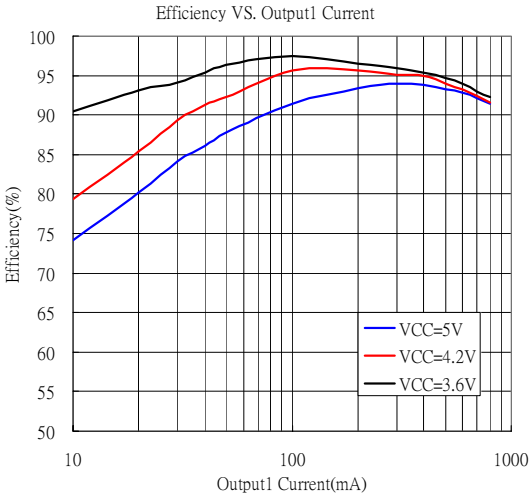
Electrical Characteristics

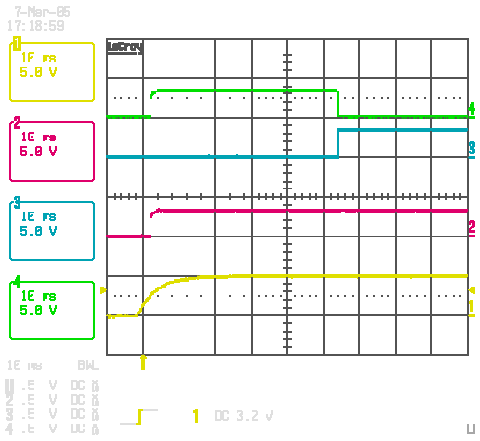
(VCC = 3.6V, T_a =+25℃ , unless otherwise noted.)

Parameter	Symbol	Condition	Values			Unit
			Min.	Typ.	Max.	
DC/DC CONVERTER						
VCC UVLO	V_{UV}	VCC=3V→2V Sweep	-	2.4	-	V
UVLO Hysteresis width	V_{UVHY}		-	100	-	mV
Input Supply Range	V_{CC}		2.5	-	6.0	V
Quiescent Current	I_S	Active Mode	-	500	-	μA
Output1 Voltage Accuracy	V_{OUT1}		-2	-	+2	%
Output1 Voltage line-regulation	$V_{OUT1\text{-}Line}$	VCC=3.5V to 6.0V	-	0.1	0.5	%
Output1 Variation with Temperature		T_a =-20℃ to +85℃	-	0.5	1.0	%
Feedback current	I_{OUT1}	V_{OUT1}=3.3V	-	6	-	uA
Current Limit	I_{CL1}	VIN=5V, V_{OUT1}=3.3V	1.10	1.25	1.50	A
Maximum Output Current	I_O	VIN=5V, V_{OUT1}=3.3V, L=4.7uH	-	-	800	mA
Oscillator Frequency	fosc1	Vout1=3.3V	0.8	1.0	1.2	MHz
	fosc2	Vout1=0V	-	200	--	KHz
$R_{DS(ON)}$ of P-Channel MOSFET	R_{PFET}	I_{LX}= 600mA	-	0.3	0.4	Ω
$R_{DS(ON)}$ of N-Channel MOSFET	R_{NFET}	I_{LX}= -600mA	-	0.25	0.35	Ω
SW Leakage Current	I_{SWL}		-	±0.1	±1	μA
CONTROL BLOCK						
CTL Threshold	V_{CTL}	V_{CTL}=0V~2V sweep（Metal Option）	0.3	1.0	1.5	V
CTL leakage Current	I_{CTL}	V_{CTL}=5.0V（Metal Option）	-	6	-	μA
PG on voltage	V_{PGON}	I_{PG}=1mA	-	-	0.4	V
PG Hysteresis width	V_{PGTHYS}		-	80	-	mV
PG pin leak current	I_{PGTLK}	$V_{/PG}$=5.0V	-	-	1	uA
/PG on voltage	$V_{/PGON}$	$I_{/PG}$=1mA（Metal Option）	-	-	0.4	V
/PG Hysteresis width	$V_{/PGTHYS}$	（Metal Option）	-	80	-	mV
/PG pin leak current	$I_{/PGTLK}$	$V_{/PG}$=5.0V（Metal Option）	-	-	1	uA
DELAY Pin Charge Current	I_{DELAY}		0.3	0.5	0.8	uA
LDO						
Output2 Voltage Accuracy	V_{OUT2}		-2	-	+2	%
Current Limit	I_{CL2}	V_{OUT1}=3.3V	450	-	-	mA
Dropout Voltage	V_{DV}	I_{OUT2}=400mA	-	400	600	mV
Load Regulation	ΔV_{OUT2}	I_{OUT2}=1mA→ 100mA	-	15	50	mV
Line Regulation	LR	I_{OUT2}=100mA, V_{OUT1}=3.5V→6.0V	-	0.05	0.25	%
Ripple Rejection Rate	PSRR	I_{OUT2}=100mA, f=1kHz	-	60	-	dB
OUT2 Leakage Current	I_{OUT2LK}	CTL=0V, V_{OUT2}=2.5V/1.8V（Metal Option）	-	6	-	uA

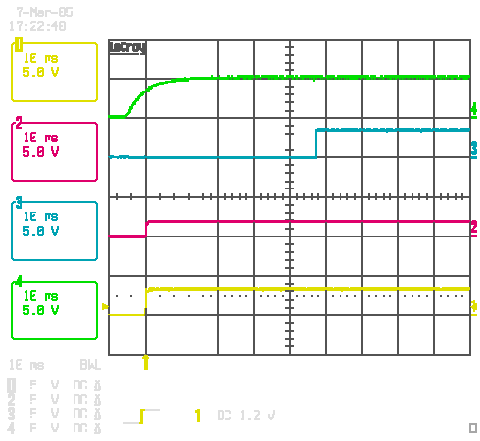
Typical characteristics



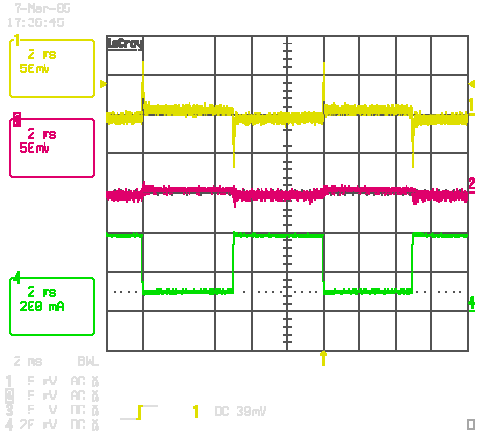




CH1：Vin, CH2：Vout1, CH3：PG, CH4：/PG

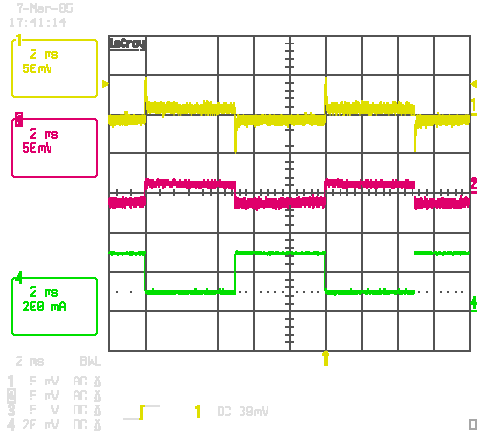


CH1：Vout1, CH2：Vout2, CH3：PG, CH4：CTL



CH1：Vout1, CH2：Vout2, CH4：Iout1

Iout1=100mA~400mA, Iout2=300mA



CH1：Vout1, CH2：Vout2, CH4：Iout2

Iout1=300mA, Iout2=100mA~300mA

Typical Application Circuits

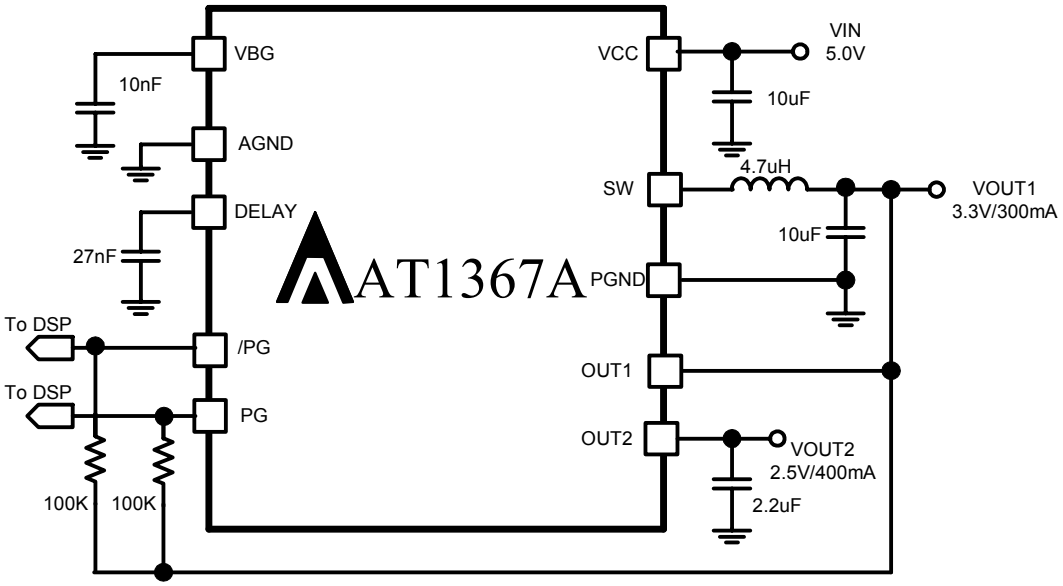


Figure 1

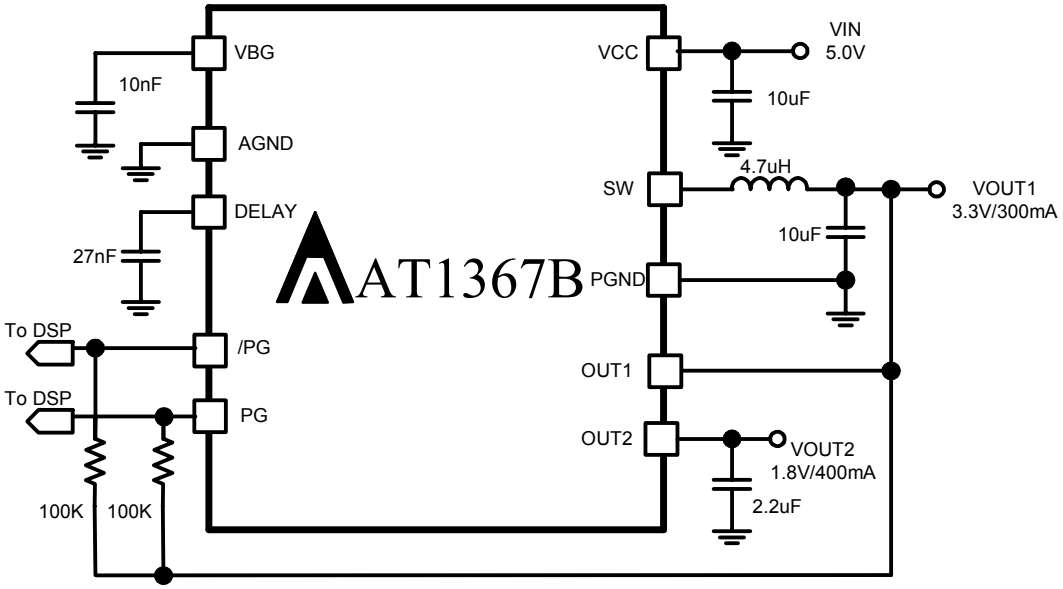


Figure 2

Typical Application Circuits (Continued)

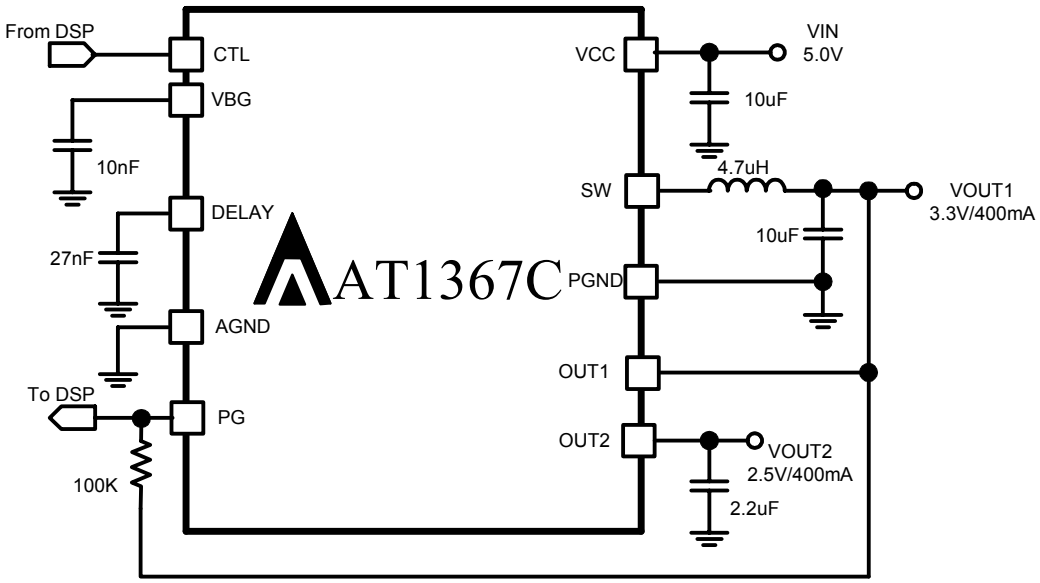


Figure 3

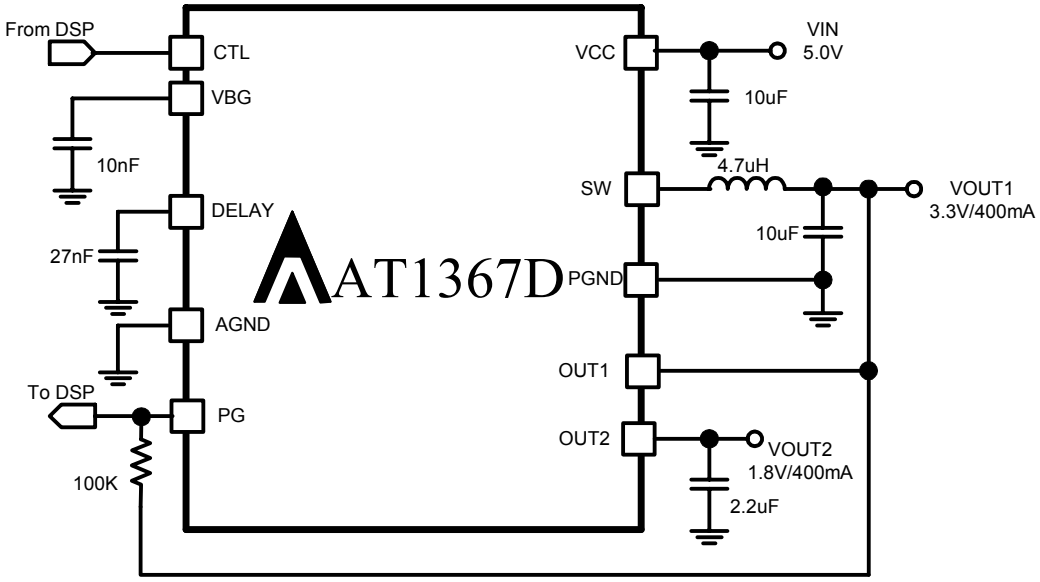


Figure 4

Typical Application Circuits (Continued)

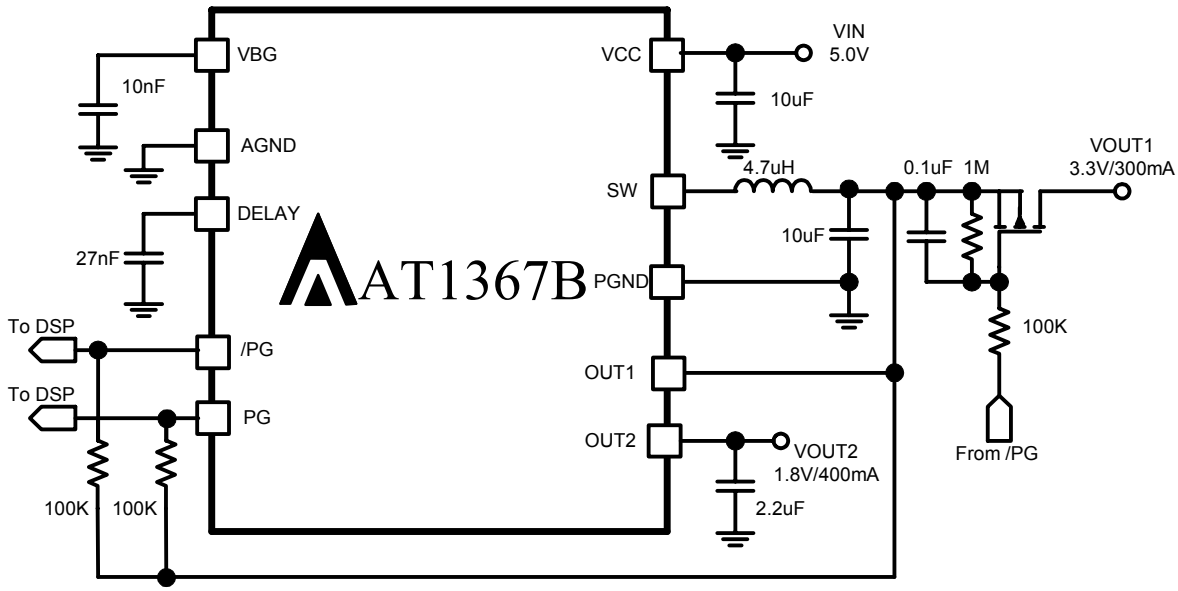


Figure 5

Application Information

Capacitor Selection

In continuous mode, the source current of the top MOSFET is square wave of duty cycle. The Primary function of the input capacitor is to provide a low impedance loop for the edges of pulsed current drawn by the AT1367A/B/C/D. A load step at the output can induce ringing at the input VIN. This ringing can couple to the output and be mistaken as loop instability. The oscillation can be improved by add the capacitance of the input capacitor. A typical value is 10μF ceramic (X5R or X7R), POSCAP or Aluminum Polymer. These capacitors will provide good high frequency bypassing and their low ESR will reduce resistive losses for higher efficiency. The input capacitor RMS current varies with the input voltage and the output voltage. The equation for the maximum RMS current in the input capacitor is:

$$I_{RMS} = I_{OMAX}\sqrt{\frac{V_O}{V_{IN}}(1-\frac{V_O}{V_{IN}})}$$

The output capacitor depends on the suitable ripple voltage. Low ripple voltage corresponds to lower effective series resistance (ESR). The output ripple voltage is determined by:

$$\Delta V_{OUT} \cong \Delta I_L (ESR + \frac{1}{8 f C_{OUT}})$$

The output capacitor RMS ripple current is given by:

$$I_{RMS} = \frac{1}{2\sqrt{3}} \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times f \times V_{IN}}$$

VBG Capacitor

A VBG pin is provided to decouple the bandgap reference voltage. An external capacitor connected form VBG to GND reduces noise present on the internal reference voltage, which in turn significantly reduces output noise and also improves PSRR. Larger capacitor values may be used to further improve PSRR, but result in a longer time period (slower turn on) to settle output voltage when power is initially applied.

LDO

For general purposes, use a 2.2uF capacitor on the LDO output. Larger capacitor values and lower ESR provide better supply noise rejection and transient response. A higher value input capacitor may be necessary if large, fast transients are anticipated . Ceramic capacitors have the lowest ESR, and will offer the best AC performance.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Inductor Selection

The inductor is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple current. Always consider the losses associated with the DCR and its effect on the total converter

efficiency when selecting an inductor. The inductor is selected to limit the ripple current to some predetermined value, typically 20~40% of the full load current at the maximum input voltage. The formula of inductance value is as below:

$$\Delta I_L = 0.2 \sim 0.4 \times I_{OUT(MAX)}$$

$$L = \frac{V_{OUT}}{f \times \Delta I_L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$I_{PK} = I_O + \frac{\Delta I_L}{2} = I_O + \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{2 \times L}$$

Power Good Indicator with Adjustable Time Delay

The PG and /PG pin terminal is an open drain output of N-MOS. Connect a resistor from PG and /PG pin to VCC or OUT1 to create a logic signal. If OUT1 pin is less than 2.97V (typ.) this pin is pulled to ground. When OUT1 pin is above 2.97V and with a delay time this pin is open. PG and /PG pin is forced low when in UVLO. The formula of adjustable delay time is as below :

$$delay - time = C \times \frac{0.8}{I_{DELAY}}$$

The Dissipation

The power loss is given by:

$$P_{LOSS(DC-DC)} = I_{OUT1}^2 \times R_{DS(ON)-P} \times D + I_{OUT1}^2 \times R_{DS(ON)-N} \times (1-D) + V_{IN} \times I_{OUT1} \times (t_r + t_f) \times f_s + I_s \times V_{IN}$$

$$P_{LOSS(LDO)} = I_{OUT2} \times (V_{OUT1} - V_{OUT2})$$

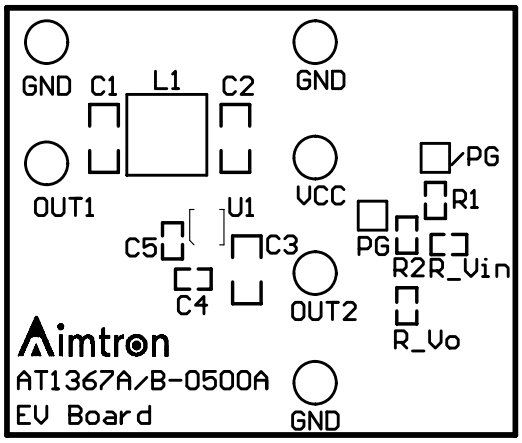
$$T_{J(MAX)} = T_A + \theta_{JA} \times (P_{LOSS(DC-DC)} + P_{LOSS(LDO)})$$

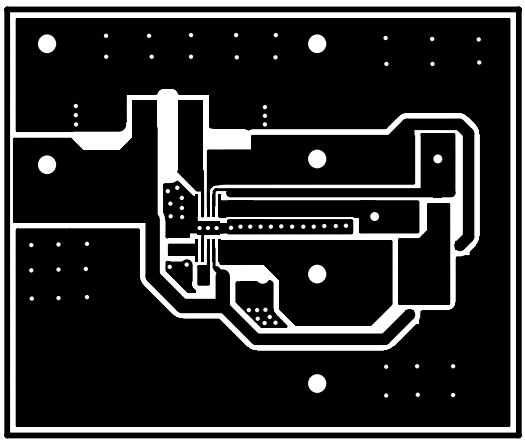
Inductors Surface Mount		
Inductance(μH)	Manufacturer/Part No.	Manufacturer Website
3.3	Sumida CDRH4D28-3R3	www.sumida.com
4.7	Sumida CDRH5D18-4R7	
3.3	Mitsumi C3-K1.8L-3R3 Mitsumi C4-K1.8L-3R3	www.mitsumi.co.jp
3.3	ABC SH40283R3YSB	www.atec-group.com
4.7	ABC SH40284R7YSB	

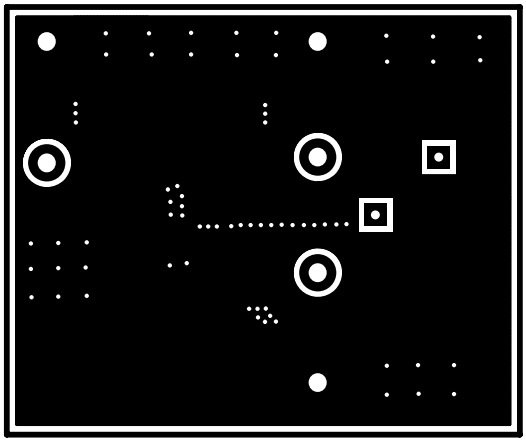
Capacitors Surface Mount		
Capacitance(μF)	Manufacturer/Part No.	Manufacturer Website
22	TDK C3216X5R0J226M	www.tdk.com
47	TDK C3225X5R0J46M	www.tdk.com
10	GRM42-6X5R 106K6.3	www.murata.com
2.2	TAIYO LMK212BJ225MD	www.t-yuden.com
4.7	TAIYO JMK212BJ475MG	www.t-yuden.com

PC Board Layout

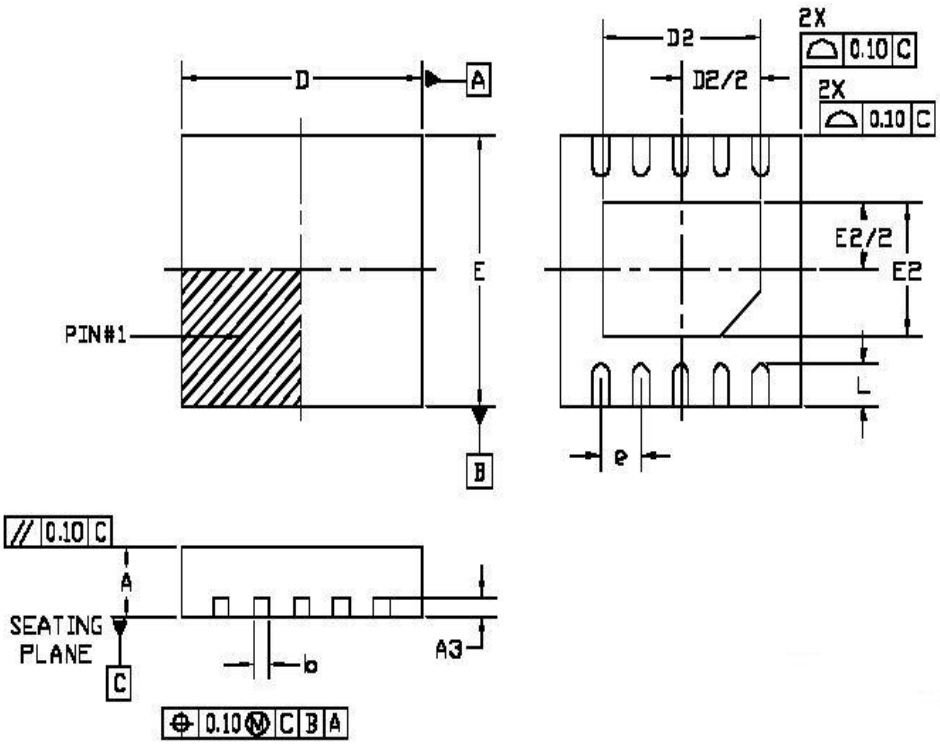
1. The most critical aspect of the layout is the placement of the input capacitor C2. It must be placed as close as possible to the AT1367A/B/C/D to reduce the input ripple voltage.
2. Power loops on the input and output of the converter should be laid out with the shortest and widest traces possible. The longer and narrower the trace, the higher resistance and inductance it will have. The length of traces in series with the capacitors increases its ESR and ESL and reduces their effectiveness at high frequency.
3. The OUT1 pin should connect to C1 directly. And the route should be away from the noise source, such as inductor of SW line.
4. Grounding all components at the same point may effectively reduce the occurrence of loop.







Package Outline : DFN10

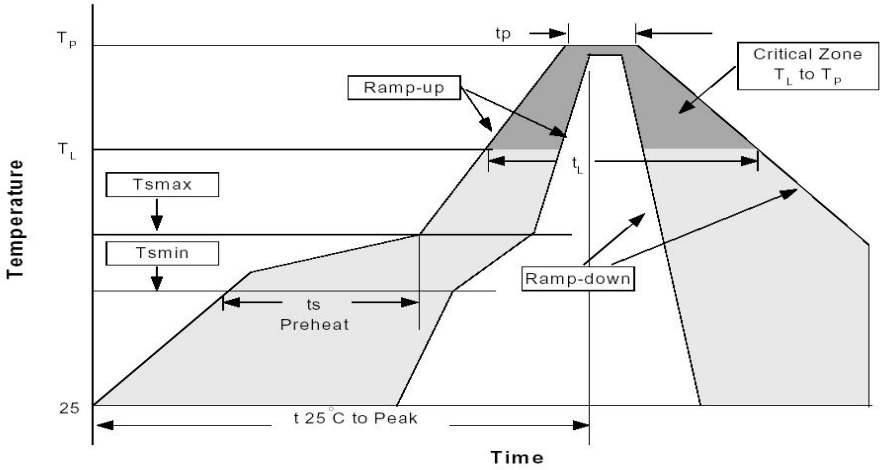


SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	SEE VARIATIONS					
A3	0.195	0.203	0.211	0.0077	0.0080	0.0083
b	0.18	0.25	0.30	0.007	0.010	0.012
D	2.95	3.0	3.05	0.116	0.118	0.120
E	2.95	3.0	3.05	0.116	0.118	0.120
e	0.50 BSC			0.020 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018

VARIATIONS "A"					
DIMENSIONS MILLIMETER			DIMENSIONS INCH		
MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
0.70	0.75	0.80	0.027	0.029	0.031

D2/E2			D2/E2		
DIMENSIONS MILLIMETER			DIMENSIONS INCH		
MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
2.30/1.55	2.35/1.60	2.40/1.65	0.090/0.061	0.092/0.063	0.094/0.065

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat -Temperature Min(Tsmin) -Temperature Max (Tsmax) -Time (min to max)(ts)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: -Temperature (T_L) -Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak/Classification Temperature(T_P)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (t_P)	10-30 seconds	10 seconds max.
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

***All temperatures refer to topside of the package, measured on the package body surface.**

Classification Reflow Profiles(Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3<350	Volume mm^3≥350
<2.5mm	240+0/-5℃	225+0/-5℃
≥2.5mm	225+0/-5℃	225+0/-5℃

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3<350	Volume mm^3 350-2000	Volume mm^3>2000
<1.6mm	260+0℃	260+0℃	260+0℃
1.6mm - 2.5mm	260+0℃	250+0℃	245+0℃
≥2.5mm	250+0℃	245+0℃	245+0℃

***Tolerance: The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0˚C. For example 260˚C+0˚C) at the rated MSL level.**