

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

NEC

The 2SK3901 is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super low On-state resistance $R_{DS(on)1} = 13 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 30 \text{ A})$
- $R_{DS(on)2}$ = 16.5 m Ω MAX. (VGS = 4.5 V, ID = 30 A)
- Low Ciss: Ciss = 1950 pF TYP.
- Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (VGS = 0 V)	VDSS	60	V
Gate to Source Voltage (VDs = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	D(DC)	±60	А
Drain Current (pulse) Note1	D(pulse)	±150	А
Total Power Dissipation (Tc = 25° C)	P _{T1}	64	W
Total Power Dissipation ($T_A = 25^{\circ}C$)	P _{T2}	1.5	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Energy Note2	Eas	68	mJ
Repetitive Avalanche Current Note3	IAR	26	А
Repetitive Avalanche Energy Note3	Ear	68	mJ

ORDERING INFORMATION

PART NUMBER	PACKAGE	
2SK3901-ZK	TO-263 (MP-25ZK)	





Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

- **2.** Starting T_{ch} = 25°C, V_{DD} = 30 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V, L = 100 μ H
- **3.** RG = 25 Ω , Tch(peak) \leq 150°C

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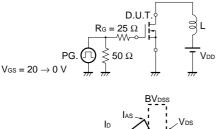
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 60 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	lgss	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 30 A	18	36		S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = 10 V, I _D = 30 A		10.3	13	mΩ
	RDS(on)2	V _{GS} = 4.5 V, I _D = 30 A		12.1	16.5	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V		1950		pF
Output Capacitance	Coss	V _{GS} = 0 V		380		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		150		pF
Turn-on Delay Time	td(on)	V _{DD} = 30 V, I _D = 30 A		12		ns
Rise Time	tr	V _{GS} = 10 V		6		ns
Turn-off Delay Time	td(off)	R _G = 0 Ω		48		ns
Fall Time	tr			5.0		ns
Total Gate Charge	QG	V _{DD} = 48 V		40		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		7.5		nC
Gate to Drain Charge	Qgd	I⊳ = 60 A		10.0		nC
Body Diode Forward Voltage Note	VF(S-D)	I⊧ = 60 A, V _{GS} = 0 V		0.96	1.5	V
Reverse Recovery Time	trr	IF = 60 A, VGS = 0 V		32		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ <i>µ</i> s		45		nC

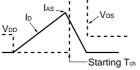
ELECTRICAL CHARACTERISTICS (TA = 25°C)

Note Pulsed

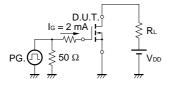
TEST CIRCUIT 1 AVALANCHE CAPABILITY

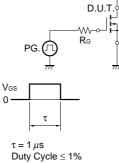
TEST CIRCUIT 2 SWITCHING TIME

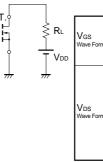


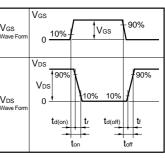


TEST CIRCUIT 3 GATE CHARGE

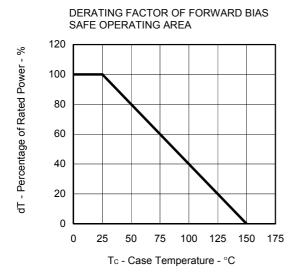


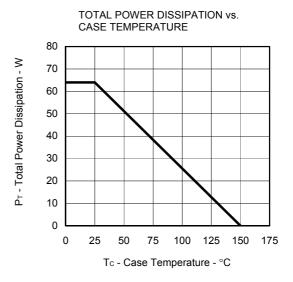




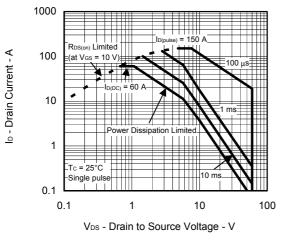


TYPICAL CHARACTERISTICS (TA = 25°C)

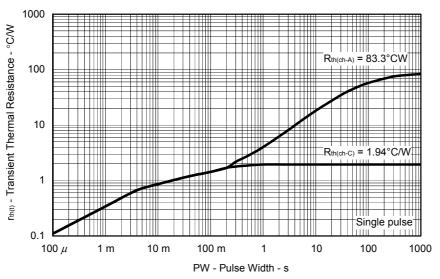




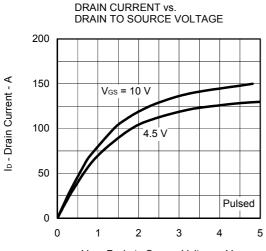
FORWARD BIAS SAFE OPERATING AREA





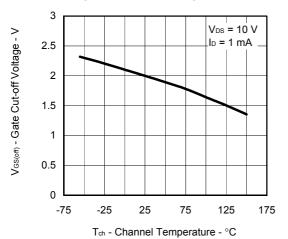


Data Sheet D17176EJ1V0DS



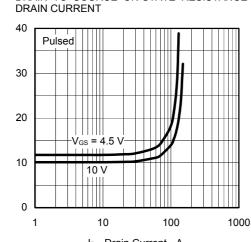




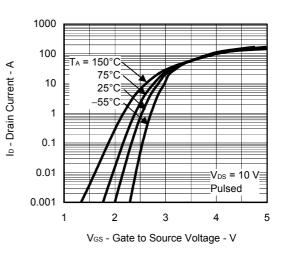


DRAIN TO SOURCE ON-STATE RESISTANCE vs.

 $R_{DS(on)}$ - Drain to Source On-state Resistance - m Ω

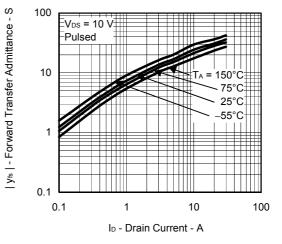


ID - Drain Current - A

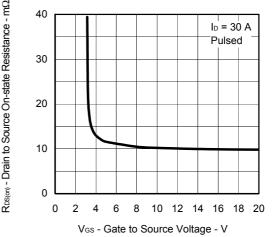


FORWARD TRANSFER CHARACTERISTICS

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

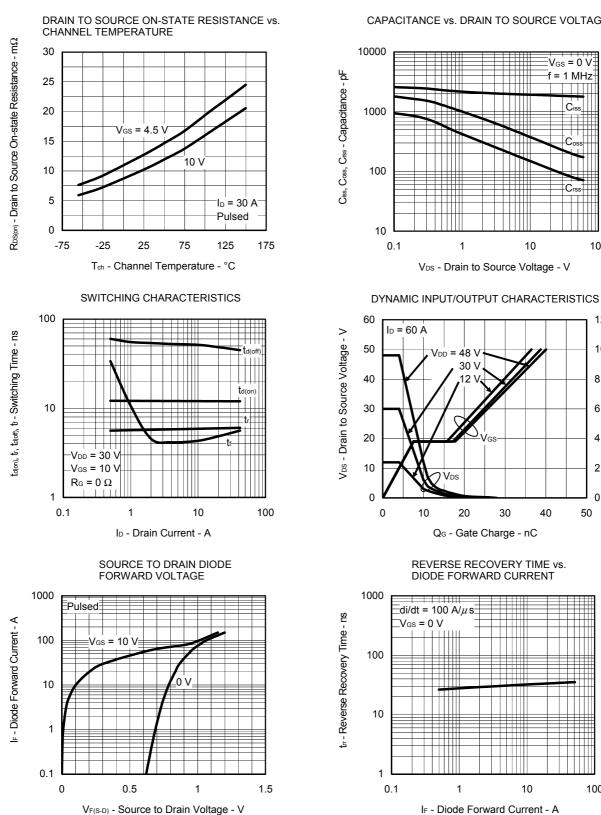


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

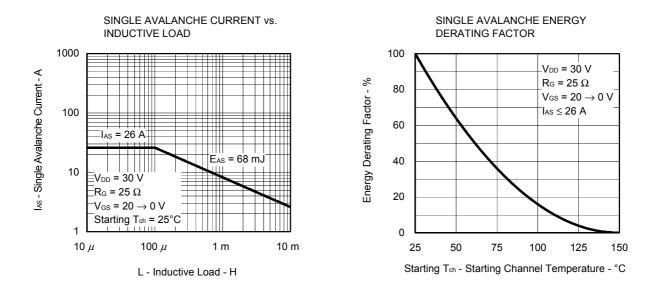


Ciss

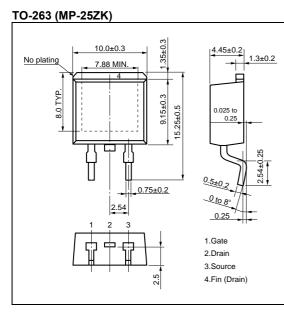
V_{GS} - Gate to Source Voltage - V



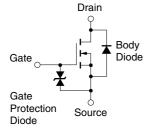
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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