T1Fx8 Device
8-Channel T1 Framer
TXC-03108

TECHNICAL OVERVIEW

FEATURES

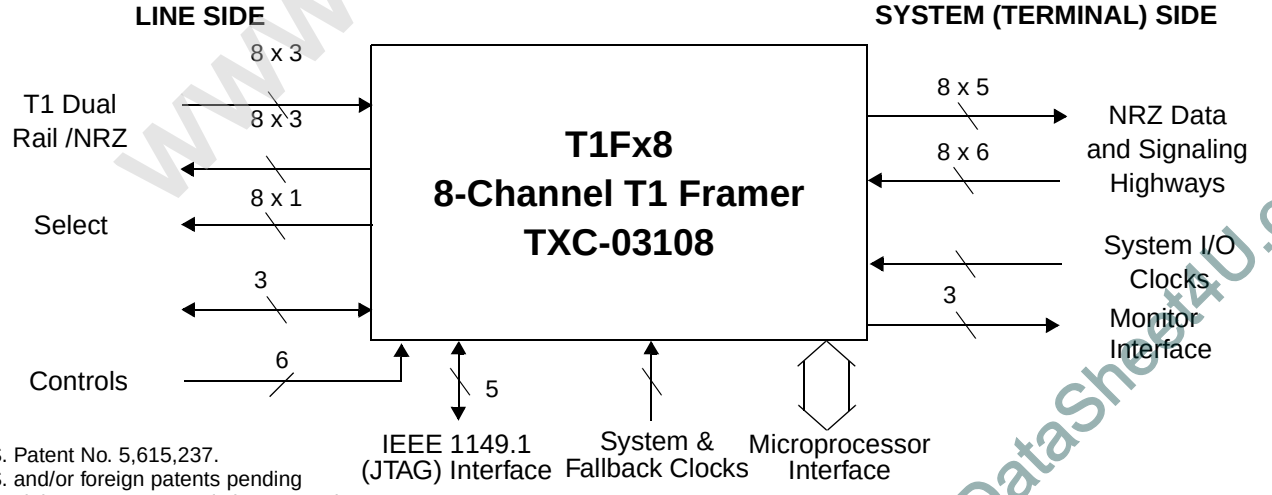
- D4 SF, ESF (including HDLC Link support), auto search, and independent transparent framing modes
- Encodes/decodes AMI/B8ZS and forced ones density line codes
- Fractional T1; Gapped clock or marker; Auxiliary input
- Monitor any DS1 for clock, data, and frame pulse
- Two-frame slip buffers in both receive and transmit directions with delay measurements
- Supports common channel and robbed-bit signaling (debounced or processor-forced on a per DS0 basis)
- Detects and forces RAI (Yellow) and AIS alarms; detects OOF, Severely Errored Frame, and Change of Frame Alignment; supports RAI-CI and AIS-CI
- Detects, counts and forces line code errors (BPVs and excess zeros), CRC errors, and frame bit errors
- Motorola/Intel-compatible microprocessor interface
- One-second interrupt input latches counter values and line events into shadow registers
- Local, line remote, payload remote and DS0 loopbacks with N x DS0 loopback code detection
- Automatic FDL Performance Report Message (PRM) Transmission; supports SPRM and NPRM
- Per framer PRBS/code word generator and analyzer for DS1 and N x DS0 testing
- Four system interface Modes: Transmission, Data, MVIP, H-MVIP/H.100
- Boundary scan capability (IEEE 1149.1)
- Single +3.3 V power supply; 5 V tolerant TTL inputs
- 208-lead or 256-lead plastic grid array package

DESCRIPTION

The T1Fx8 is an eight-channel DS1/J1 (1.544 Mbit/s) framer designed with extended features for voice and data communications applications. AMI, B8ZS, and forced ones density line codes are supported with full alarm detection and generation per ANSI T1.231. The transmit and receive sections of each of the eight framers are independent, with individual slip buffers to allow operation in a wide range of switching and transmission products. D4 SF and ESF modes are provided per ANSI T1.403.CORE-1998 draft and AT&T Pub. 62411, with per DS0 signaling and DS0 data access and control via a Motorola/Intel-compatible microprocessor. For ESF applications, each framer supplies a full duplex HDLC/bit-oriented message controller with dual 128-byte FIFOs in addition to on-board latching of all required performance parameters, which it can use to automatically generate one-second PRMs; minimal software overhead is required to support either ANSI T1.403-1998 or AT&T Pub. 54016 protocols. Diagnostic, test, and maintenance functions are provided, including DS1 and DS0 level loopback modes plus boundary scan (IEEE 1149.1).

APPLICATIONS

- SONET/SDH terminal or add/drop multiplexers supporting DS1 byte-synchronous operation
- DCS, digital central office or remote digital terminals
- Computer telephony integration equipment
- T1 and Fractional T1 CSUs
- ATM products with integrated DS1 interfaces
- LAN routers with integrated DS1 interfaces
- Multichannel DS1 test equipment
- Internet access equipment with fractional T1 interfaces



Document Number:
TXC-03108-MA
Ed. 2, May 2001

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LIST OF FIGURES

OVERVIEW

The T1Fx8 provides the features of two QT1F-*Plus* devices complemented by independent per time slot remote loopbacks, a gapped clock/marker system interface option, a per-channel PRBS/code word generator analyzer, a per-channel time slot inband loopback activate/deactivate detector/generator (compatible with the E1Fx8 and ANSI T1.231) and an internal selection option for the one-second clock. In addition, an intact mode for slip buffering unframed T1s, an auxiliary input for fractional T1 or ISDN D channel access, and independent transmit or receive framing bypass have been incorporated. The T1Fx8 supports the new ANSI T1.231 sectionalizer codes, AIS-CI and RAI-CI, for enhanced network diagnostics as well as being fully compliant to all alarm detection requirements of ANSI T1.231. Signaling debounce and a signaling change of state interrupt are incorporated along with certain alarms mapped to and from ESF ABCD codes to automatically support GR-253-CORE DS0 AIS and DS0 RAI alarm propagation. The HDLC FIFOs have been expanded to 128 bytes for each transmit and receive channel as well as being able to support back-to-back frames. The T1Fx8 supports an automatic generation of the ANSI T1.231 and T1.403 one-second PRM with microprocessor parameter modification capability. A delay value register was added to the slip buffers and mu-law digital milliwatt or a programmable idle code is available per time slot. The System Interface options are the same as those of the E1Fx8 with both separate signaling and data inversion capability. The T1Fx8 has the same lead configuration as the E1Fx8 in the same PBGA packages. Reduced power consumption is an added benefit of the T1Fx8, which is powered from a 3.3 volt supply, but is still tolerant of inputs from 5 volt parts.

The T1Fx8 supports multiple applications, including SONET/Async. networks and data applications where multiple framing functions are required in a single board. The T1Fx8 contains many features which allow it to be used in SONET Add/Drop multiplexers, T1 multiplexers, T1 and fractional T1 CSUs, PBXs, ATM products, LAN routers with integrated T1 interfaces, T1 Internet access equipment, Primary Rate ISDN interfaces, multichannel T1 test equipment, repeaters, access nodes and switches. In addition, the T1Fx8 includes many advanced diagnostic, test, and maintenance features, including boundary scan (IEEE 1149.1) and both T1 and time slot level loopbacks. The T1Fx8 is well suited for embedded CSU/DSU functions in routers and bridges and for test instruments needing a high degree of data manipulation.

The T1Fx8 supports both SF and ESF framing operating in an off-line mode with an automatic search feature. Either Common Channel Signaling (CCS, e.g., ISDN) or Channel Associated Signaling (robbed-bit) is supported. Per DS0 signaling enable/freeze or clear channel is supported. The transmit and receive sections of each of the eight framers are independent, with individual slip buffers and independent framed or unframed operation to allow use in a wide range of switching and transmission products.

Each framer supplies a full duplex HDLC message controller with onboard transmit and receive FIFOs, for ESF mode, in addition to onboard latching of all required performance parameters, requiring minimal software overhead and microprocessor bandwidth to support HDLC protocols. The HDLC controller is enhanced to include deep FIFOs (128 bytes each way) and a back-to-back capability where a single flag can separate frames.

The T1 digital line interface port is extremely flexible, allowing the device to connect to any industry standard line interface device with no external glue logic. AMI, B8ZS, and NRZ line codes are supported with full alarm detection and generation. Several forced ones density options are supported for the AMI line code. Optional frame pulse or drive bit output is available as well as fast sync input in the NRZ mode. The NRZ mode also allows the T1Fx8 to count externally detected code violations or to incorporate an external loss of clock/signal detector. The interface contains a serial port, which can directly control the external line interface unit and other components using the industry standard 'host' mode for device control.

The framer provides a microprocessor interface that is compatible with either Motorola or Intel processors. It is designed to act as an 8-bit peripheral using asynchronous bus transfers. Polling or interrupt support and latching of critical events are provided to accelerate interrupt processing and reduce the burden on the attached microprocessor. Individual alarm masks are available to ignore certain alarms or to operate different channels in different modes. Direct access to the slip buffers is provided for DS0 and the signaling RAMs, which makes sending special signaling or DS0 codes possible with low overhead. Scanning for signaling is facilitated with signaling debounce and interrupt on signaling change of state.

The framer supports a wide variety of individual and multiplexed system interface options to permit seamless interfacing to many types of DS0-based devices. Both MVIP and HMVIP/H.100 interfaces are provided for operation with many different system buses and devices. For maintenance support the T1Fx8 incorporates a per T1 PRBS code word generator/analyzer that provides 2^{15}-1 and QRSS (2^{20}-1) codes plus a programmable 32-bit code word. In addition, a per T1 time slot loopback activate and deactivate function compatible with the E1Fx8 and ANSI T1.231 Fractional T1 Loopback are provided. Error forcing and diagnostic access are also provided.

Although many advanced features are included, the device is optimized for the multichannel application. System I/O is minimized, and peripheral functions requiring significant logic or I/O have been reduced or eliminated. This device is well suited to systems requiring many T1 interfaces where real estate is at a premium and power consumption is important.

FEATURES

The 8-Channel T1 Framer (T1Fx8) device is a highly-featured eight-channel DS1 (T1) framer for use in a wide variety of interface, transmission and switching applications. Eight independent DS1 framers are provided in a single monolithic VLSI device using sub-micron CMOS technology. Powered from a single +3.3 volt supply, all eight framers dissipate less than one half watt typically. The T1Fx8 is provided in a 208-lead 17 mm by 17 mm small outline plastic ball grid array package or a 27 mm by 27 mm 256-lead plastic ball grid array package. Its ambient operating temperature range extends from -40°C to +85°C.

The T1Fx8 device has been designed to meet the latest industry standards (see sources list at rear), namely:

- ANSI T1.102-1993, T1.403.ROB-1998, T1.403.CORE-1998, T1.107- 1995 and T1.231-1997
- Bellcore GR-253-CORE (Issue 2), GR-303-CORE (Issue 1, Rev. 2) and GR-499-CORE (Issue 1)
- AT&T Pub. 62411 (Dec. 1990), Pub. 43801 and Pub. 54016
- IEEE 1149.1- 1990, 1149.1b - 1994
- ITU-T G.711 and O.151
- MVIP (Multi-Vendor Integration Protocol) and H-MVIP
- Enterprise Computer Telephony Forum, H.100 Revision 1
- TTC JT-704 (Japan)

The following features are independently selectable for each of the eight T1 (DS1) framers:

Framing Modes:

- D4 SF (Superframe Format)
  Programmable for both frame bits, Fs only, or Ft only (permitting basic framing for SLC-96, T1DM, etc.)
  Alternate RAI alarm (Japanese)
- ESF (Extended Superframe Format)
  FPS bits with or without a valid CRC-6 check to declare in frame.
  HDLC on-board controller
  4 kbit/s data link or 2 kbit/s data link using even or odd bits.
  Transmit fixed ZBTSI value
- Unframed (bypass) optional for either transmit, receive or both.
- Automatic option
  Framer searches alternatively for SF (Fs and Ft) or ESF (FPS and CRC-6)
  State of search available as status in both automatic and manual modes.
- Programmable Out of Frame control
  2 out of 4, 5, or 6 frame bits
- Alarm and signaling access for T1DM and other SF modes may be supported with external logic
- Microprocessor-forced reframe option

Line Interface Options:

- Rail option:
  B8ZS or AMI
  LOS detector
  16-bit BPV counters with excessive zeros option
- NRZ option:
  External BPV, fast sync or LOS (sense option) using RNEGn/RSCANn lead
  Drive lead using TNEGn/TDRVn lead or
  Transmit framing pulse option (3 ms, 1.5 ms, or 125 µs) using TNEGn/TDRVn lead
  Clock polarity selection for receive line clock input and transmit line clock output
  NRZ data inversion and clock edge options (separate transmit and receive control)

Signaling:

- Receive and transmit signaling buffers
- DS0 channel individual signaling freeze option with microprocessor rewrite capability in both receive and transmit directions for call control and trunk conditioning
- DS1 signaling freeze on LOS, OOF or AIS.
- Signaling debounce option; 2 superframes in a row must be equal in order to update
- Signaling change of state interrupt and activity register used with debounce feature.
- A, AB (SF)
- A, AB, ABCD (ESF)
- Byte-synchronous operation with TranSwitch DS1MX7

  Signaling bit positions in received DS0s optionally replaced by ones
  VT AIS and VT RFI to DS1 AIS and DS1 RAI (Yellow), respectively
  DS1 AIS and DS1 RAI (Yellow) to VT AIS and VT RFI, respectively
  DS0 AIS (ABCD transmit signaling robbed-bit code for all channels) on SONET alarms (ESF only)
  DS0 AIS (ABCD code to signaling highway for all channels) on DS1 AIS, LOF, LOS (ESF only)
  DS0 RAI (ABCD code to signaling highway for all channels) on DS1 RAI (Yellow) (ESF only)

Clock Management:

- Flexible receive and transmit clock selection, including local oscillator
- Two frame slip buffers for each of receive and transmit paths, with independent bypass
- System side and line side clocks on receive and transmit, each independent

Alarms and Errors:

- Detect and force RAI (Yellow) and AIS (Blue) alarms
- Detect Out Of Frame, Loss Of Signal, Severely Errored Frame, Change of Frame Alignment, transmit or receive slips and change of signaling state
- Detect, count and force CRC errors (ESF only), frame bit errors and line code errors (bipolar violations, with or without excessive zeros)
- Detect and force frame slips
- RAI-CI and AIS-CI support

Fractional T1:

- Programmable per DS0 receive gapped clock or marker output per framer
- 56 kbit/s switched data service or 64 kbit/s clear channel service
- Insert a 1 or signaling for 56 kbit/s service
- Programmable per DS0 transmit gapped clock or marker output per framer
- Fractional T1 data channel input that multiplexes data into frame

Slip Buffers and DS0 Control:

- Receive and transmit slip buffers
- Full frame (24 channels plus the framing bit) with bypass option
- Slip buffers work on a framed DS1 as well as an unframed T1 intact mode support
- Slip buffer features:
  24 DS0 channels
  Current delay (1.3 μs resolution) plus read and write pointer values
  Microprocessor recentering option
  DS1 freeze option
  DS0 channel individual freeze option with microprocessor write capability
  Framing bit freeze option with microprocessor rewrite capability

Storage when slip buffers are bypassed
Slip buffer status with common interrupt on any slip

- Per DS0 enable (independent receive and transmit) with microprocessor read and substitution in both receive and transmit directions to support maintenance codes and testing

Performance and Fault Monitoring

- One second basis via selected line clock or backplane clock
- Shadow registers for all alarms and counters
- Separate registers to indicate alarm changes and hard faults
- Facility Data Link HDLC controller
  Transmit from HDLC controller or system side (Transmission Mode only)
  128-Byte transmit and receive FIFOs per framer (new message size to support TSID, PID and IDLE)
  Back to back messages (supports NPRM)
  FIFO status bits
  Flag detection/generation, abort message detection/CRC-16
  Bit-oriented message generation and reception
- Automatic generation and transmission of FDL performance message:
  Optional
  Every second
  Gathers performance statistics from shadow registers

Maintenance:

- Loopbacks - line remote, local, payload remote (ESF only) and DS0 channel
- Detect and transmit SF loop-up and loop-down codes
- PBRS Generator in transmit framer and PRBS Analyzer in receive path per DS1 Channel
  2^{15}-1 (ITU-T O.151) or QRSS; unframed or framed DS1
  2^{15}-1, QRSS, or 32-bit code word per DS0 or N x DS0
  Separate control bits with software indication
- Transmit Digital Milliwatt Option per DS0 (ITU-T G.711)
- Transmit Idle (Microprocessor-written word) Option per DS0
- DS0 local Loopback transmission of Activate and Deactivate codes
- DS0 Remote Loopback (based on ANSI T1.403)
  With Interrupt Indication upon Completion of PRBS pattern and all ones
  With Interrupt Indication upon the reception of just the PRBS pattern to facilitate multiple fractions
  One fraction at a time
- Power-down modes force transmit leads to low, high or tristate

Microprocessor Interface:

- Eight-bit status register for LOS, AIS, OOF, YEL, CFA/AISCI, SEF, SLIP and change of signaling state
- Eight-bit latched event register and interrupt mask register for same conditions
- CRC (ESF only), code violation and frame bit error counters
- Shadow registers and counters
- Full control of framing, alarm generation and propagation, codec features
- HDLC link control, signaling access/control, DS0 access/control
- Reset, resync, slip buffer and frame bit access

The following features are only selectable for the eight framers as a group:

- Transmission/Data Modes (“off line” framing) or MVIP/H-MVIP/H.100 Modes as system interfaces
  1.544 Mbit/s Transmission:
    3 ms multiframe refresh rate
    Defined signaling highway format to carry signaling, AIS and RAI
    Receive system frame and clock out when slip buffers bypassed
    Receive system frame and clock in when slip buffers enabled
  1.544 Mbit/s Data
    125 µs refresh rate
    ABCD signaling nibble per DS0 channel on signaling highway
    Receive system frame and clock out when slip buffers bypassed
    Receive system frame and clock in when slip buffers enabled
  2.048 Mbit/s MVIP
    125 µs refresh rate
    32 time slots
    Slip buffers enabled (receive system clock and frame are inputs)
  8 Mbit/s H-MVIP
    Four DS1 formats byte-interleaved on two signaling and two data Highways
    125 µs refresh rate
    Slip buffers enabled (receive system clock and frame are inputs)
    H.100 compliant option for frame pulse width
- Serial port to read/write controls up to eight line interface transceivers ("Host Mode") with broadcast option
- Selection of one of eight DS1 line interfaces (receive line, receive terminal, or transmit) to monitor clock, frame pulse and data
- Microprocessor global reset, masks, polling registers, interrupt polarity and latch edge control
- Motorola split address/data with LDS option or Intel split address/data
- Global alarm Indications with separate channel pointers for DS1 alarms, FDL activity, and loopbacks
- Global interrupt mask bits
- Interrupt on alarms
  Positive edge
  Negative edge
  Both edges
- Hardware interrupt polarity selection
- Two reference clock outputs at 8 kHz or 1544 kHz with freeze on LOS and with the 8 kHz synchronized to the frame pulse as an option.
- IEEE 1149.1 boundary scan
- Ability to tristate all outputs for in-circuit testing with a single control lead.
- Synchronization start position is programmable to any receive or transmit bit position on the system side to any one of 256 positions
- External shadow register clock input

T1Fx8 Feature Enhancements and Differences Versus the QT1F-*Plus*

- Framing:

  SF/ESF - automatic search

  2 or 4 kbit/s HDL with fixed value in 2 kbit/s non-data link

  Individual transmit or receive bypass

- Line Interface:

  Alarm muxed in NRZ - LOS/fast sync/BPV; LOS input is separate pin for QT1F-*Plus*

- The frame pulse output option (fast sync) on the T1Fx8 TNEGn lead is programmable to 1.5 ms (SF mode), 3.0 ms (ESF mode) or 125 µs; QT1F-*Plus* is only 1.5/3.0 ms
- Signaling:

  Enable/Freeze per DS0, per transmit or receive; QT1F-*Plus* is one control bit for transmit and receive per DS0

  Signaling A or B in SF, A, AB or ABCD in ESF and debounce for 2 superframes; QT1F-*Plus* is A, AB or ABCD in SF or ESF (QT1F-*Plus* “B” version only) with no debounce option

  DS0 RAI and AIS code substitution, AIS line to signaling highway DS0 AIS, RAI line to signaling highway DS0 RAI, system AIS to line DS0 AIS in ESF

- Slip buffer - receive and transmit delay value register (1.3 µs resolution)
- Slip of 192 bits/frame or 193 bits/frame (intact)
- Clocks - one-second clock, external, backplane oscillator, or 1 of 8 receive lines; QT1F-*Plus* has external only
- Two reference clock outputs at 8 kHz or 1544 kHz with freeze on LOS (the 8 kHz clock output can be synchronized to the frame pulse as an option which is not available on QT1F-*Plus)*
- Alarms - signaling change, AIS-CI/RAI-CI primitive supported; QT1F-*Plus* "B" supports AIS-CI and RAI-CI reception only
- Fractional T1 - transmit and receive marker as well as the QT1F-*Plus* gapped clock, separate lead in 256-lead package; TTAIXn - second input permits clear and robbed-bit signaling muxed; 56 kbit/s option as well as 64 kbit/s option; no signaling option; digital milliwatt and idle code
- HDLC 128 byte FIFO, back-to-back message support; automatic generation and transmission of performance message with microprocessor interrupt and modification ability
- Loopbacks: Detects ANSI Fractional T1 loopback Activate/Deactivate codes for N x DS0
- PRBS: Per channel generator/analyzer QRSS, 32 bit word, option for 56 kbit/s or 64 kbit/s framed and un-framed or N x DS0
- System Bus: MVIP and Transmission mode (like QT1F-*Plus*) with H-MVIP and Data modes which are only on the T1Fx8

APPLICATION EXAMPLES

The diagrams in Figure 1 and Figure 2 illustrate use of the T1Fx8 device to provide framing and DS0 access for a variety of T1 sources. Direct control of most commercial line interface unit devices (LIUs) is provided.

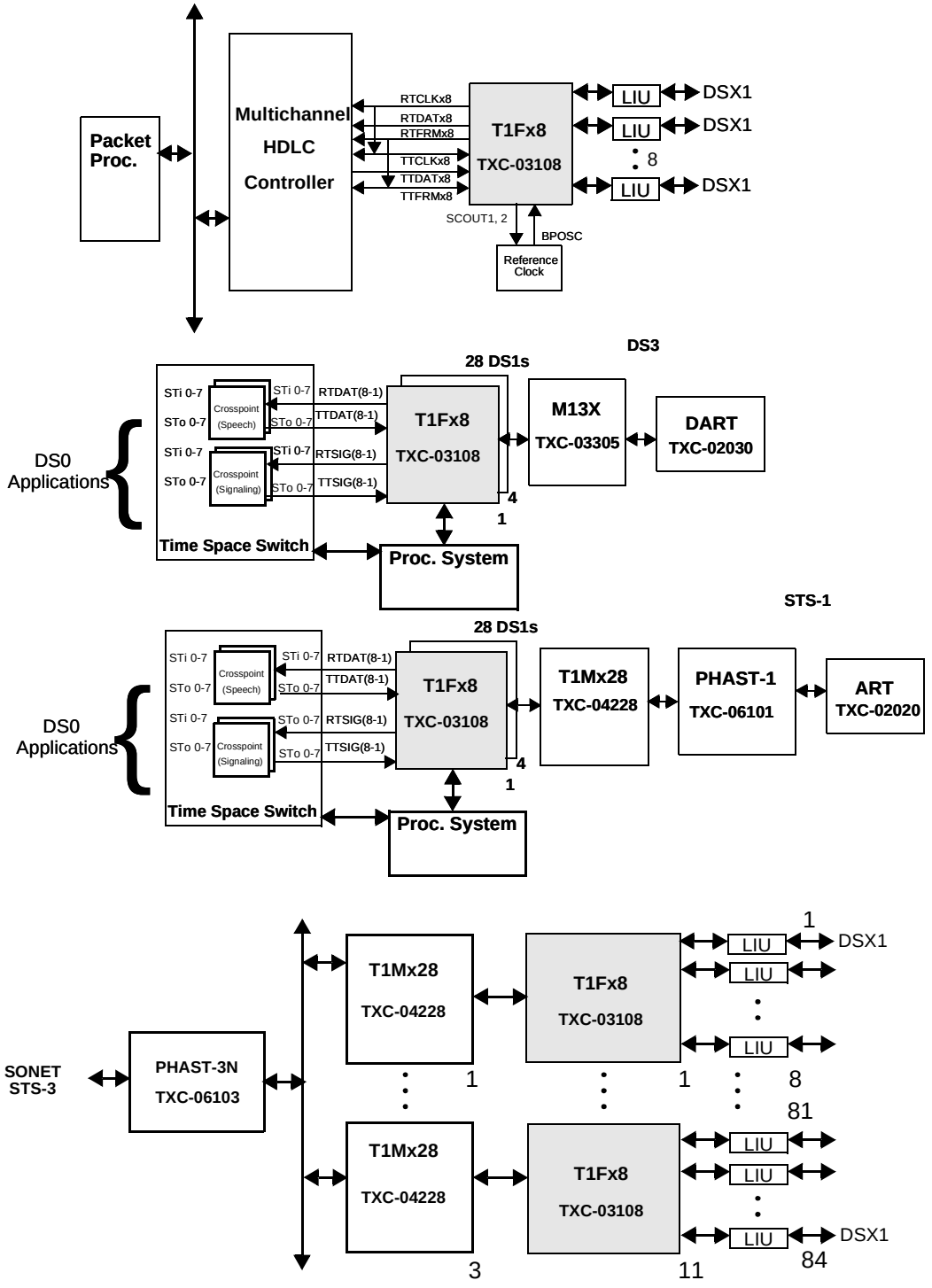


Figure 1. Example T1Fx8 TXC-03108 T1, Fractional T1, and DS0 Applications

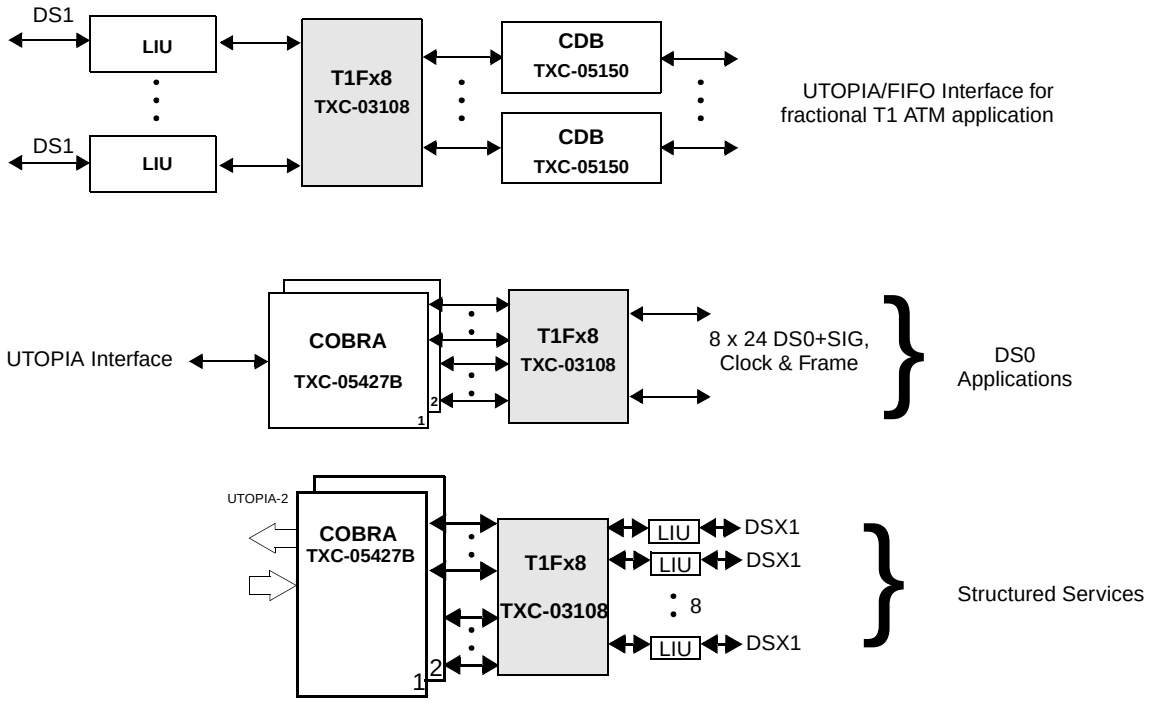
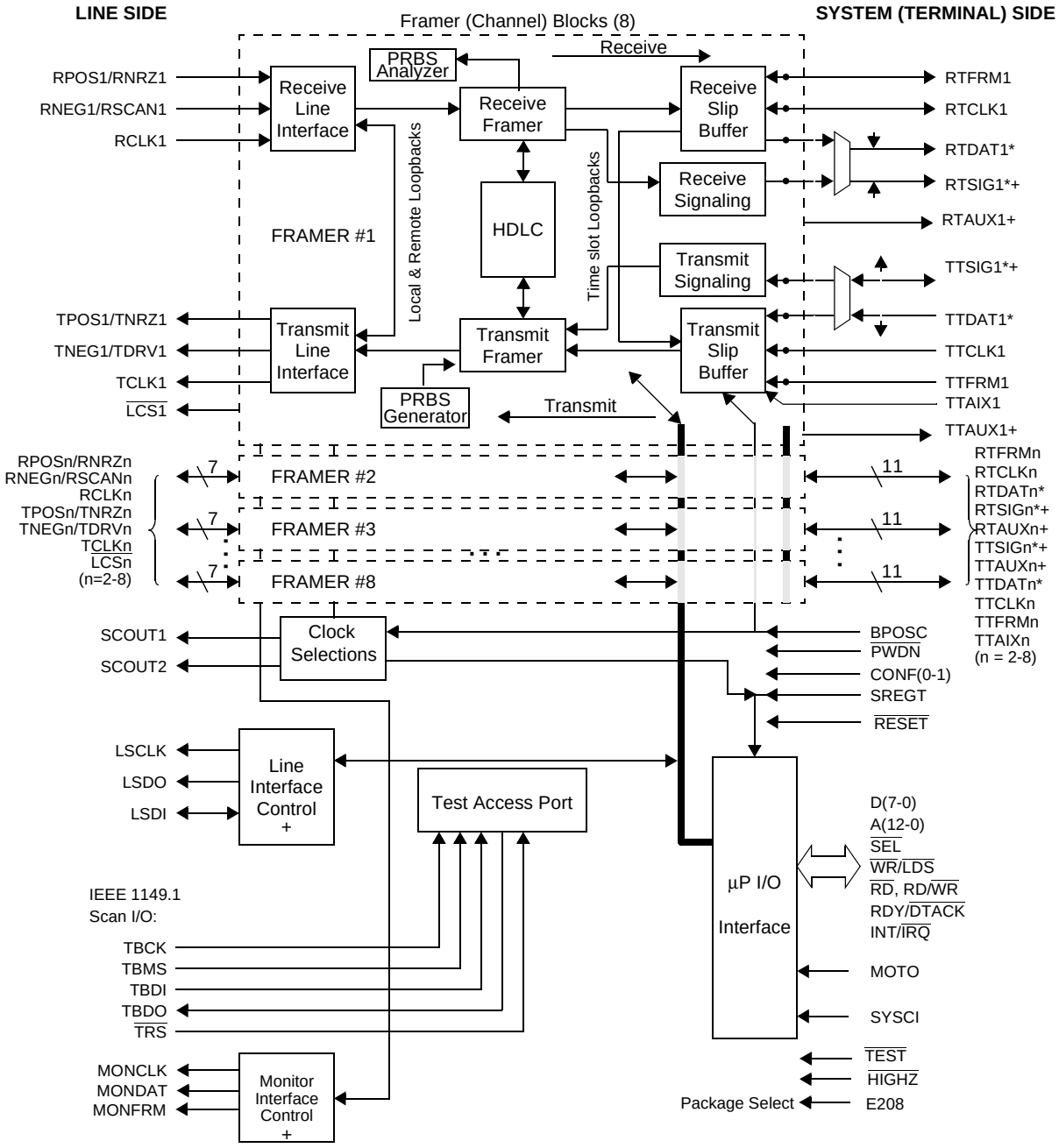


Figure 2. Example T1Fx8 TXC-03108 ATM Applications

FUNCTIONAL DESCRIPTION



* Note: Signaling and data for each group of four framers are multiplexed on framers 1 and 5 signaling and data leads for HMVIP/H.100 Mode.

\+ Note: For 208-lead PBGA, the Line Interface Control and Monitor Interface Control share leads based on the ESPBMON bit state, and TTSIGn/RTSIGn share leads with TTAUXn/RTAUXn based on the FTIM bit state.

Figure 3. T1Fx8 TXC-03108 Block Diagram

BLOCK DIAGRAM DESCRIPTION

A simplified block diagram of the T1Fx8 8-channel T1 Framer is shown in Figure 3. The T1Fx8 consists of the following major blocks: eight Framer blocks, Line Interface Control, Monitor Interface Control, Microprocessor Input/Output Interface, Clock Selections, and Test Access Port.

Each of the eight identical Framer blocks consists of the following blocks: Receive and Transmit Line Interface blocks, Receive and Transmit Framer blocks, HDLC block, Receive and Transmit Slip Buffer blocks, PRBS Generator, PRBS Analyzer, and Receive and Transmit Signaling blocks.

The Receive and Transmit Line Interface blocks connect each of the eight framers to an external line interface transceiver, which performs the LIU and clock recovery functions. The interface to the external line interface transceiver can be configured for two interface modes: a dual unipolar (rail) interface or a NRZ interface.

When the dual unipolar interface mode is selected, input data from the external line interface transceiver is clocked into the T1Fx8 on lead RPOSn and RNEGn using the recovered receive clock present on the RCLKn input lead (where the suffix n=1-8 identifies one of the eight framers). In the transmit direction, unipolar data is clocked out of the T1Fx8 on leads TPOSn and TNEGn by the transmit line clock present on the TCLKn output lead. For reduced power dissipation in protection switching applications, the TCLKn, TPOSn, and TNEGn leads for the four framers may be forced low by setting control bits. Control bits are provided in the memory map which enable the unipolar data to be clocked in and out of the T1Fx8 on either edge of the clocks. For the dual unipolar interface mode, the T1Fx8 provides either a Bipolar with Eight Zero Substitution (B8ZS), or an Alternate Mark Inversion (AMI), coder and decoder function, and Loss Of Signal detection. The Loss Of Signal detector meets the requirements specified in the ANSI T1.231 documents listed above in the 8-channel T1 Framer Features section. A 16-bit performance counter is provided for each framer, for counting B8ZS coding violation errors. An option is provided to also include excessive zeros in the coding violations count.

When the NRZ interface mode is selected, NRZ data is clocked in at the RNRZn lead by the recovered received clock present on the RCLKn lead. The NRZ data is clocked out of the T1Fx8 on the TNRZn lead by the transmit system clock present on the TCLKn output lead. Control bits are provided in the memory map which enable the NRZ data to be clocked in and out of the T1Fx8 on either edge of the clocks. In NRZ interface mode, the B8ZS or AMI coder and decoder functions are bypassed. However, bipolar violations which are detected in the external line interface transceiver may be clocked into the T1Fx8 on the RNEGn/RSCANn lead and counted in the associated 16-bit coding violation performance counter. The RNEGn/RSCANn lead may also be used for forwarding an externally detected Loss Of Signal or providing a fast synchronization signal input. The TNEGn/TDRVn output may be used in NRZ mode as a drive bit or fast synchronization output. The Remote Line Loopback function for each framer is also implemented in the Line Interface blocks.

The Receive Framer block for each framer performs frame synchronization alignment. When frame alignment is acquired, the signaling bits are forwarded to the Receive Signaling block for buffering, microprocessor access, and formatting into the signaling highway data stream. The frame synchronization circuit has framing option for the SF and ESF formats. For the SF format, Fs or Ft, or Fs and Ft bits can be used for frame alignment. For the ESF format, FPS, or FPS and a valid CRC-6, may be used. The frame synchronizing circuit meets the framing requirements specified in the ANSI documents. The Out Of Frame alarm criteria can be programmed to use 2 out of 4, 5, or 6 framing bits in error. Framing bit errors and CRC-6 errors are counted in performance counters. An automatic framing option is provided that alternatively searches for SF and ESF until framing is found. The Receive Framer block also monitors and detects the RAI (Yellow) alarm for either the SF (D4 or Japanese) or ESF formats and AIS. Detection of RAI-CI and AIS-CI primitives is supported. A non-framing mode can be enabled when the T1Fx8 is configured in the Transmission or Data Modes. The non-framing mode bypasses the Receive Framer block and optionally the Receive Slip Buffer block.

Each Receive Slip Buffer block controls DS0 access and retiming for framer n by using a two-frame receive slip buffer that can be optionally bypassed in the Transmission and Data Mode. When the receive slip buffer is enabled, received DS0s are written into the buffer by recovered receive clock RCLKn, and read out as data (RTDATn) from the receive slip buffer by the system input clock RTCLKn. A phase shift between the two clocks is detected in this block and a deletion or repetition of one frame of data (24 DS0 channels) is provided when the buffer reaches an almost full or almost empty condition, respectively. Microprocessor access to a delay register (difference between write and read pointers)

as well as the read and write pointers is also provided. The framing bits may either be slipped or not as an option; when the framing bits are slipped and the receive framer is disabled, a non-SF or ESF T1 signal can be retimed but passed intact through the T1Fx8. Slip alarm indications are provided for the microprocessor. The receive slip buffer may be recentered by the microprocessor, or automatically. Individual DS0s can be accessed by the microprocessor for the insertion or detection of system idle, test pattern or out of service codes. When the receive slip buffer is bypassed, the receive clock (RTCLKn) and data (RTDATn and RTSIGn) are provided as outputs, along with a receive synchronization signal (RSYNCn).

For 2, 4 or 16-state signaling (robbed-bit signaling), a three times 96-bit signaling buffer is used to store the signaling bits which have been extracted by the Receive Framer. The signaling buffer may be debounced, read, frozen and written to by the microprocessor. This feature permits both signaling to or from the microprocessor (call control) as well as trunk conditioning under control of the microprocessor. If signaling is disabled for a particular channel, the ABCD signaling bits for that time slot will be frozen in their present states. When a loss of signal or an out of frame condition is detected, the signaling bits are also automatically frozen in their present states. The signaling bit states are held until framing has been recovered. For non-switched 56 kbit/s service, the eighth bit of every DS0 may be set to a one. For GR-253-CORE applications, DS0 alarms are supported for full DS1 applications.

On the terminal side, the system interface interconnects the eight framers with the system. For each framer there is a separate receive and transmit highway for the Transmission, Data and MVIP interface Modes of operation. The receive highway consists of a data bus (RTDATn), a signaling bus (RTSIGn), a clock (RTCLKn), and a synchronization signal (RTFRMn). The transmit highway consists of a data bus (TTDATn), a signaling bus (TTSIGn), a clock (TTCLKn), and a synchronization signal (TTFRMn). In the Transmission Mode, the system interface operates at 1.544 MHz, with channels in the data highway, and signaling and alarms on the signaling highway. The receive and transmit system interfaces are synchronized by multiframe pulses that occur at 3-millisecond intervals. Twenty-four frames are sent on the data and signaling highways within the 3-millisecond period, with each of the twenty-four frames consisting of 193-bits (24 DS0 channels plus the framing bit), which correspond to a DS1 frame. The receive and transmit slip buffers can be individually bypassed in this Mode. The Data Mode is very similar to the Transmission Mode except that the synchronization signal occurs every 125 microseconds and the signaling highway carries the all signaling bits as nibbles every frame.

To support fractional T1 applications in Transmission and Data Modes, a Gapped Clock or Marker pulse may be individually programmed for each transmit or receive DS0 (7 or 8 bits wide) and is supplied on leads RTAUXn and TTAUXn. In addition, an auxiliary data highway is provided and the transmit side system DS0s may come from either TTDATn, TTAIXn, the Receive Slip Buffer (DS0 loopback), digital milliwatt or programmable idle code which is selectable on a per DS0 basis.

When the MVIP Mode is selected, the system interface also consists of receive and transmit data highways. However, the receive and transmit system interfaces are synchronized by pulses occurring at 125-microsecond intervals in this Mode. The receive and transmit slip buffers must always be enabled in this Mode. Each frame consists of 32 time slots which carry the DS0 channels in defined time slots on the data highway. The signaling highway also carries 32 time slots, which contain the signaling states for each channel. RTCLKn and TTCLKn are always inputs at 2.048 MHz. Gapped clock or Marker pulses and the auxiliary input are not available in this Mode.

The T1Fx8 also supports an H-MVIP/H.100 Mode on the system side. The data and signaling highways from framers 1 through 4, essentially operating in MVIP Mode, are byte-interleaved, sharing the RTDAT1, TTDAT1, RTSIG1 and TTSIG1 leads; RTCLK1 and TTCLK1 operate at 16.384 MHz with RTFRM1 and TTFRM1 providing either H-MVIP or H.100 synchronization pulses at 125-microsecond intervals. Framers 5 through 8 share the system side leads for framer number 5 in a like manner. Gapped clock or Marker pulses and the auxiliary input are not available in this Mode.

A transmit slip buffer is provided to absorb low speed jitter in the transmit data. Each Transmit Slip Buffer block controls DS0 access and retiming for the framer by using a two-frame buffer that can be optionally bypassed in the Transmission and Data Mode. When the transmit slip buffer is enabled, transmit DS0s are written into the buffer by the transmit system clock (TTCLKn), and they are optionally read out from the buffer by the receive clock (RCLKn) or local oscillator (BPOSC) in any system side Mode or the transmit system clock (TTCLKn) in Transmission or Data Modes. A phase shift between the two clocks is detected in this block, and a deletion or repetition of one frame of data (i.e., 24 DS0 channels) is provided when the buffer reaches an almost full or almost empty condition, respectively. Microprocessor

access to a delay register (difference between write and read pointers) as well as the read and write pointers is also provided. Slip buffer alarm indications are also provided. The slip buffer may be recentered by the microprocessor, or automatically. Individual DS0s can be accessed by the microprocessor for the insertion or detection of system idle, test pattern or out of service codes.

The Transmit Framer block forms the frame (SF or ESF formats) with DS0 channels read from the Transmit Slip Buffer block, PRBS Generator block or system interface, and signaling information from the Transmit Signaling block. The HDLC bits (m-bits, see Figure 45 in Datasheet Ed. 3, May 2001) in the ESF format can be inserted from the HDLC block or from the system interface (in Transmission and Data Modes only). The CRC-6 is calculated and inserted for the ESF format. The RAI (Yellow) alarm indication is inserted by the microprocessor, or via the signaling highway (TTSIGn) in Transmission Mode only. RAI for SF format, and loop-up and loop-down codes, can be inserted, if selected. A single frame bit error, or CRC-6 error, can be generated for test purposes. The Transmit Framer and Transmit Slip Buffer can be bypassed if the unframed mode of operation is selected in the Transmission or Data Modes. An option to slip buffer the framing bits is provided similar to that in the Receive Slip Buffer Block. Generation of the primitives for RAI-CI and AIS- CI are also provided.

Each framer has a full duplex HDLC link controller. The HDLC link controller can be configured to send and receive messages using the 4 kbit/s m-bits in the ESF format. A 128-byte FIFO is provided in each direction. Interrupt and status alarm support is provided to facilitate FIFO servicing for long messages. The HDLC link controller supports zero bit stuffing/destuffing, ITU-T CRC generation/checking, flag generation/detection, abort generation/detection, start of frame detection, end of frame detection, and FIFO underflows and overflows. Back-to-back message reception is supported. Bit code reception and transmission are supported in this block. This block may be configured to automatically send an ANSI T1.403 PRM every second. Registers are provided to set up the TEI, SAPI, Control, C/R, EA, R, and U1/2 fields; CRC error range, SEFs, slips, BPVs, frame bit errors and payload loopback status are collected for each 1-second report. Handshaking is provided to share the HDLC controller with microprocessor-generated messages.

Each framer has a dual PRBS/Code Word Generator block and dual Analyzer block. One Generator and Analyzer supports the QRSS, 32-bit programmable Code Words and 2^{15}-1 patterns. The other Generator and Analyzer support the ANSI T1.403-1998 DS0 loopback activate and deactivate sequences. Both may be used simultaneously for fully compliant testing. The Analyzers monitor the fractional or full T1 that is received and framed (N x DS0 and Code Word). The Generators substitute for the DS1 or N x DS0 from the Transmit Slip Buffer or Transmit System side.

The Line Interface Control block is a common block to all eight framers that provides a serial port for communicating with external line interface transceivers that support 'Host Mode' operation. This allows the system microprocessor to control the transceivers through the T1Fx8. The interface consists of a data output lead (LSDO), clock output lead (LSCLK), and a data input lead (LSDI). These signals are shared by all of the transceivers. Each transceiver is selected by the T1Fx8, using individual chip select output signals ($\overline{\text{LCSn}}$). In addition, a general purpose input lead (RSCANn) can be used in NRZ mode to generate a maskable interrupt.

The Test Access Port block is common to all eight framers and includes a five-lead Test Access Port (TAP) that conforms to the IEEE 1149.1 standard. This Test Access Port block provides external boundary scan to read and write the T1Fx8 input and output leads from the TAP for board and component testing. In addition, a 4-byte read-only memory location is provided for reading the JEDEC manufacturer ID, T1Fx8 part number, and version number of the part.

The T1Fx8 provides a common Monitor Interface Control block. Any receive (before or after framing) or transmit data, clock and frame sync signal may be placed on a common tristateable bus which can be shared with other T1Fx8 devices. This permits any DS1 to be brought out for testing or other applications.

A common Clock Selections Block is provided that generates two reference outputs, each derived from one of the eight RCLKn signals, with both at either 1.544 MHz or 8 kHz, with the 8 kHz outputs synchronized to the received frame. The reference clock outputs may be placed on a tristateable bus which can be shared with other T1Fx8 devices. A selected output will go low on Loss Of Signal to prevent false drifting of a clock slave system. To facilitate the Automatic PRM feature, SF loop codes, DS0 loopbacks and the shadow registers, this block can divide down either the backplane oscillator (BPOSC) or one of the eight RCLKn signals for a 1-second reference.

The T1Fx8 can be configured to operate with either Intel or Motorola-compatible microprocessors via the Microprocessor Input/Output Interface block. Interrupt capability is provided with global and individual framer mask bits as well as activity registers to guide software quickly to the exact cause of an interrupt. An option is provided which permits interrupt polarity inversion. An external system clock (SYSCI) is used to run the internal state machines.

SELECTED PARAMETER VALUES

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	+3.9	V	Note 1
DC input voltage	V_{IN}	-0.5	5.5	V	Note 1
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient Operating Temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity	RH		100	%	non-condensing
ESD Classification	ESD	Absolute value 2000		V	See Note 3.
LATCH-UP	LU				Meets JEDEC STD-78

Notes: 1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.

2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.

3. Absolute value tested per MIL-STD-883D, Method 3015.7.

THERMAL CHARACTERISTICS

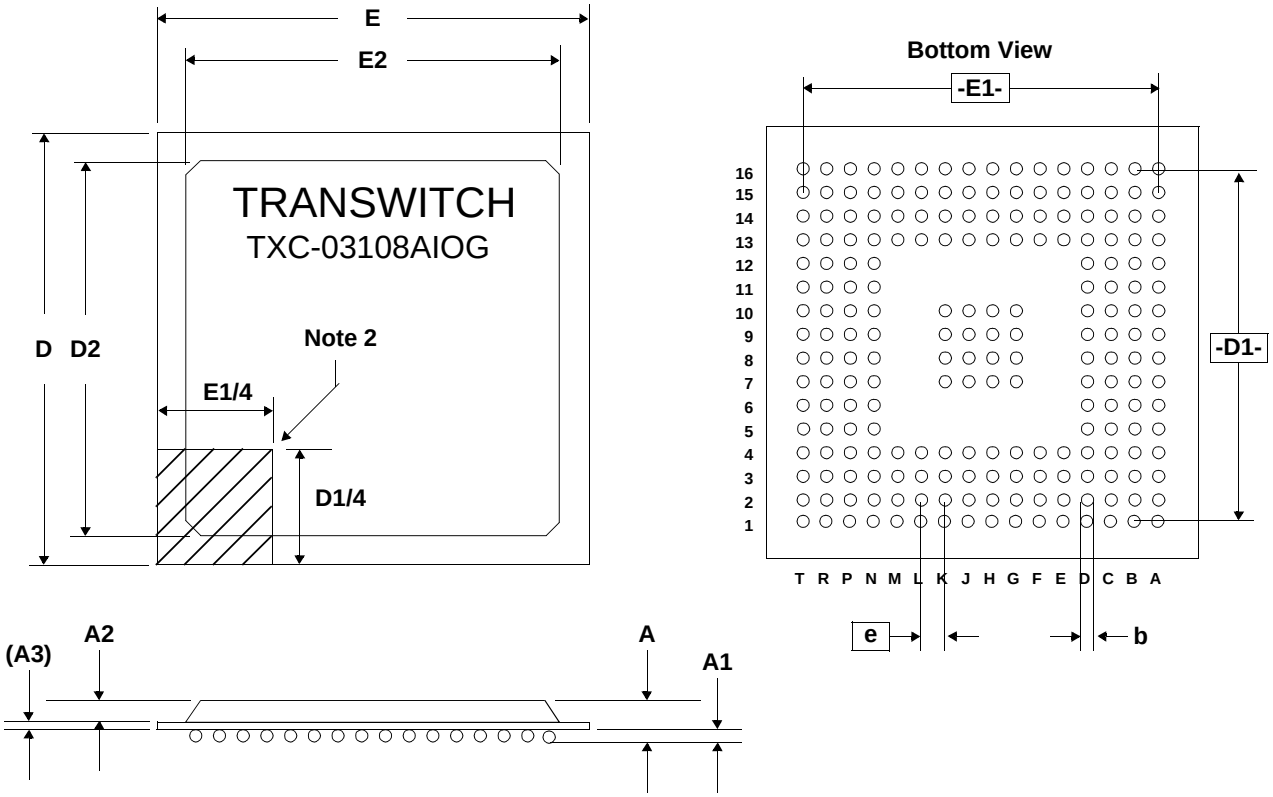
Parameter	Min	Typ	Max	Unit	Test Conditions
208-lead BGA thermal resistance: junction to ambient			38.0	$^oC/W$	0 ft/min linear airflow
256-lead BGA thermal resistance: junction to ambient			25.0	$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	3.15	3.30	3.45	V	
I_{DD} (outputs loaded)		82[1]	140[2]	mA	1. All channels operating. Output load 30 pF. SYSCI at 16 MHz. Transmission, MVIP or Data Mode. 2. All channels operating. Output load 30 pF. SYSCI at 25 MHz. H-MVIP Mode.
P_{DD} (outputs loaded)		270[1]	485[2]	mW	
I_{DD} (outputs loaded)		67		mA	All channels powered down (lead $\overline{PWDN}$ low). Output load 30 pF. SYSCI at 16 MHz.
P_{DD} (outputs loaded)		220		mW	

PACKAGE INFORMATION

The T1Fx8 device is available in two package formats. One is a 208-lead small outline plastic ball grid array package suitable for surface mounting, as illustrated in Figure 4. The other is a 256-lead plastic ball grid array package suitable for surface mounting, as illustrated in Figure 5.

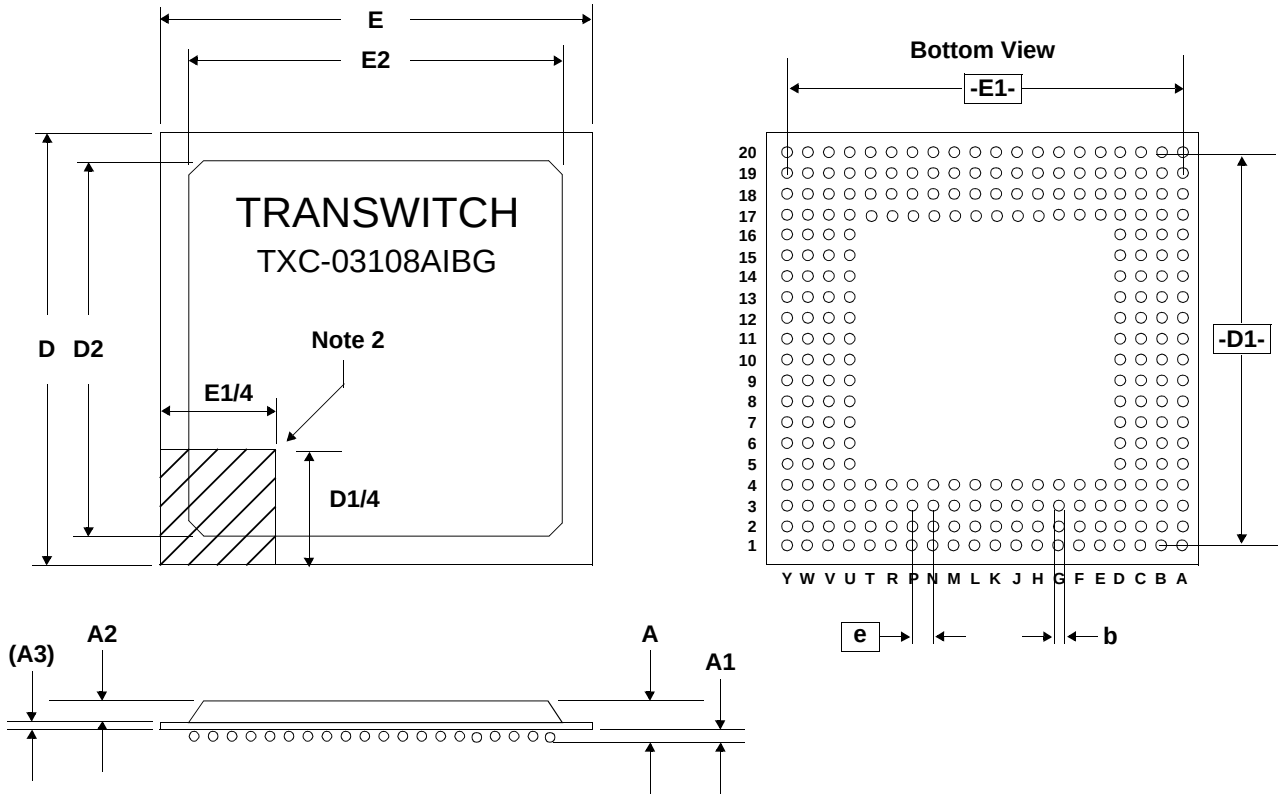


Notes:

1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.
3. Size of array: 16 x 16, JEDEC code MO-151-AAF-1

Dimension (Note 1)	Min	Max
A A1 A2	1.35 0.30 0.75	1.75 0.50 0.85
A3 (Ref.)	0.36	
b	0.40	0.60
D	17.00	
D1 (BSC)	15.00	
D2	15.00	15.70
E	17.00	
E1 (BSC)	15.00	
E2	15.00	15.70
e (BSC)	1.00	

Figure 4. T1FX8 TXC-03108 208-Lead Plastic Ball Grid Array Package Diagram



Notes:

1. All dimensions are in millimeters. Values shown are for reference only
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.
3. Size of array: 20 x 20, JEDEC code MO-151-BAL-2.

Dimension (Note 1)	Min	Max
A	1.92	2.32
A1	0.50	0.70
A2	1.12	1.22
A3 (Ref.)	0.36	
b	0.60	0.90
D	27.00	
D1 (BSC)	24.13	
D2	23.50	24.70
E	27.00	
E1 (BSC)	24.13	
E2	23.50	24.70
e (BSC)	1.27	

Figure 5. T1FX8 TXC-03108 256-Lead Plastic Ball Grid Array Package Diagram

ORDERING INFORMATION

Part Number: TXC-03108AIOG	208-lead Small Outline Plastic Ball Grid Array Package
Part Number: TXC-03108AIBG	256-lead Standard Outline Plastic Ball Grid Array Package

RELATED PRODUCTS

TXC-02020, ART VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). ART performs the transmit and receive line interface functions required for transmission of STS-1 (51.840 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface.

TXC-02021, ARTE VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). ARTE has the same functionality as ART, plus extended features.

TXC-02030, DART VLSI Device (Advanced E3/DS3 Receiver/Transmitter). DART performs the transmit and receive line interface functions required for transmission of E3 (34.368 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface.

TXC-02302B, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). Provides complete STS-3/STM-1 frame synchronization on incoming 155 Mbit/s signals in a single low-power unit. It has both clock and data outputs on the line side.

TXC-03001B, SOT-1 VLSI Device (SONET STS-1 Overhead Terminator). Performs Section, Line, and Path Overhead processing for STS-1 SONET signals. Interfaces are provided for both Section and Line Orderwire and Datacom channels. Further, control bits in the Memory Map enable the SOT-1 to perform loopback and serial or parallel I/O.

TXC-03003B, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This is a programmable device that performs section, line and path overhead processing for STM-1/STS-3/STS-3c signals. The SOT-3 device performs pointer generation (with internal pointer justification) with respect to external clock timing in both the transmit and receive directions.

TXC-03011, SOT-1E VLSI Device (SONET STS-1 Overhead Terminator). This device provides extended features relative to the 84-pin TXC-03001B SOT-1 devices, and it has a 144-pin package.

TXC-03102, QDS1F VLSI Device (Quad DS1 Framer). A 4-channel framer for voice and data applications. This device handles all logical interfacing functionality to a T1 line. This device is not recommended for use in new designs; use TXC-03103.

TXC-03103, QT1F-*Plus* VLSI Device (Quad T1 Framer-*Plus*). A 4-channel framer for voice and data applications. This device handles all logical interfacing functionality to a T1 line. It has extended features relative to the QDS1F device. Requires +5.0 V power supply. This device is not recommended for use in new designs; use TXC-03103C.

TXC-03103C, QT1F-Plus VLSI Device (Quad T1 Framer-Plus). A 4-channel DS1 (1.544 Mbit/s) framer designed with extended features for voice and data communications applications.

TXC-03303, M13E VLSI Device (DS3/T1 Mux/Demux, Extended Features). This single chip multiplex/demultiplex device provides the complete interfacing function between a single DS3 signal and 28 independent DS1 signals.

TXC-03305, M13X VLSI Device (DS3/DS1 Mux/Demux). This single-chip device provides the functions needed to multiplex and demultiplex 28 independent DS1 signals to and from a DS3 signal with either an M13 or C-bit frame format. It includes some enhanced features relative to the M13E device.

TXC-04228, T1Mx28 VLSI Device (DS1 Mapper 28-Channel). Maps twenty-eight 1.544 Mbit/s DS1 signals into any twenty-eight selected asynchronous or byte-synchronous mode VT1.5 or TU-11 virtual tributaries carried in a SONET or SDH synchronous payload envelope.

TXC-04251, QT1M VLSI Device (Quad DS1 to VT1.5 or TU-11 Async Mapper-Desync). Interconnects four DS1 signals with any four asynchronous mode VT1.5 or TU-11 tributaries carried in SONET STS-1 or SDH AU-3 rate payload interface.

TXC-05150, CDB VLSI Device (Cell Delineation Block). Provides cell delineation for ATM cells carried in a physical line at rates of 1.544 to 155 Mbit/s.

TXC-05427C, COBRA Device (COnstant Bit Rate ATM Adaptation Layer 1). This is a four-channel device that implements all of the functions needed for circuit emulation over ATM. Both Unstructured service (e.g., 1544 kbit/s and 2048 kbit/s) and Structured service (e.g., n x 64 kbit/s) are supported. COBRA offers three clock modes: internal clock recovery based on the Synchronous Residual Time Stamp (SRTS), clock recovery based on the FIFO fill level (adaptive FIFO), and an external clock mode.

TXC-06101, PHAST-1 VLSI Device (SONET STS-1 Overhead Terminator). This device provides features similar to those of the TXC-03011 SOT-1E device, but it operates from a power supply of 3.3 volts rather than 5 volts.

TXC-06103, PHAST-3N VLSI Device (SONET/SDH STM-1, STS-3 or STS-3c Overhead Terminator) This PHAST-3N VLSI device provides a COMBUS interface for downstream devices and operates from a power supply of 3.3 volts.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator/Receiver). Programmable multi-rate test pattern generator and receiver in a single chip with serial, nibble, or byte interface capability.

- NOTES -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