TORISAN

ENGINEERING SPECIFICATIONS

TFT COLOR LCD MODULE

TM121XG-02L01

- 31cm (12.1 inch) diagonal
- XGA resolution (1024 x 768 pixels)
- LVDS (6 bits x RGB)
- Front mount / Slim (t=5.7mm Max.)
- With CFL backlight unit
- Nonglare surface type

(TENTATIVE)

Ver.4 Mar. 19, 2001

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REVISION HISTORY

DATE	REVISION NO.	PAGE	DESCRIPTIONS
Oct. 26, '99	Ver. 1	-	Initial Release
Nov. 30, '99	Ver. 2	3	Response time: tr 30ms → 32ms, tf 10ms → 13ms
		8	DCLK Frequency: 38.0MHz MIN → 60.0MHz MIN
Apr. 21, '00	Ver. 3	2	Power supply current: (300) mA TYP → 300mA TYP (600) mA MAX → 600mA MAX
		3	Brightness uniformity: Non → 1.45 MAX
			Color of CIE Coordinate: xR: (0.58) → (0.57), yR: (0.34) → (0.35) xG: (0.33) → (0.31), yG: (0.53) → (0.56) xB: (0.15) → (0.15), yB: (0.12) → (0.11) xW: 0.313 → 0.313 +/- 0.03, yW: 0.329 → 0.329 +/- 0.03
		4	BACKLIGHT CHARACTERISTICS: Operating life → CFL life time Note 2 about recommended CFL waveform was added.
		8	The descriptions of INTERFACE (LVDS) SIGNAL TIMING PARAMETERS and CYCLE JITTER of LVDS CLOCK were added.
		9	The description about DE and DATA timing was added to Note 2 in INTERNAL SIGNAL TIMING PARAMETERS (DE_MODE).
			The description about V_{IH}/V_{IL} was deleted.
		12 - 15	PRECAUTIONS: PRECAUTIONS were altered to same as Delivery specification.
Mar. 19, '01	Ver. 4	2	ELECTRICAL ABSOLUTE MAXIMUM RATINGS Define the Maximum value of Lamp supply voltage: V_{HV}=2000Vrms and V_{LGND}=100Vrms.
		4	BACKLIGHT CHARACTERISTICS Add Note3 and Note 4.
		8	INTERFACE (LVDS) SIGNAL TIMING PARAMETERS Remove the Specifications at T_{in}=18ns.
			CYCLEJITTER of LVDS CLOCK Change the example diagram. t_{CLK} MIN.18.0ns→15.0ns, t_{CLK} MAX.18.42ns→15.42ns
		11	POWER ON/OFF SEQUENCE REQUIREMENT Add the subscript "1,2,3,4,5,6,7" to "t". 0 < t_4 < 20ms → 0 < t_4 < 50ms, 1sec < t_5 → 150ms < t_5

MECHANICAL CHARACTERISTICS

Ta=25 degC

ITEM	SPECIFICATION	UNIT
Module size	275.0(W) x 199.0(H) x 5.7 Max.(t)	mm
Resolution	1024 x R.G.B(W) x 768(H)	pixel
Sub-pixel pitch	0.080(W) x 0.240(H)	mm
Pixel pitch	0.240(W) x 0.240(H)	mm
Active area	245.76(W) x 184.32(H)	mm
Effective viewing area	248.20(W) x 186.75(H)	mm
Bezel opening area	250.4(W) x 188.9(H)	mm
Weight	370 Typ.	g

ELECTRICAL ABSOLUTE MAXIMUM RATINGS

Ta=25 degC

ITEM	SYMBOL	MIN	MAX	UNIT	NOTE
Power supply voltage	V_{DD}-V_{SS}	-0.3	4.0	V	
Input voltage	V_I	V_{SS}-0.3	V_{DD}+0.3	V	
Lamp current	I_L	-	6.5	mA	
Lamp supply voltage	V_{HV}	-	2000	Vrms	
	V_{LGND}	-	100	Vrms	

ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

Ta=25 degC

ITEM	SYMBOL	CONDITIONS	MIN	MAX	UNIT	NOTE
Ambient temperature	T_{ST}	Storage	-20	60	degC	Note 1
	T_{OP}	Operation	0	50		
Humidity	-	Ta=40 degC max.	-	85	%RH	No condensation Note 2
Vibration	-	Storage	-	1.5	G	Note 3
Shock	-	Storage	-	50	G	XYZ 11ms/direction

[Note 1] Care should be taken so that the LCD module may not be subjected to the temperature beyond this specification.

[Note 2] Ta>40 degC: Absolute humidity shall be less than that of 85%RH/40 degC.

[Note 3] 10-200Hz, 30min/cycle, X/Y/Z each one cycle and except for resonant frequency.

ELECTRICAL CHARACTERISTICS

V_{DD}=3.3V ,f_V=60Hz ,f_{CLK}=65MHz ,Ta=25 degC

ITEM	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Power supply voltage	V_{DD}-V_{SS}		3.0	3.3	3.6	V	
LVDS input Threshold voltage	V_{TH}	High level	-	-	+100	mV	V_{CM}=1.2V
	V_{TL}	Low level	-100	-	-		
LVDS input Termination resistor	R_T		-	100	-	ohms	Internal
Power Supply current	I_{DD}	Note 1	-	300	600	mA	

[Note 1] Under the following display image :

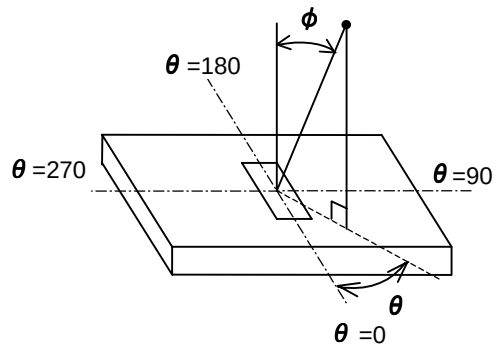
Typical Value: Display pattern is 64 gray scale bar.

[Note 2] V_{CM} : Common mode voltage of LVDS input

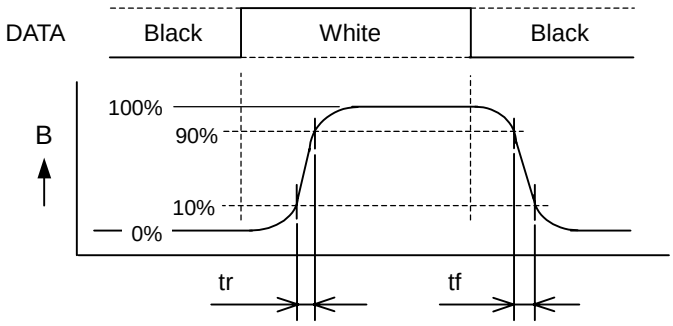
OPTICAL CHARACTERISTICS

Ta=25 degC, V_{DD}=3.3V, fv=60Hz

ITEM		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	NOTE
Brightness		B	ϕ =0 deg.		100	150	-	cd/m^2	Note 5,7,8
Brightness uniformity		δ_B	ϕ =0 deg.		-	-	1.45	-	Note 6,7,8
Contrast ratio		CR	ϕ =0 deg.		150	300	-	-	Note 2,4,8
Viewing angle range		ϕ	CR>10	θ= 0 deg.	30	-	-	deg.	Note 1,2, 4,8
				θ= 90 deg.	40	-	-		
				θ=180 deg.	10	-	-		
				θ=270 deg.	40	-	-		
Response time	Rise	tr	ϕ =0 deg.		-	32	50	ms.	Note 3,4,8
	Fall	tf			-	13	30		
Color of CIE Coordinate	Red	x	ϕ =0 deg.		-	(0.57)	-	-	Note 4,8
		y			-	(0.35)	-		
	Green	x			-	(0.31)	-		
		y			-	(0.56)	-		
	Blue	x			-	(0.15)	-		
		y			-	(0.11)	-		
	White	x			0.283	0.313	0.343		
		y			0.299	0.329	0.359		



[Note 1] ϕ and θ



[Note 3] Response time

[Note 2] The contrast ratio "CR" is defined as :

$$CR = \frac{\text{Brightness at White}}{\text{Brightness at Black}}$$

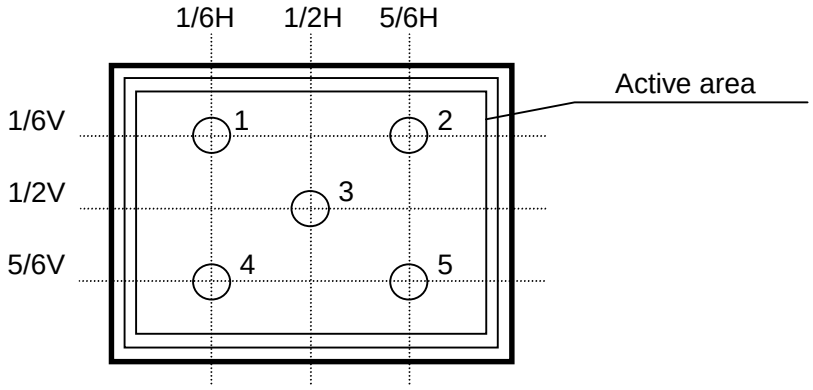
[Note 4] This shall be measured at center (point No.3 shown in Note 7).

[Note 5] The brightness shall be the average of five points.

[Note 6] The brightness uniformity " δ_B" is defined as :

$$\delta_B = \frac{\text{Maximum brightness of five points}}{\text{Minimum brightness of five points}}$$

[Note 7] Measurement points



Vp: Total Number of Vertical pixel
Hp: Total Number of horizontal pixel

[Note 8] Measurement condition

(1) Measurement equipment: BM-5A (TOPCON Corp.), Field=2 degree
(2) Ambient temperature Ta: 25 +/- 2 degC
(3) LCD: All pixels are WHITE, V_{DD}=3.3V, f_V=60Hz
(4) Measure after 30 minutes of CFL warm up.
(5) I_L=6.0 mArms with the CFL inverter CXA-L0612A-VJL (TDK).

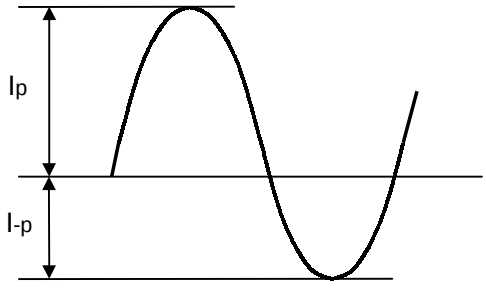
BACKLIGHT CHARACTERISTICS

Ta=25 degC

ITEM	SYM.	CONDITIOS	MIN	TYP	MAX	UNIT	NOTE
CFL voltage	V_L		-	560	-	Vrms	at I_L=6.0mArms
CFL current	I_L		3.0	-	6.0	mArms	(Recommended value)
Operating frequency	f_L		40	60	65	kHz	(Recommended value)
Start up voltage	V_S		-	-	1200	Vrms	at Ta=0 degC
CFL life time	t_{OL}		10000	-	-	hrs	at I_L=6.0 mArms

[Note 1] Backlight driving conditions (operating frequency f_L especially) may interfere with horizontal frequency f_H, causing the beat or flicker on the display.
Therefore the operating frequency f_L shall be adjusted in relation to horizontal frequency f_H to avoid interference.

[Note 2] If driving current waveform is asymmetrical, mercury deviation inside of CFL will incline to one side and consequently abnormal lighting may occur.
To prevent such unfavorable lighting, driving current waveform is asked to have unbalance rate of less than 10% and wave-height rate of less than $\sqrt{2}$ +/- 10%.
And this driving waveform shall be confirmed in your system.



Current waveform

Unbalance rate = $| I_p - I_{-p} | / I_L \times 100$ (%)

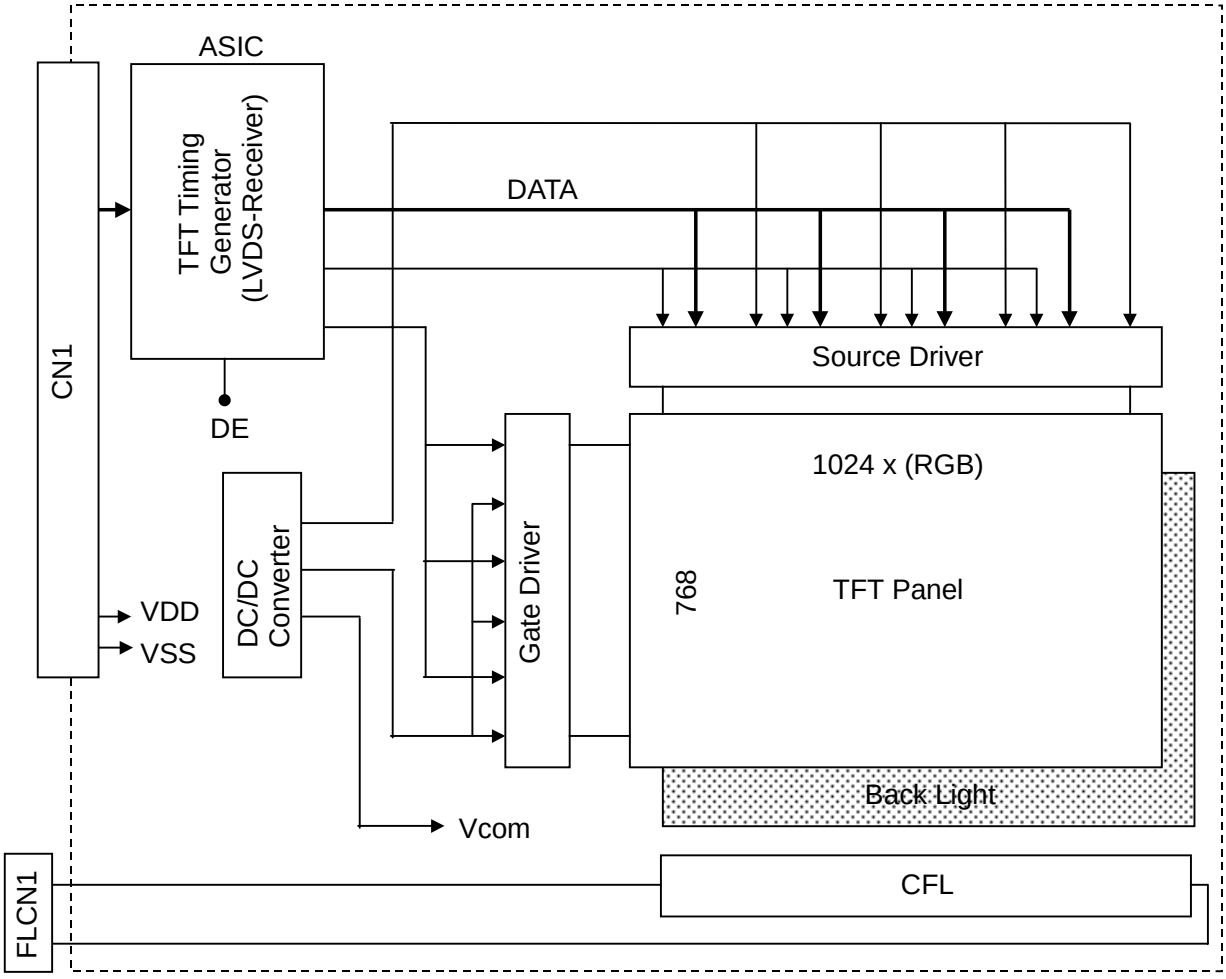
Wave-height rate = I_p (or I_{-p}) / I_L

I_p : High peak value
I_{-p} : Low peak value
I_L : Effective value

[Note 3] The inverter open voltage should be larger than start up voltage, otherwise backlight may blinking for a moment after turns on or not be turned on.
And this voltage should be applied to lamp for more than 1 second to start up, otherwise backlight may not be turned on.

[Note 4] The inverter of ground reference type should be used.
The inverter of ground floating type should not be used.

BLOCK DIAGRAM



INTERFACE PIN CONNECTIONS

LCM : CN1

PIN NO.	SYMBOL	FUNCTION
1	VDD	Power Supply (3.3V +/- 0.3V)
2	VDD	Power Supply (3.3V +/- 0.3V)
3	VSS	Ground
4	VSS	Ground
5	Rin0-	Receiver Signal(-)
6	Rin0+	Receiver Signal(+)
7	VSS	Ground
8	Rin1-	Receiver Signal(-)
9	Rin1+	Receiver Signal(+)
10	VSS	Ground
11	Rin2-	Receiver Signal(-)
12	Rin2+	Receiver Signal(+)
13	VSS	Ground
14	RCLK-	Clock Signal(-)
15	RCLK+	Clock Signal(+)
16	VSS	Ground
17	NC	No Connection (Should be open during operation.)
18	NC	No Connection (Should be open during operation.)
19	VSS	Ground
20	VSS	Ground

CN1 : FI-SEB20P-HF10 (JAE)
Suitable mating connector: FI-S20S/FI-S20M/FI-S20MR (JAE)

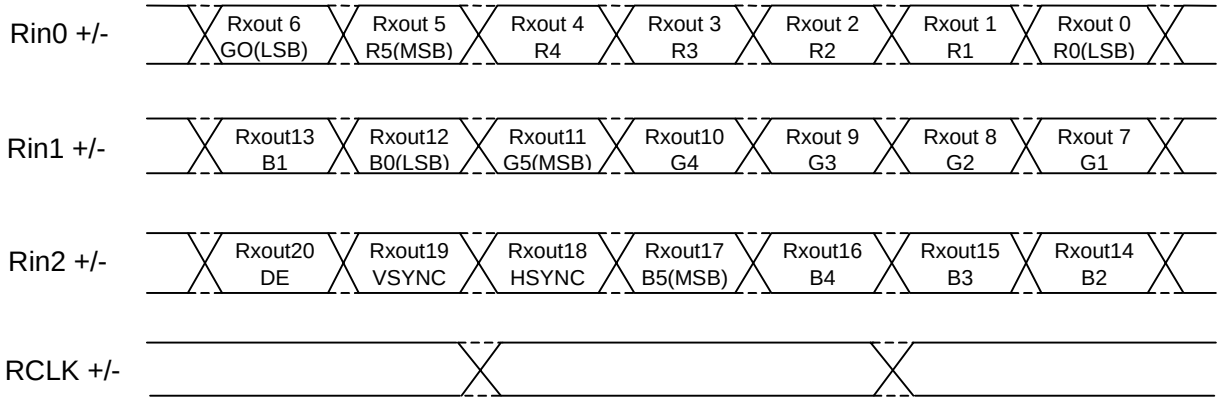
[Note 1] Internal termination resistors of LVDS input lines are 100 ohms.

Backlight : FLCN1

PIN NO.	SYMBOL	FUNCTION
1	HV	High voltage for CFL
2	LGND	Low voltage for CFL

FLCN1 : BHSR-02VS-1 (JST)
Suitable mating connector: SM02B-BHSS-1 (JST)

INTERFACE (LVDS) DATA ASSIGNMENT



INTERFACE SIGNALS

SYMBOL	FUNCTION
DCLK	Data Clock
HSYNC	Horizontal Sync - This signal initiates a new line (negative). - unused
VSYNC	Vertical Sync - This signal initiates a new frame (negative). - unused
DE	Data Enable (positive)
R0	Red Data (LSB)
R1	Red Data
R2	Red Data
R3	Red Data
R4	Red Data
R5	Red Data (MSB)
G0	Green Data (LSB)
G1	Green Data
G2	Green Data
G3	Green Data
G4	Green Data
G5	Green Data (MSB)
B0	Blue Data (LSB)
B1	Blue Data
B2	Blue Data
B3	Blue Data
B4	Blue Data
B5	Blue Data (MSB)

[Note 1] The valid synchronous signals are DCLK and DE. HSYNC and VSYNC are invalid.

[Note 2] INTERFACE SIGNALS are loaded from LVDS-transmitter to TFT Timing generator with LVDS sequence. (See BLOCK DIAGRAM.)

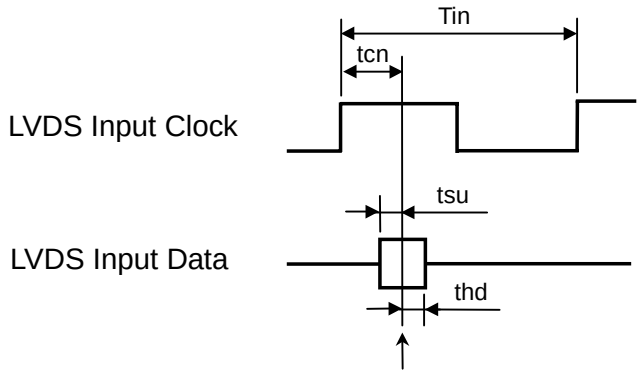
INTERFACE (LVDS) SIGNAL TIMING PARAMETERS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Data Setup Time	tsu	600	-	-	ps	at Tin=15ns Note 1
Data Hold Time	thd	600	-	-	ps	

[Note 1] In the following timing waveform, the n-th edge of internal imaginary clock tcn, which is sampling position of LVDS input data signal, is given by:

tcn = (2n-1) Tin / 14 (n=1,2, ~ 7)

where Tin is period of LVDS input clock.
For this imaginary clock edge, data setup time is tsu and data hold time is thd, respectively.



n-th edge of internal imaginary clock (data sampling position)

CYCLE JITTER of LVDS CLOCK

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
P-P of jitter / 100 cycles	tcj1	-	-	300	ps	Note 1
Jitter rate	tcj2	-	-	20	ps/cycle	

[Note 1] Please confirm tcj2 (Jitter rate), only if tcj1 (P-P of jitter/100cycles) exceeds 300ps.

[Additional explanation]

Right diagram shows the example of CYCLE JITTER of LVDS CLOCK.

According to this diagram, tCLK MIN. is 18.0ns and tCLK MAX. is 15.42ns between 0nc and 100nc. The tcj1 (P-P of jitter / 100 cycles) in this sphere is

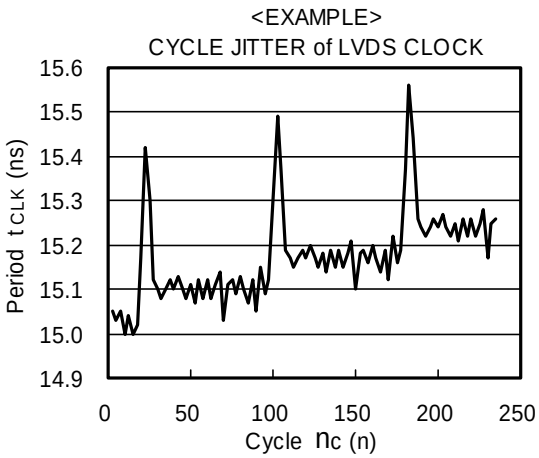
tcj1=15.42-15.0=0.42 ns

and out of specification (300ps MAX.).
So, it is neccesary to measure tcj2 (jitter rate) and to judge whether it conform to above specification.

According to the diagram, the sharpest fluctuation of tCLK is 0.4ns per 5nc. So that, the tcj2 in this sphere is

tcj2=0.4/5=0.08 ns/cycle

and larger than specification (20ps/cycle MAX.).



In conclusion, normal function of the LCD module can not be assured in this case.

INTERNAL SIGNAL TIMING PARAMETERS (DE_MODE)

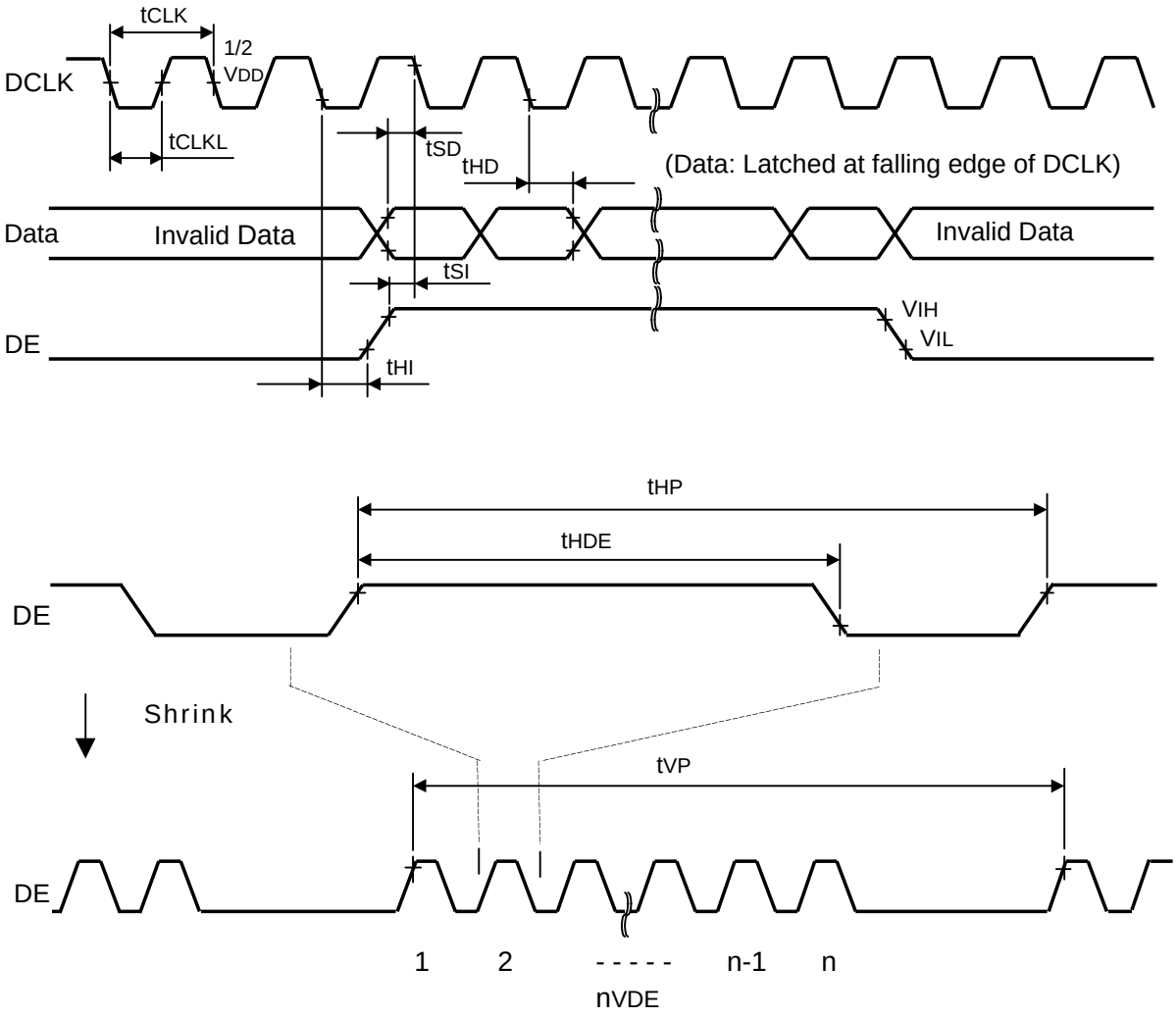
PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	NOTE
DCLK	Frequency	f_{CLK}	60.0	65.0	66.6	MHz	$t_{CLK}=1/f_{CLK}$
	Duty	D	(0.40)	0.50	(0.60)	-	$D=t_{CLKL}/t_{CLK}$
DE	Setup Time	t_{SI}	(3)	-	-	ns	for DCLK
	Hold Time	t_{HI}	(1.5)	-	-	ns	
	Horiz. Period	t_{HP}	1270	1344	1450	t_{CLK}	
	Horiz. DE	t_{HDE}	1024	1024	t_{HP}-12	t_{CLK}	
	Vert. Period	t_{VP}	780	806	900	t_{HP}	60Hz typical
	Vert. DE	n_{VDE}	768	768	t_{VP}-5	n	
DATA	Setup Time	t_{SD}	(3)	-	-	ns	for DCLK
	Hold Time	t_{HD}	(1.5)	-	-	ns	

[Note 1] f_H (Horizontal Frequency) = $1/t_{HP}$
f_V (Vertical Frequency) = $1/t_{VP}$

[Note 2] These signal timing parameters are specified at the digital inputs of LVDS transmitter. With respect to setup time and hold time for DE and DATA signals, please refer to input signal specification of LVDS transmitter.

Recommended LVDS transmitter : SN75LVDS84 (TI)

INTERNAL SIGNAL TIMING DIAGRAM (DE_MODE)

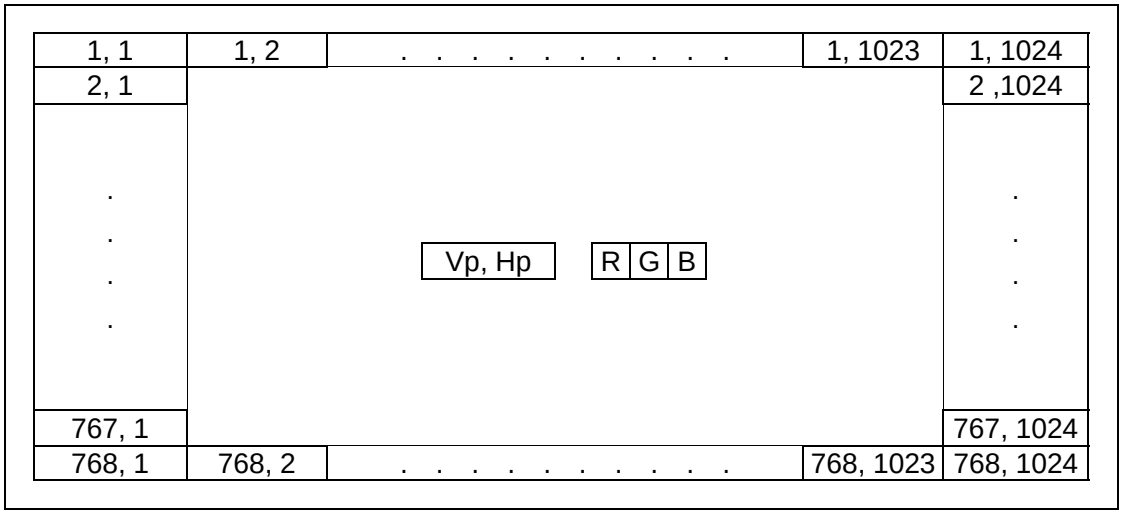


RELATIONSHIP BETWEEN INPUT DATA AND DISPLAY COLOR

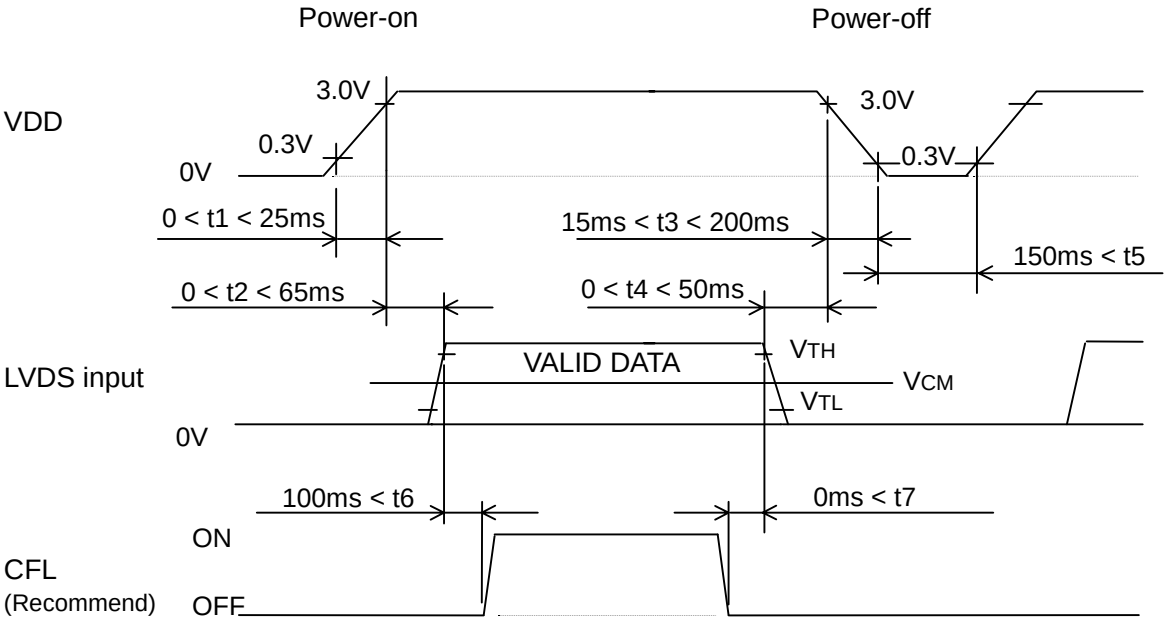
INPUT DATA / DISPLAY COLOR		RED DATA						GREEN DATA						BLUE DATA					
		MSB					LSB	MSB					LSB	MSB					LSB
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
BASIC COLOR	BLACK	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	RED(63)	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L
	GREEN(63)	L	L	L	L	L	L	H	H	H	H	H	H	L	L	L	L	L	L
	BLUE(63)	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H
	CYAN	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H
	MAGENTA	H	H	H	H	H	H	L	L	L	L	L	L	H	H	H	H	H	H
	YELLOW	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L
	WHITE	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
RED	BLACK	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	RED(1)	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
	RED(2)	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
	:	:						:						:					
	:	:						:						:					
	RED(61)	H	H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L
	RED(62)	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
	RED(63)	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L
GREEN	BLACK	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	GREEN(1)	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
	GREEN(2)	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
	:	:						:						:					
	:	:						:						:					
	GREEN(61)	L	L	L	L	L	L	H	H	H	H	L	H	L	L	L	L	L	L
	GREEN(62)	L	L	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L
	GREEN(63)	L	L	L	L	L	L	H	H	H	H	H	H	L	L	L	L	L	L
BLUE	BLACK	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	BLUE(1)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
	BLUE(2)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
	:	:						:						:					
	:	:						:						:					
	BLUE(61)	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H
	BLUE(62)	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L
	BLUE(63)	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H

[Note 1] Color(n) --- 'n' indicates gray scale step.

RELATIONSHIP BETWEEN INPUT DATA AND DISPLAY POSITION



POWER ON/OFF SEQUENCE REQUIREMENT



When the power is off, LVDS input must be kept at either low level or high impedance.

Power sequence for CFL (backlight) is not specified especially, however it is recommended to consider some timing difference between LVDS input as shown above.

If backlight lights on before LCD starts function, or if backlight is kept on after LCD stopped function, screen may look white for a moment or abnormal image may be displayed.

This is caused by variation in output signal from timing generator at LVDS input on or off. It does not cause damage to liquid crystal molecule and driving circuit.

PRECAUTIONS (INSTRUCTIONS FOR SAFE AND PROPER USE)

1. Instructions for safety

(1) Please do not disassemble or modify LCD module to avoid the possibility of electric shock, damage of electronic components, scratch at display surface and invasion of foreign particles. In addition, such activity may result in fire accident due to burning of electronic component.
LCD module disassembled or modified by customer is out of warranty.

(2) Please be careful in handling of LCD module with broken glass.
When the display glass breaks, please pay attention not to injure your fingers. The display surface has the plastic film attached, which prevents dispersion of glass pieces, however touching broken edge will injure your fingers. Also CFL (Cold Cathode Fluorescent Lamp) is made of glass, therefore please pay attention in the same way.

(3) Please do not touch the fluid flown out of broken display glass.
If the fluid should stick to hand or clothes, wipe off with soap or alcohol immediately and then wash it with water. If the fluid should get in eyes, wash eyes immediately with washing lotion for more than 15 minutes and then consult the doctor.

(4) Please make secure connection of CFL connector.
Please make sure that CFL connector from LCD module is connected with output connector on inverter circuit securely. Poor connection may cause smoke or fire accident due to high voltage in circuit. If connection may not be secure, please switch off the power supply for LCD module and CFL and then make secure connection.
Please do not make connection with another connector than recommended mating connector.

(5) CFL contains mercury inside. Please follow regulations or rules established by local autonomy at its disposal.

(6) Please be careful to electric shock.
Before handling LCD module, please switch off the power supply.
Since high voltage is applied to CFL terminal, cable, connector and inverter circuit in operation mode, touching them will cause electric shock.

2. Instructions for designing

(1) Mounting of LCD
Please fix LCD module at all mounting flanges shown in this specification for installation onto system. The used screws should have proper dimensions.
Furthermore, designing of mounting parts should be adequate so that LCD module is not putted stresses (ex. warped, twisted and pressed stress), to achieve good display quality. The stresses may cause non-uniformity even if there is no non-uniformity statically.

(2) Polarity of power supply for CFL
Please give careful consideration in designing so that each polar of cable should be connected correctly at assembling (i.e. high voltage side is connected to high voltage side and low voltage side is connected to low voltage side). Since longer CFL cable may cause insatiable start-up of CFL and reduction of brightness, please make cable short as much as possible.

(3) Designing of power supply circuit for CFL
Please design the circuit so that high voltage output can be kept for more than 1 second. The shorter time may not start up CFL. The driving inverter circuit is recommended to be the type which CFL current can be controlled.
The type which voltage is controlled is not recommended, because it may cause big current under high temperature and insatiable start-up of CFL under low temperature.

(4) Heat radiation
CFL generates heat at lighting and causes temperature rise inside system. Therefore, designing to radiate heat like radiation slits at cabinet is recommended to meet the specified operating temperature range for LCD module.

(5) Noise on power line
Spike noise contained in power line causes abnormal operation of driving circuit and abnormal display. To avoid it, spike noise should be suppressed below VDD +/- 200mVp-p. (In any case, absolute maximum rating should be kept.)

(6) Power sequence
Before LCD module is switched on, please make sure that power supply and input signals of system, testing equipment, etc. meet the recommended power sequence.

(7) Absolute maximum rating
Absolute maximum rating specified in this specification has to be kept in any case. It shows the maximum that cannot be exceeded.
Exceeding it may cause burning or non-recoverable break of electronic components in circuit. Please make system design so that absolute maximum rating is not exceeded even if ambient temperature, input signal and components are varied.

(8) Protection for power supply
Please study to adapt protection for power supply against trouble of LCD module, depending on usage condition of system. Fuse installed on LCD module should be never modified. Any modification to make the function of fuse ineffective may cause burning or break of printed wiring board or other components at circuit trouble.

(9) Protection against electric shock
High voltage is applied to CFL connector, inverter circuit and CFL at lighting. Please make design not to expose or be accessible to such high voltage parts to avoid electric shock.

(10) Protection cover and cut-off filter for ultraviolet rays
When LCD module is used under severe condition like outdoor, it is recommended to use transparent protection cover over display surface to avoid scratches and invasion of dust and water. In addition, when LCD module is exposed to direct sun light for long time, use of cut-off filter for ultraviolet rays is also recommended. Please be careful not to get condensation.

3. Instructions for use and handling

(1) Protection against Static electricity
C-MOS LSI and semiconductors are easily damaged by static discharge. LCD module should be handled on conductive mat by person grounded with wrist strap etc. to avoid getting static electricity. Please be careful not to generate static electricity during operation.

(2) Protection against dust and stain
LCD module should be handled in circumstance as clean as possible.
It is recommended to wear fingerstalls or ductless and soft gloves before handling to avoid getting dust or stain on display surface.

(3) Protection film for display surface
It is recommended to remove protection film at nearly final process of assembling to avoid getting scratch or dust. To remove film, please pick up its edge with dull-head tweezers or cellophane tape at first and then remove film gradually taking more than 3 seconds. If film is removed quickly, static electricity may be generated and may damage semiconductors or electronic components.

(4) Contamination of display surface
When display surface of LCD module is contaminated, please wipe the surface softly with cotton swab or clean cloth. If it is not enough, please take it away with cellophane tape or wipe the surface with cotton swab or clean cloth containing benzine. In this case, please be careful so that benzine does not get in inside of LCD module, because it may be damaged.

(5) Water drop on LCD surface
Please do not leave LCD module with water drop. When the display surface gets water drop, please wipe it off with cotton swab or soft cloth immediately, otherwise display surface will be deteriorated.
If water gets in inside of LCD module, circuit may be damaged.

(6) Please make sure that LCD module is not warped or twisted at installation into system. Even temporary warp or twist may be the cause for failure.

(7) Mechanical stress
Please be careful not to apply strong mechanical stress like drop or shock to LCD module. Such stress may cause break of display glass and CFL or may be the cause for failure.

(8) Pressure to display surface
Please be careful not to apply strong pressure to display surface. Such pressure may cause scratches at surface or may be the cause of failure.

(9) Protection against scratch
Please be careful not to hit, press or rub the display surface with hard material like tools. In addition, please do not put heavy or hard material on display surface, and do not stack LCD modules. Polarizer at front surface can be easily scratched.

(10) Plugging in of connector
Please be careful not to apply strong stress to connector part of LCD module at plugging in or out, because strong stress may damage the inside connection. At plugging in connector, place LCD module on the flat surface and hold the backside of connector on LCD module. Please make sure that connector is plugged in correctly. Insecure connection may be the cause for failure during operation.
In addition, please be careful not to put the connecting cable between cabinet of system and LCD module at installing LCD module into system.

(11) Handling of CFL cable and FPC (Flexible Printed Circuit)
Please be careful not to pull or scratch CFL cable, because CFL or soldered part of cable may be damaged consequently.
Also FPC should not be pulled or scratched.

(12) Switching off before plugging in connector
Please make sure that power is switched off before plugging in connector.
If power is on at plugging in or out, circuit of LCD module may be damaged.
When LCD is switched on for test or inspection, please make sure that power supply and input signals of driving system meet the specified power sequence.

(13) Temperature dependence of LCD display
Response speed (optical response) of LCD display is dependent on temperature. Under low temperature, response speed is slower.
Also brightness and chromaticity change slightly depending on temperature.

(14) Slow light-up and life time of CFL under low temperature
Under low temperature, start-up of CFL gets difficult. (The time from switch-on to stable lighting becomes longer.)
As characteristic of CFL, operation under low temperature makes the life time shorter. To avoid this, it is recommended to operate under normal temperature.

(15) Condensation
LCD module may get condensation on its display surface and inside in the circumstance where temperature changes much in short time.
Condensation can cause deterioration or failure. Therefore, please be careful not to get condensation.

(16) Remaining of image
Displaying the same pattern for long time may cause remaining of image even after changing the pattern. This is not failure but will disappear with time.

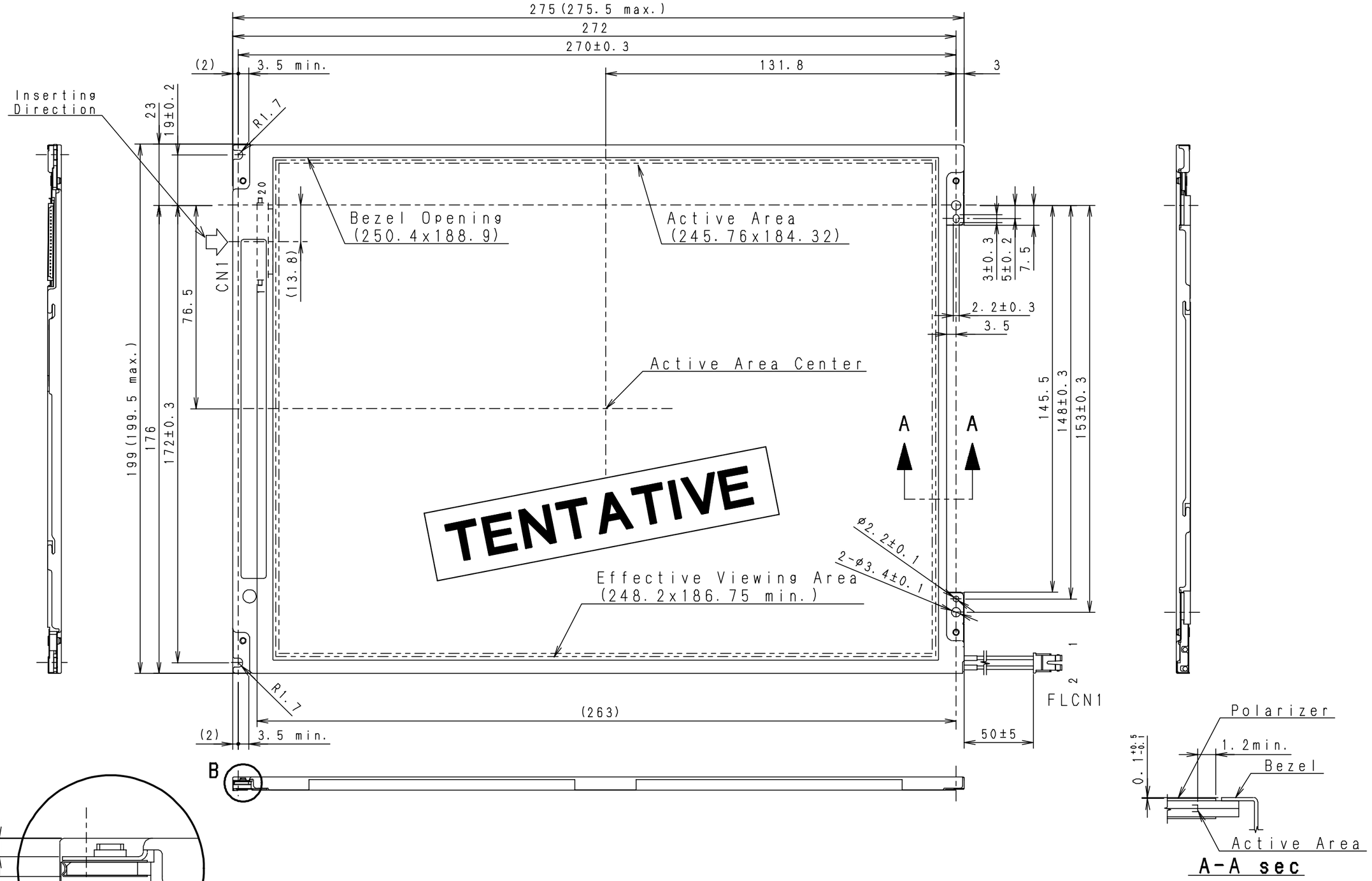
4. Instructions for storage and transportation

(1) Storage
Please store LCD module in the dark place of room temperature and low humidity in original packing condition, to avoid condensation that may cause failure.
Since sudden temperature change may cause condensation, please store in circumstance of stable temperature.

(2) Stacking number
Since excessive weight causes deformation and damage of carton box, please stack only up to the number stated on carton box for storage and transportation.

(3) Handling
Since LCD module consists of glass and precise electronic components, it will be damaged by excessive shock and drop. Therefore, please handle the carton box carefully to minimize shock at loading, reloading and transportation.

Outer Dimensions



CN1 :FI-SEB20P-HF10(JAE)
FLCN1:BHSR-02VS-1(JST)

Note1:All dimensional tolerance unless otherwise specified ±0.5
2:※--This value shows the thickness after mounting and fixing to customer's cabinet.

Unit:mm