

# PH2920

N-channel enhancement mode field-effect transistor

Rev. 01 — 13 June 2003

Product data

## 1. Product profile

### 1.1 Description

N-channel enhancement mode field-effect power transistor in a SOT669 (LFAK) package.

Product availability:

PH2920 in SOT669 (LFAK).

### 1.2 Features

- Low thermal resistance
- Low gate drive current
- SO8 equivalent area footprint
- Low on-state resistance.

### 1.3 Applications

- DC-to-DC converters
- Portable appliances
- Switched mode power supplies
- Notebook computers.

### 1.4 Quick reference data

- $V_{DS} \leq 20 \text{ V}$
- $P_{tot} \leq 62.5 \text{ W}$
- $I_D \leq 60 \text{ A}$
- $R_{DS(on)} \leq 2.9 \text{ m}\Omega$

## 2. Pinning information

Table 1: Pinning - SOT669 (LFAK), simplified outline and symbol

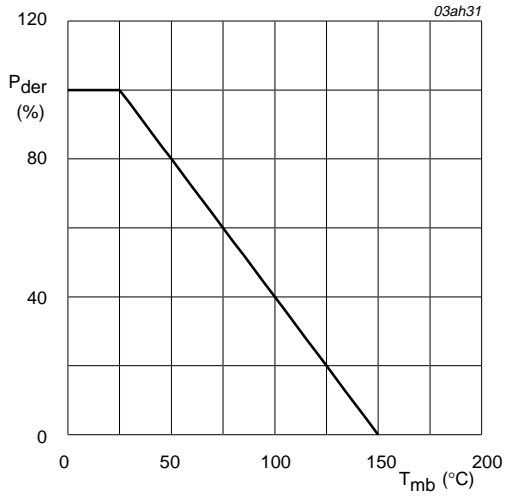
Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p style="text-align: center;">SOT669 (LFAK)</p>	
4	gate (g)		
mb	drain (d)		

### 3. Limiting values

**Table 2: Limiting values**

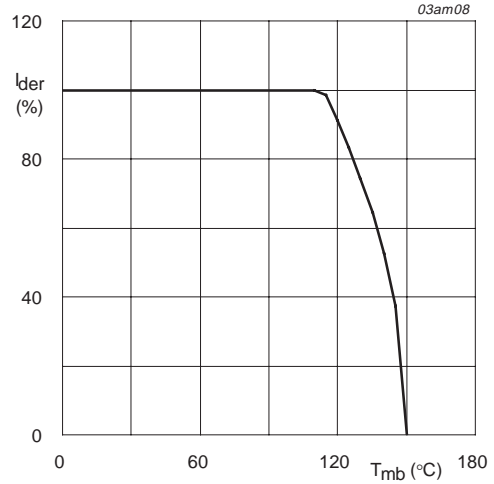
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$T_j = 25$ to $150$ °C	-	20	V
$V_{GS}$	gate-source voltage (DC)		-	$\pm 20$	V
$I_D$	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; <b>Figure 2 and 3</b>	-	60	A
$I_{DM}$	peak drain current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ $\mu$ s; <b>Figure 3</b>	-	240	A
$P_{tot}$	total power dissipation	$T_{mb} = 25$ °C; <b>Figure 1</b>	-	62.5	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	junction temperature		-55	+150	°C
<b>Source-drain diode</b>					
$I_S$	source (diode forward) current (DC)	$T_{mb} = 25$ °C	-	60	A
$I_{SM}$	peak source (diode forward) current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ $\mu$ s	-	240	A



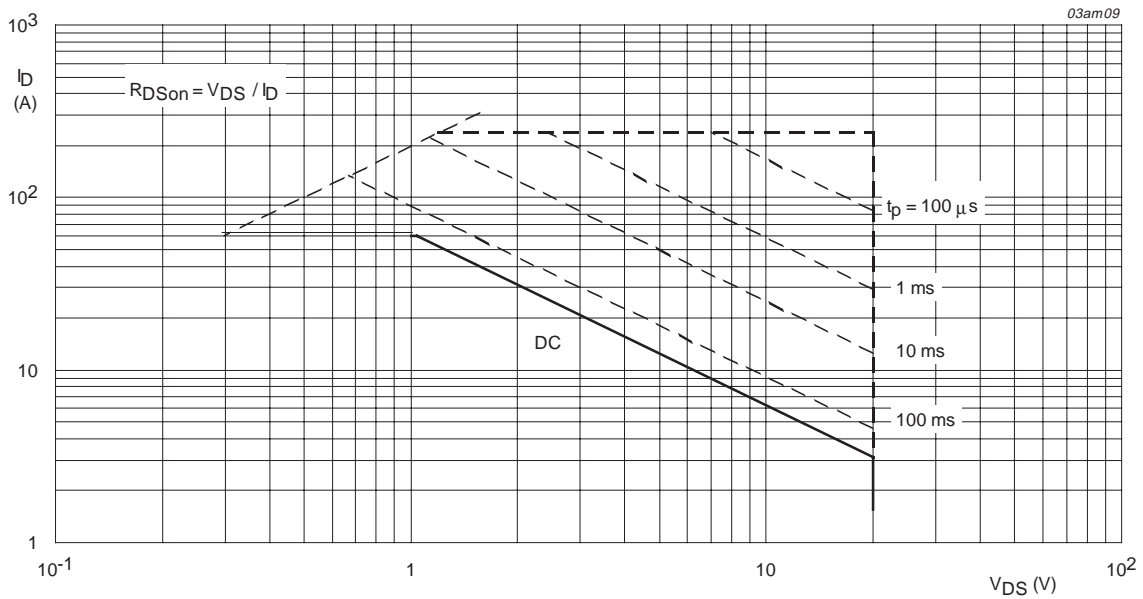
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

## 4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	2	K/W

### 4.1 Transient thermal impedance

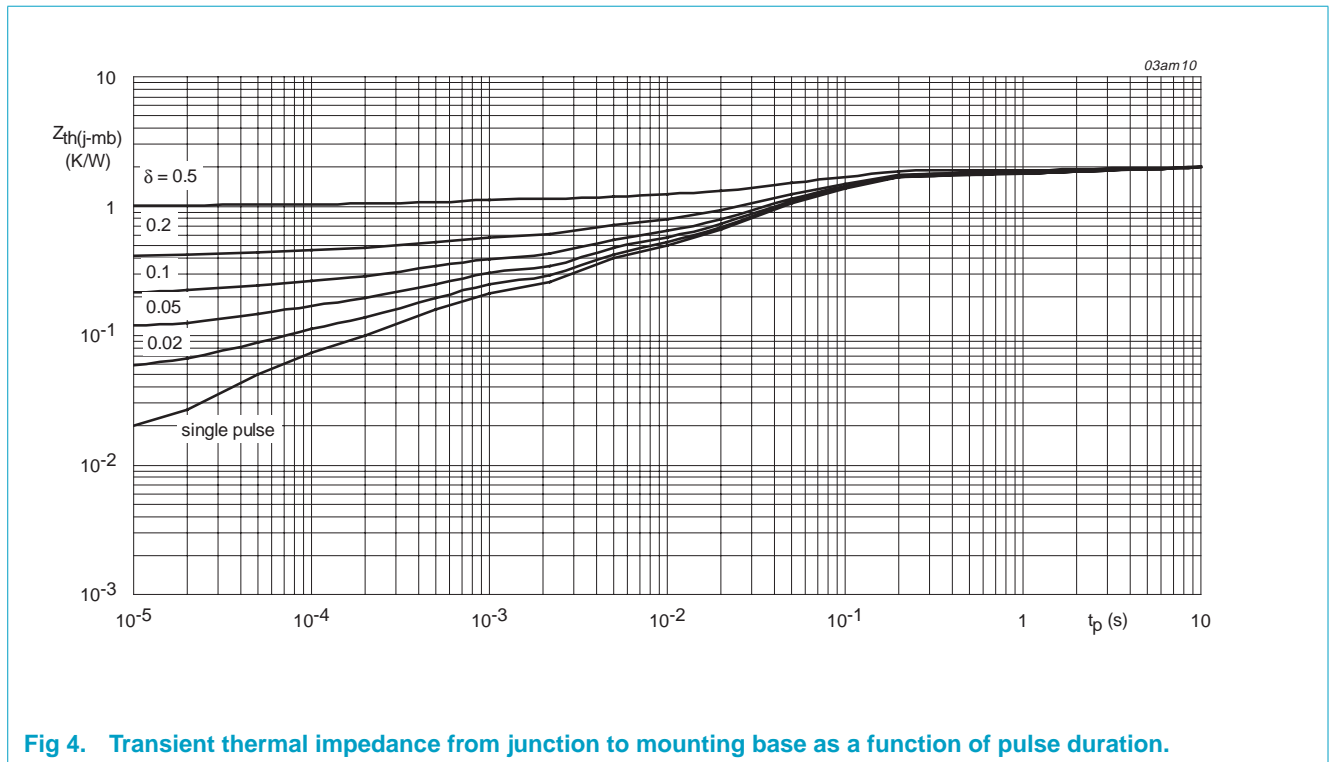
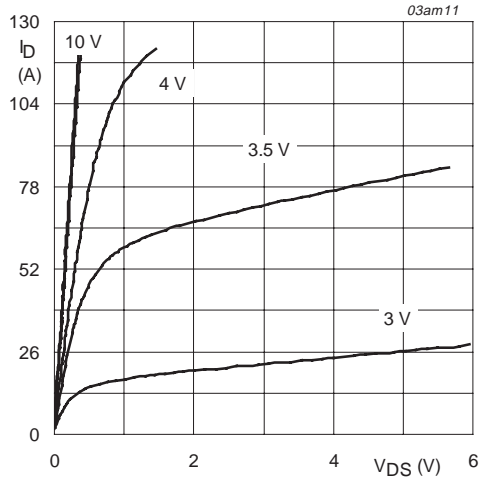


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

## 5. Characteristics

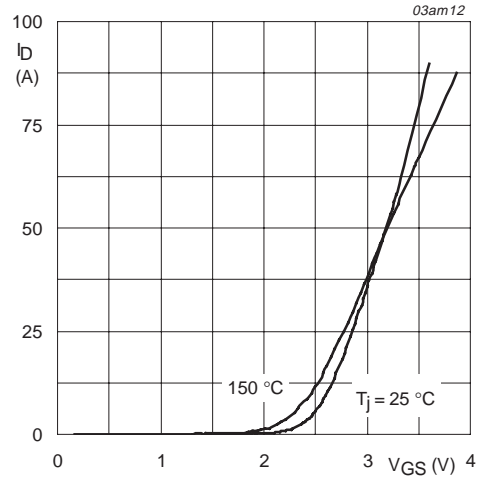
**Table 4: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 10 mA; V <sub>GS</sub> = 0 V	20	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; <b>Figure 9</b>	1	1.75	2.5	V
I <sub>DSS</sub>	drain-source leakage current	V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.06	1	μA
I <sub>GSS</sub>	gate-source leakage current	V <sub>GS</sub> = ± 16 V; V <sub>DS</sub> = 0 V	-	-	10	μA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 30 A; <b>Figure 7 and 8</b>	-	2.6	2.9	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 30 A	-	4.3	5.8	mΩ
<b>Dynamic characteristics</b>						
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 30 A	45	75	-	S
Q <sub>g(tot)</sub>	total gate charge	I <sub>D</sub> = 60 A; V <sub>DD</sub> = 10 V; V <sub>GS</sub> = 10 V; <b>Figure 13</b>	-	60	-	nC
Q <sub>gs</sub>	gate-source charge		-	15	-	nC
Q <sub>gd</sub>	gate-drain (Miller) charge		-	11	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 10 V; f = 1 MHz; <b>Figure 11</b>	-	4200	-	pF
C <sub>oss</sub>	output capacitance		-	1200	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	650	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DD</sub> = 10 V; I <sub>D</sub> = 30 A; V <sub>GS</sub> = 10 V; R <sub>G</sub> = 4.7 Ω	-	20	-	ns
t <sub>r</sub>	rise time		-	85	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	95	-	ns
t <sub>f</sub>	fall time		-	20	-	ns
<b>Source-drain (reverse) diode</b>						
V <sub>SD</sub>	source-drain (diode forward) voltage	I <sub>S</sub> = 60 A; V <sub>GS</sub> = 0 V; <b>Figure 12</b>	-	0.85	1.1	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 60 A; dI <sub>S</sub> /dt = -50 A/μs; V <sub>GS</sub> = 0 V	-	50	-	ns



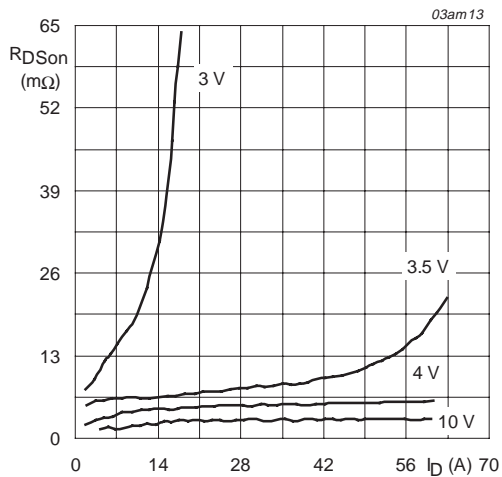
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



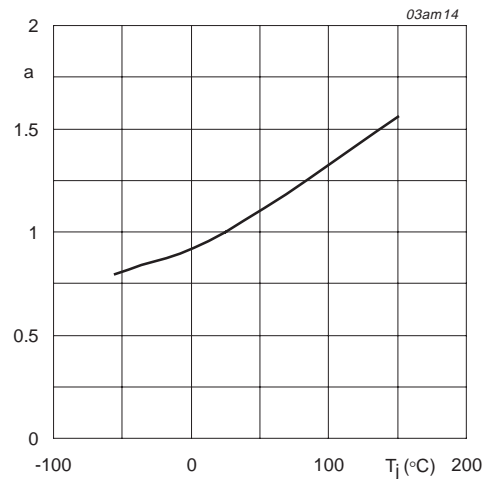
$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



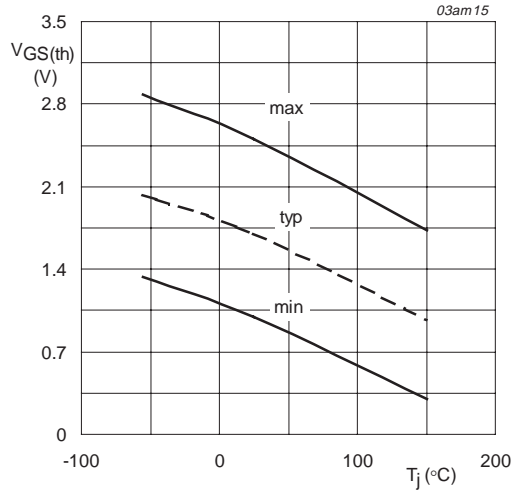
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



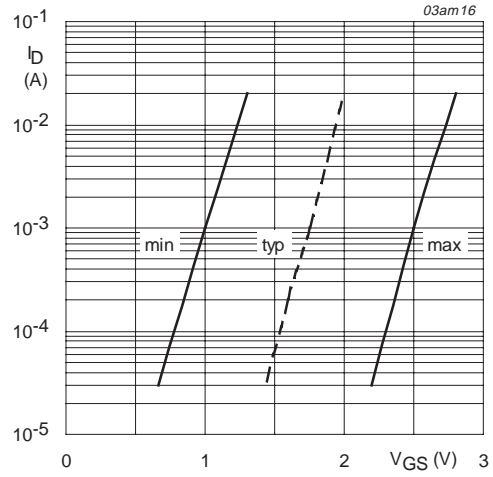
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



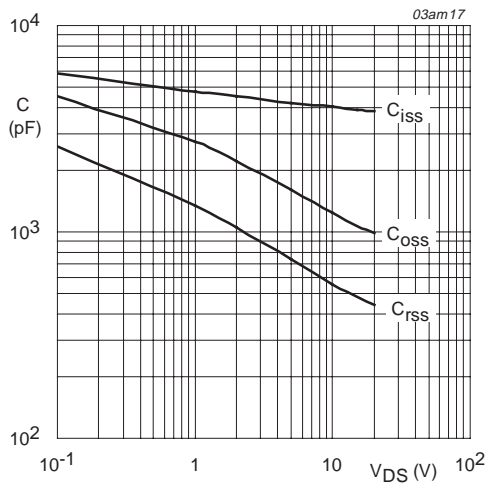
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



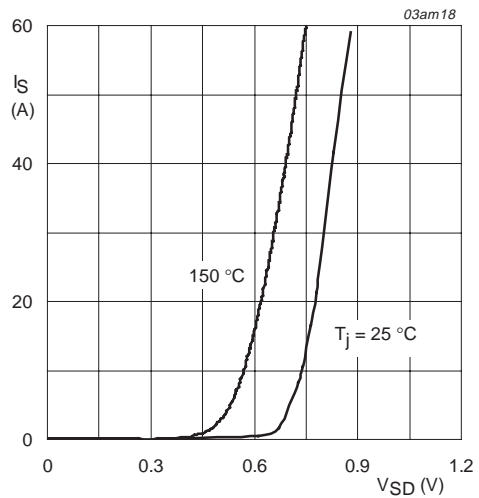
$T_j = 25 \text{ }^{\circ}C$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



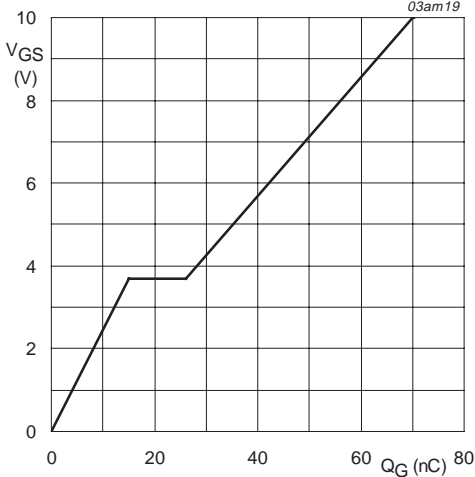
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25 \text{ }^{\circ}C$  and  $150 \text{ }^{\circ}C; V_{GS} = 0 \text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$ ;  $I_D = 60\text{ A}$ ;  $V_{DD} = 10\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.



6. Package outline

Plastic single-ended surface mounted package (Philips version LPAK); 4 leads

SOT669

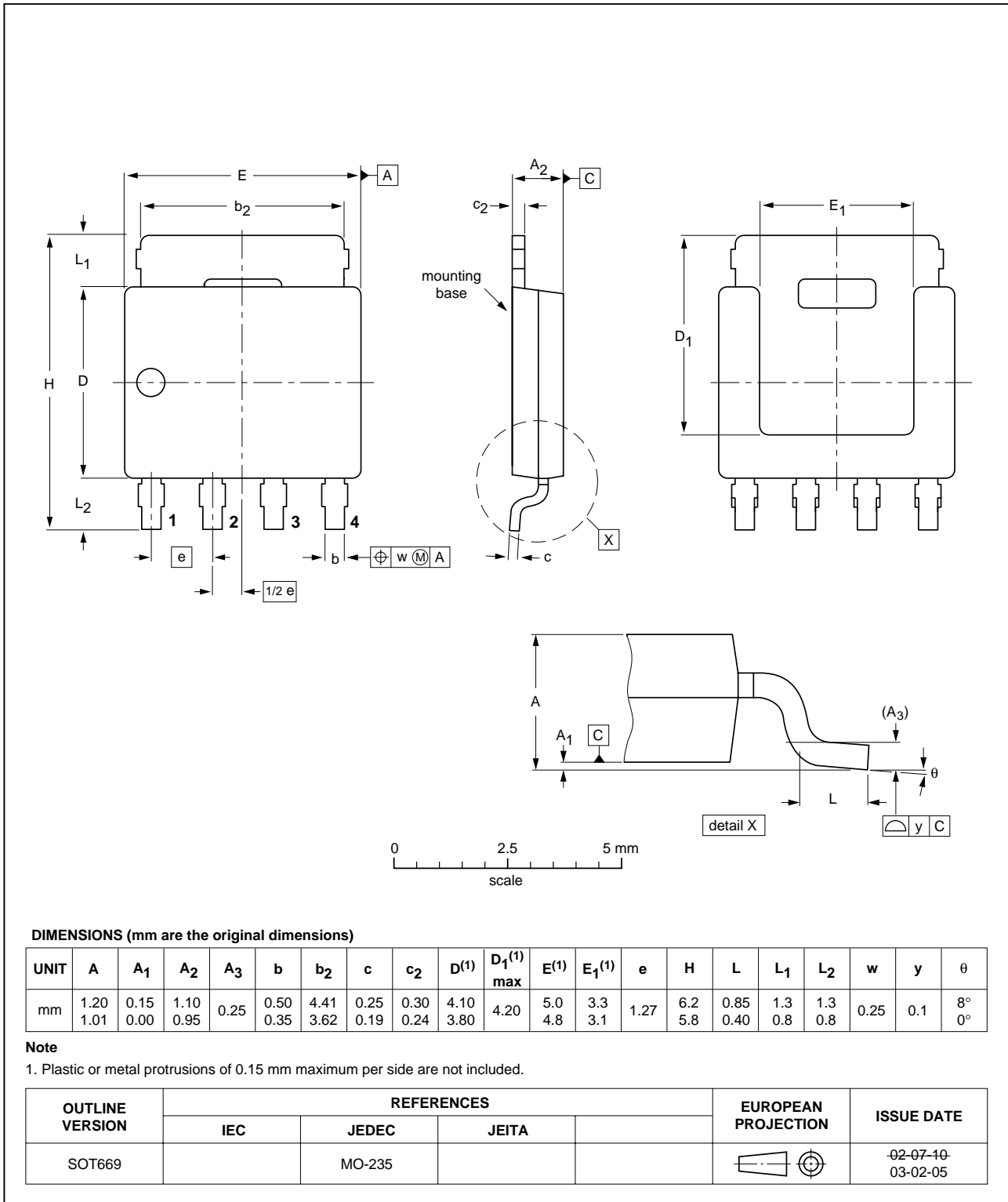


Fig 14. SOT669 (LPAK).

## 7. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
01	20030613		Product data (9397 750 11119)

## 8. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2][3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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