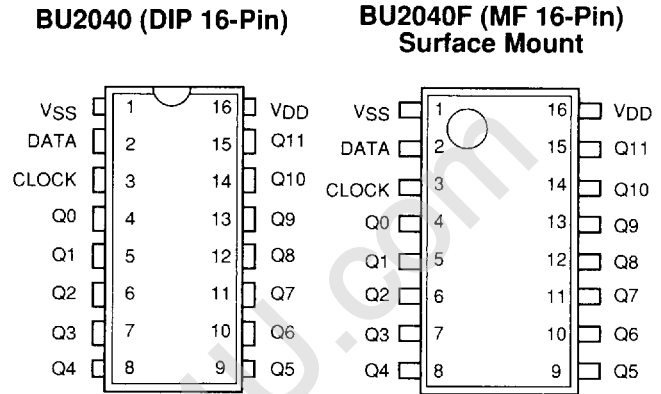


FEATURES

- 12-bit Serial/Parallel Conversion
- Low Quiescent Current Due To CMOS Configuration
- Output Open Drain
- $I_{SINK} = 20mA$
- Default High-Z On At Power Up
- No External Latching Required

PIN CONFIGURATION

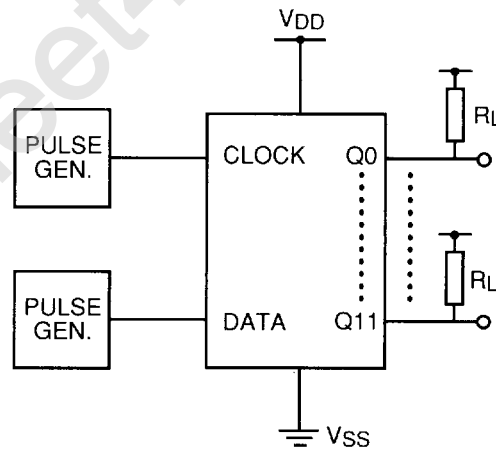


APPLICATIONS

- Microprocessor port expansion
- Serial/Parallel conversion
- Computer peripheral

DESCRIPTION

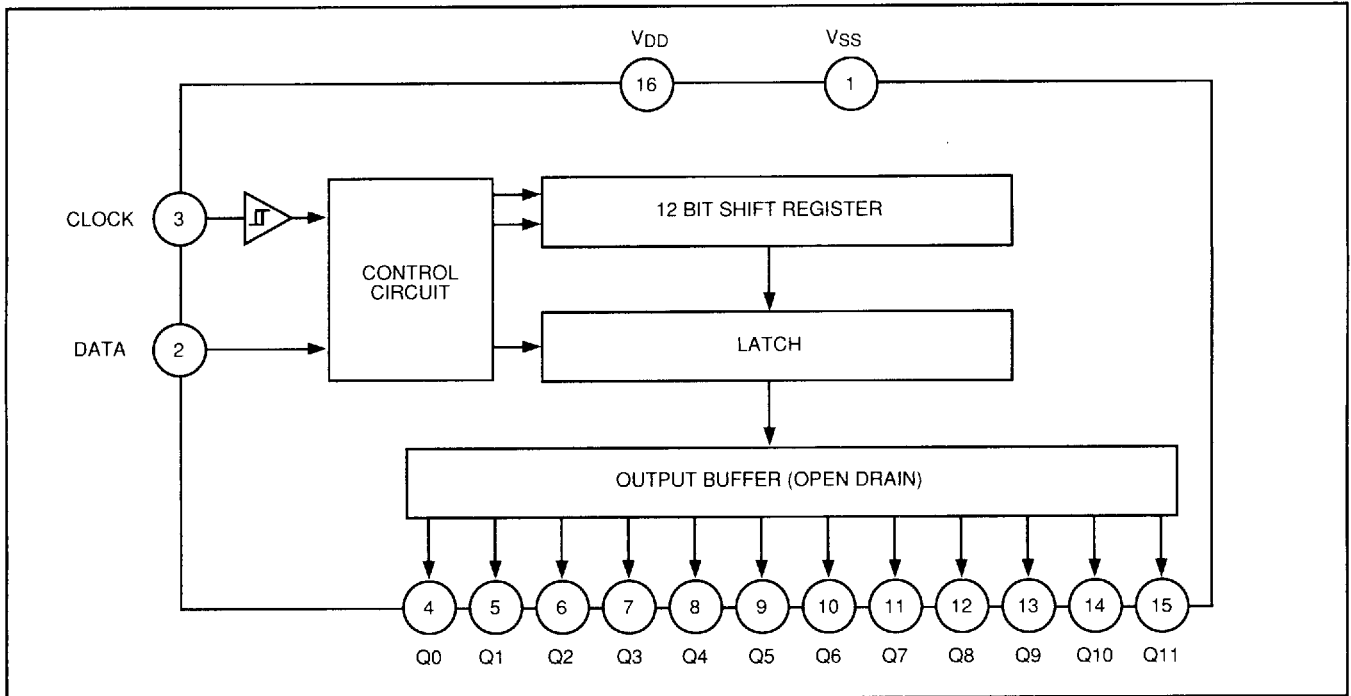
The BU2040 is a 12-bit serial/parallel converter which can be used to expand the input or output capability of a microcontroller or microprocessor. It has the particular benefit that latching is derived from the clock and data inputs and does not require a separate input.



PIN NAMES

VSS	Steady State Voltage
DATA	Serial DATA Input
CLOCK	Clock Input
Q0-Q11	Outputs
VDD	Supply Voltage

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

$T_A = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	-0.3 to +7.0	V
P_d	Power Dissipation	1100(DIP)/500(MF)	mW
T_{opr}	Operating Temperature Range	-25 to +75	$^\circ\text{C}$
T_{stg}	Storage Temperature Range	-55 to +125	$^\circ\text{C}$
V_{IN}	Input Voltage	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
V_O	Output Voltage	V_{SS} to 7.0	V
I_O	DC Output Current	20	mA

Notes:

1. Absolute Maximum Ratings are values below which the device will not sustain damage and does not guarantee operation.
2. Power dissipation is done at 11mW/ $^\circ\text{C}$ for operation above $T_A = 25^\circ\text{C}$.

RECOMMENDED OPERATING CONDITIONS

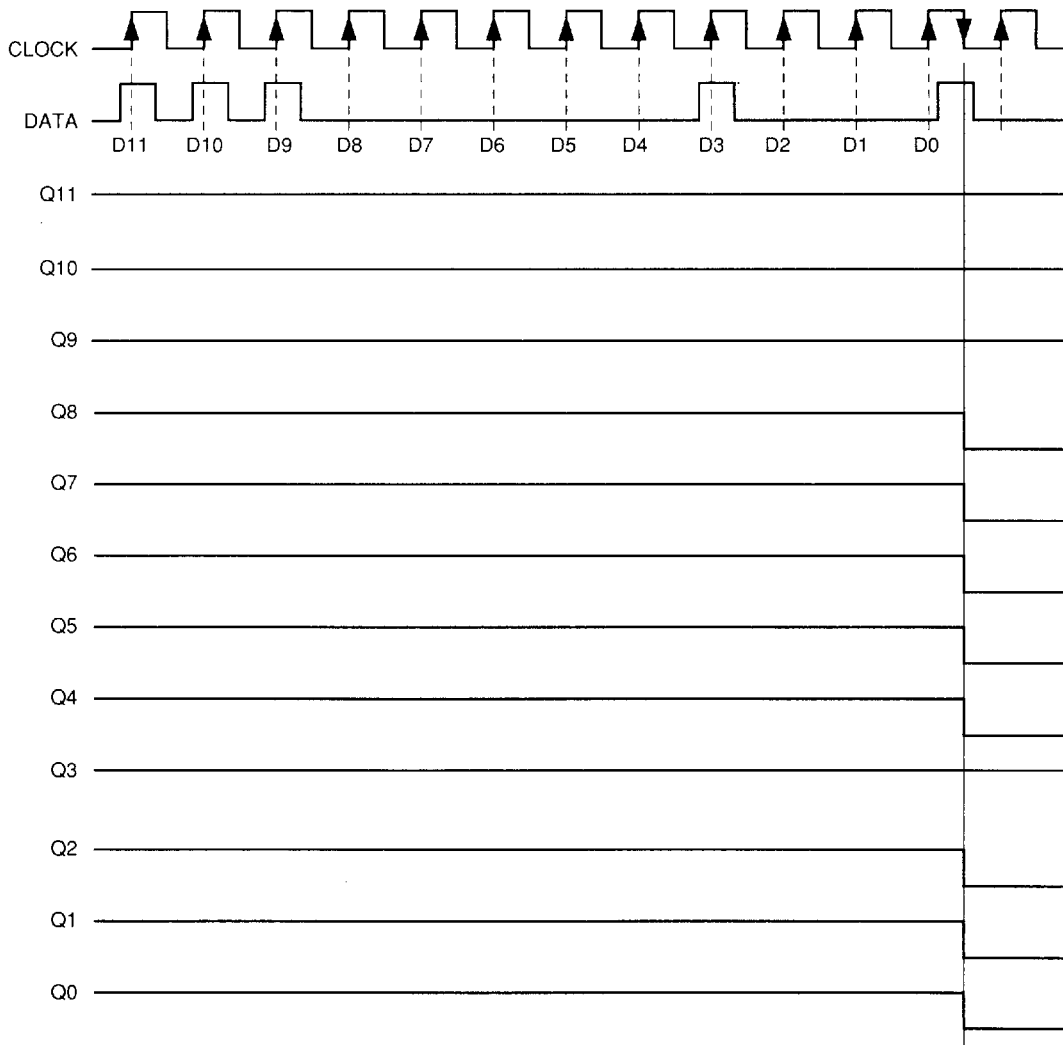
$T_A = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input Voltage (High Level)	$0.7 \times V_{DD}$	V_{DD}	V_{DD}	V
V_{IL}	Input Voltage (Low Level)	0	0	$0.3 \times V_{DD}$	V

ELECTRICAL CHARACTERISTICS

TA = 25°C, VDD = 5V, VSS = 0V

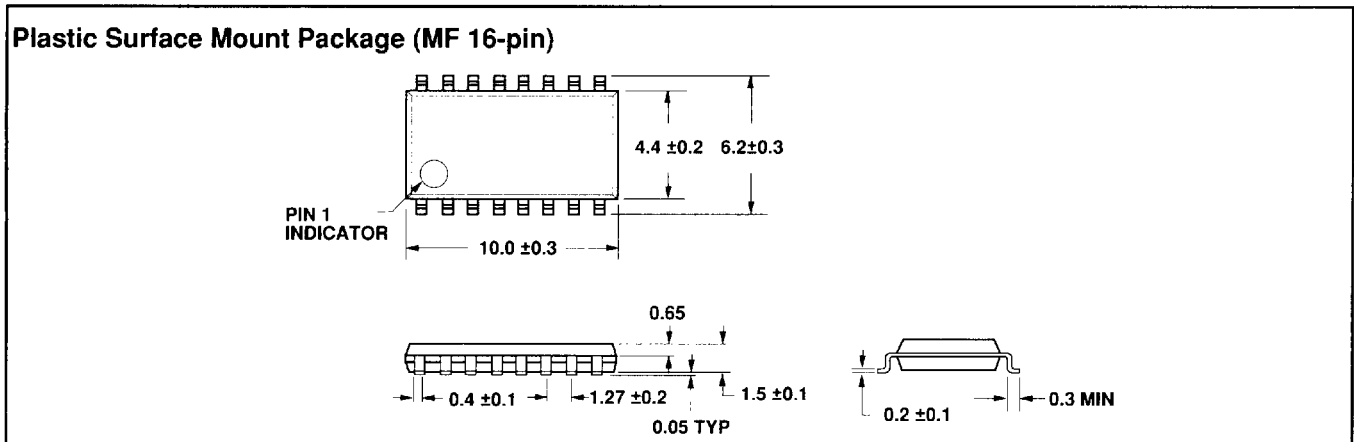
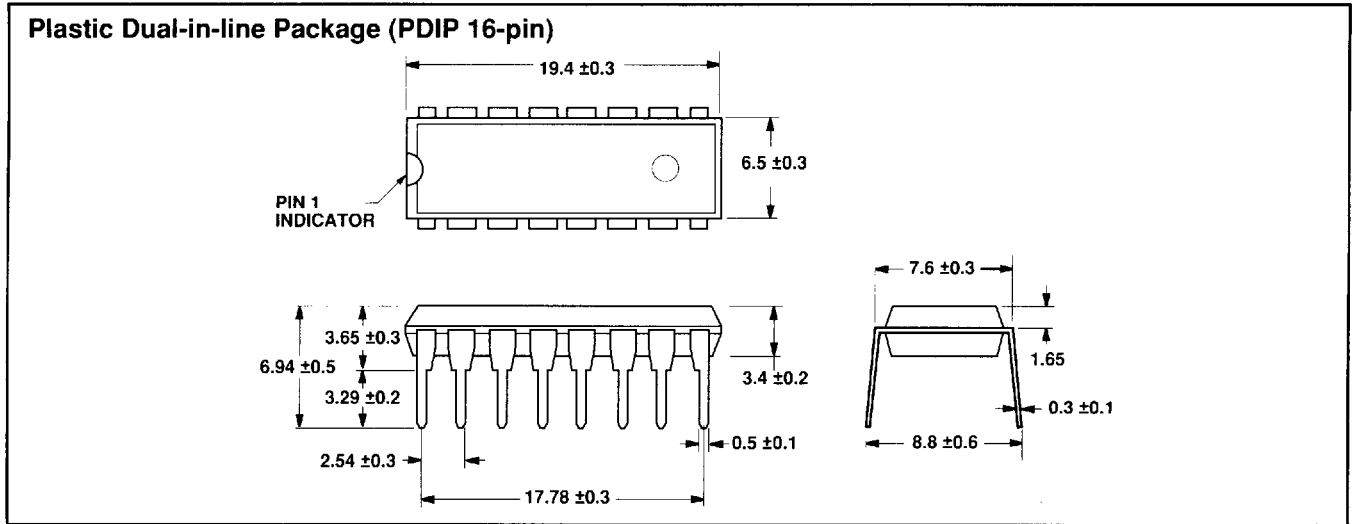
Symbol	Parameter	BU2040/BU2040F			Unit	Test Conditions
		Min.	Typ.	Max.		
VOL	Output Voltage (Low Level)	—	—	2	V	IOL = 20mA
IOZH	Output Disable Current (High Level)	—	—	7	μA	VO = 7.0V
IOZL	Output Disable Current (Low Level)	—	—	-5	μA	VO = 0V
IDD	Quiescent Supply Current	—	—	5	μA	VIN = VSS or VDD
tw	Minimum Clock Pulse Width	500	—	—	ns	



NOTE: If the data is 'high' as the clock pulse falls, the contents of the shift register is transferred to the latch circuit.

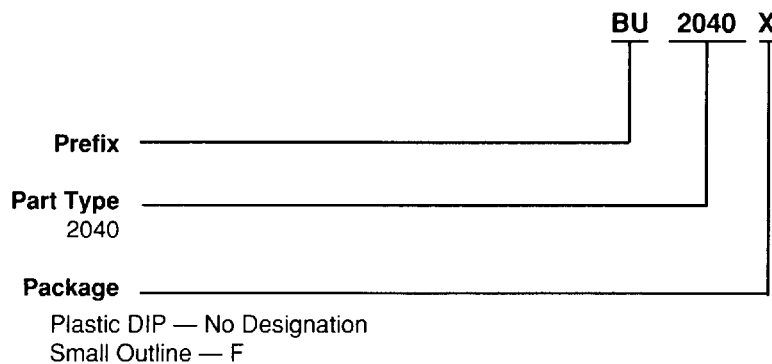
FIGURE 1. TIMING DIAGRAM

PACKAGE DIAGRAMS



ORDERING INFORMATION

Part Numbers:



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