Audio Processor for Video Recorders and Satellite Receivers

Note:
If not otherwise designated, the pin numbers mentioned refer to the 24–pin DIL package.

1. Introduction

The AMU 2481 VS Audio Processor is a digital real–time signal processor in NMOS technology, housed in a 24–pin Dil plastic package or in a 44–pin PLCC package. It is designed to perform digital processing of both TV audio information and digital audio data supplied by the MSP 2410 Multistandard Sound Processor or the DMA 2271 D2–MAC Decoder. The architecture of the AMU 2481 VS combines two main blocks:

– I/O blocks

– DSP block

The I/O blocks are used to manage the input and output of audio information. The DSP block consists of a mask–programmable digital signal processor, whose software can be controlled by a microprocessor (CCU) via the IM bus. So parameters like coefficients can be modified during performance. By means of the DSP software, audio functions, such as deemphasis, oversampling mixing and volume control are performed. Fig. 1–1 gives an overview over the AMU's functions.

1.1. Application of the AMU 2481 VS

The AMU 2481 VS Audio Processor is designed to interface with ITT's ADC 2311 E Audio A/D Converter, MSP 2410 Multistandard Sound Processor, DMA 2271 D2–MAC Decoder on the input side, and with the APU 2471 or the ACP 2371 Audio Processors on the output side. It can receive digital audio data in two different formats:

Via the PDM inputs, the AMU 2481 VS is supplied with two 1–bit PDM data streams produced by the ADC 2311 E Audio A/D Converter which receives analog audio information either from the SCART interface (Euro connector), which is used, e.g., for video recorder connection, or from any terrestrial TV transmission. For this input format, decimation filters are provided in the AMU 2481 VS, which convert each PDM stream into a 16–bit word at a sampling rate of 32 kHz.

Via the SBUS interface the AMU 2481 VS receives serial audio data, provided, e.g., by the MSP 2410 Multistandard Sound Processor or by the DMA 2271 D2–MAC Decoder.

Fig. 1–2 shows how the AMU 2481 VS can be used together with the mentioned ICs of ITT to realize multistandard audio processing with PAL and D2–MAC or NICAM signals. In the following descriptions data coming from the ADC will be called "PDM data" and data coming from the DMA or MSP will be called "S data".

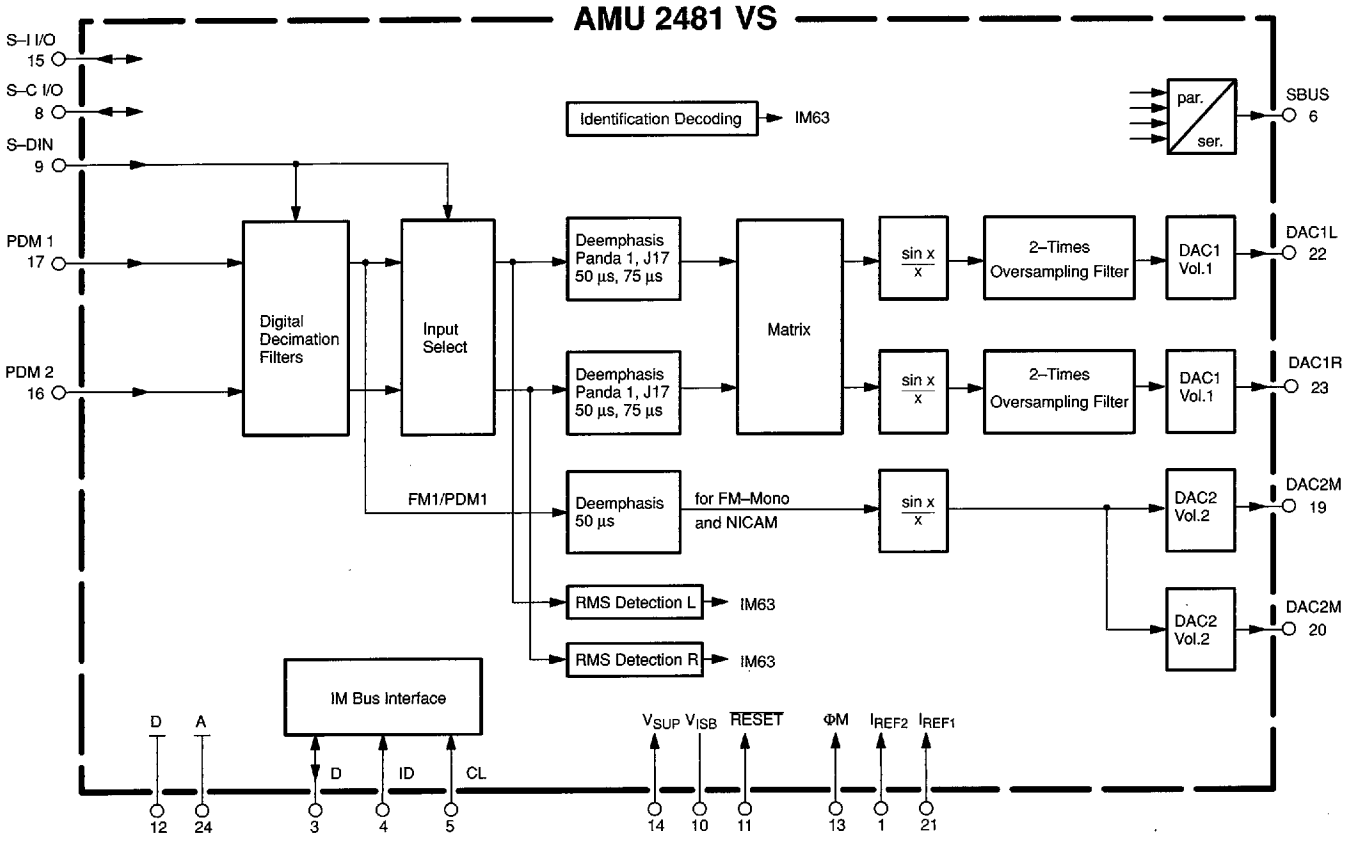


Fig. 1–1: Functional block diagram of the AMU 2481 VS

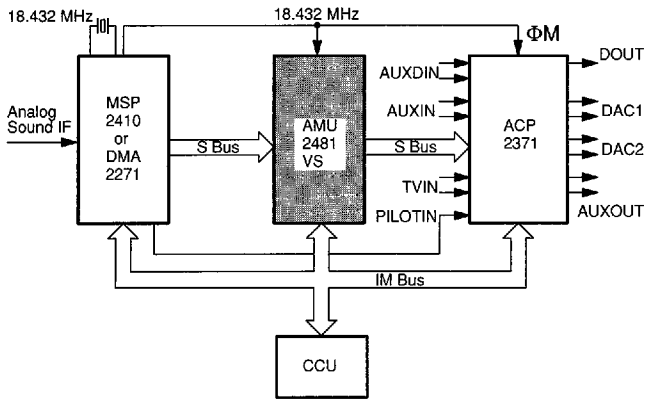


Fig. 1–2: Multistandard audio system with AMU 2481 VS

1.2. Architecture of the AMU 2481 VS and Functional Description

As already mentioned in section 1., the AMU 2481 VS architecture combines two main parts, the I/O blocks and the DSP core. Fig. 1–3 shows a block diagram of the architecture.

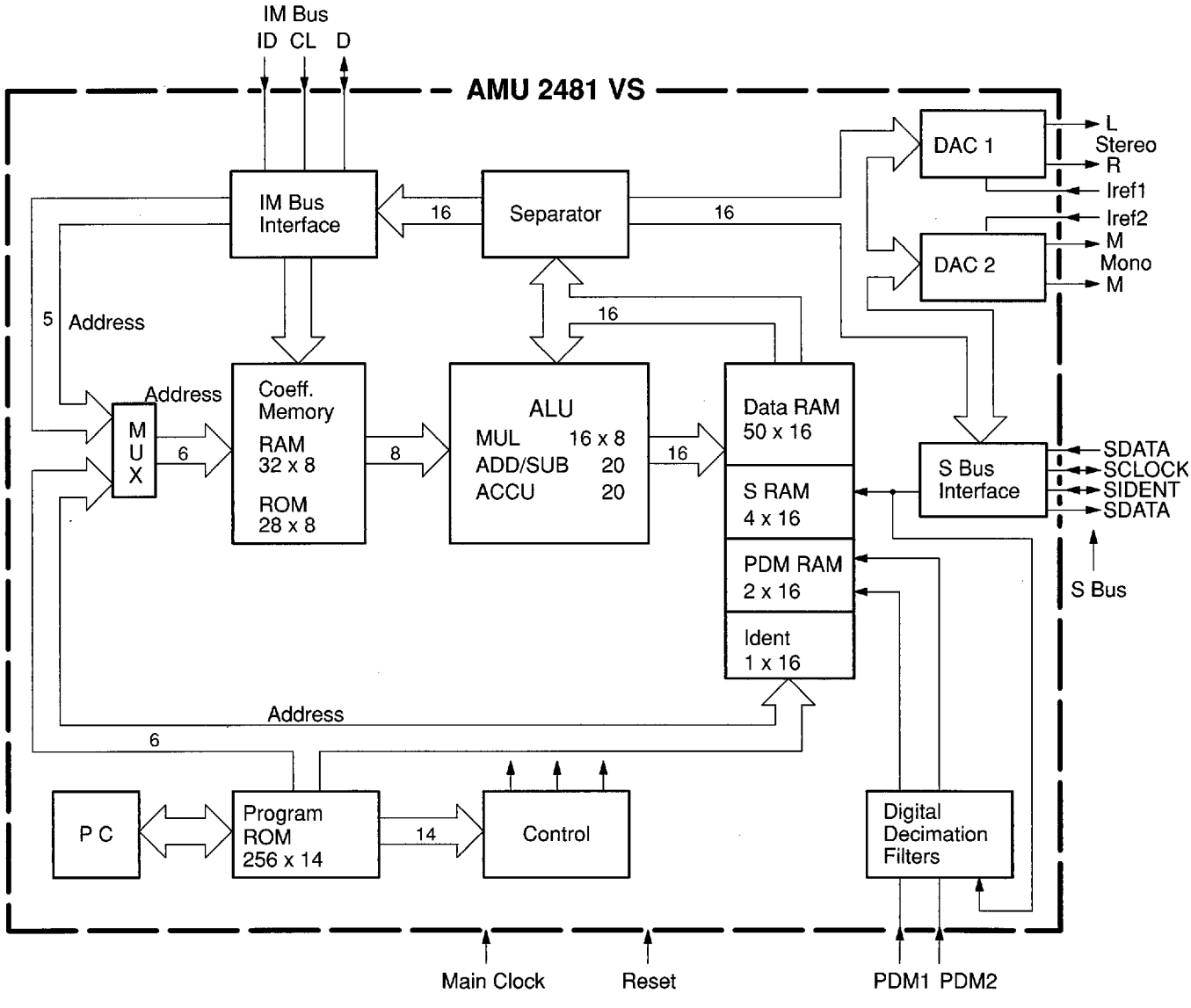


Fig. 1–3: AMU 2481 VS Architecture

2. I/O Blocks

2.1. Digital Decimation Filters

The digital decimation filters are cascades of transversal and recursive lowpass filters. They are required to convert the two 1–bit PDM data streams by stepwise reduction of bandwidth and word rate (sampling rate) into two PCM data streams with 16 bit word length and a sampling rate of approximately 35 kHz, which in the following are called PCM data 1 and 2. They are temporarily stored in the corresponding locations of the AMU's data RAM.

As the two PDM data streams at the input of the decimation filters have no separate clock signal, the decimation filters are equipped with a synchronization facility. This feature also supplies the AMU software with the sampling clock (approx. 35 kHz), which is called "I/O Sync" or IOSYNC. More details on data/clock timing can be found in section 2.5.

2.2. SBUS Interface and SBUS

2.2.1. Description of the SBUS

The SBUS was designed to connect the digital sound output of the DMA 2271 D2–MAC Decoder or the MSP 2410 Multistandard Sound Processor to audio–processing ICs such as the AMU 2481 VS Audio Processor or the APU 2471 Audio Processor etc., and to connect these ICs with each other. The SBUS is an unidirectional, digital bus which transmits the sound information in one direction only, so that it is not necessary to solve priority problems on the bus.

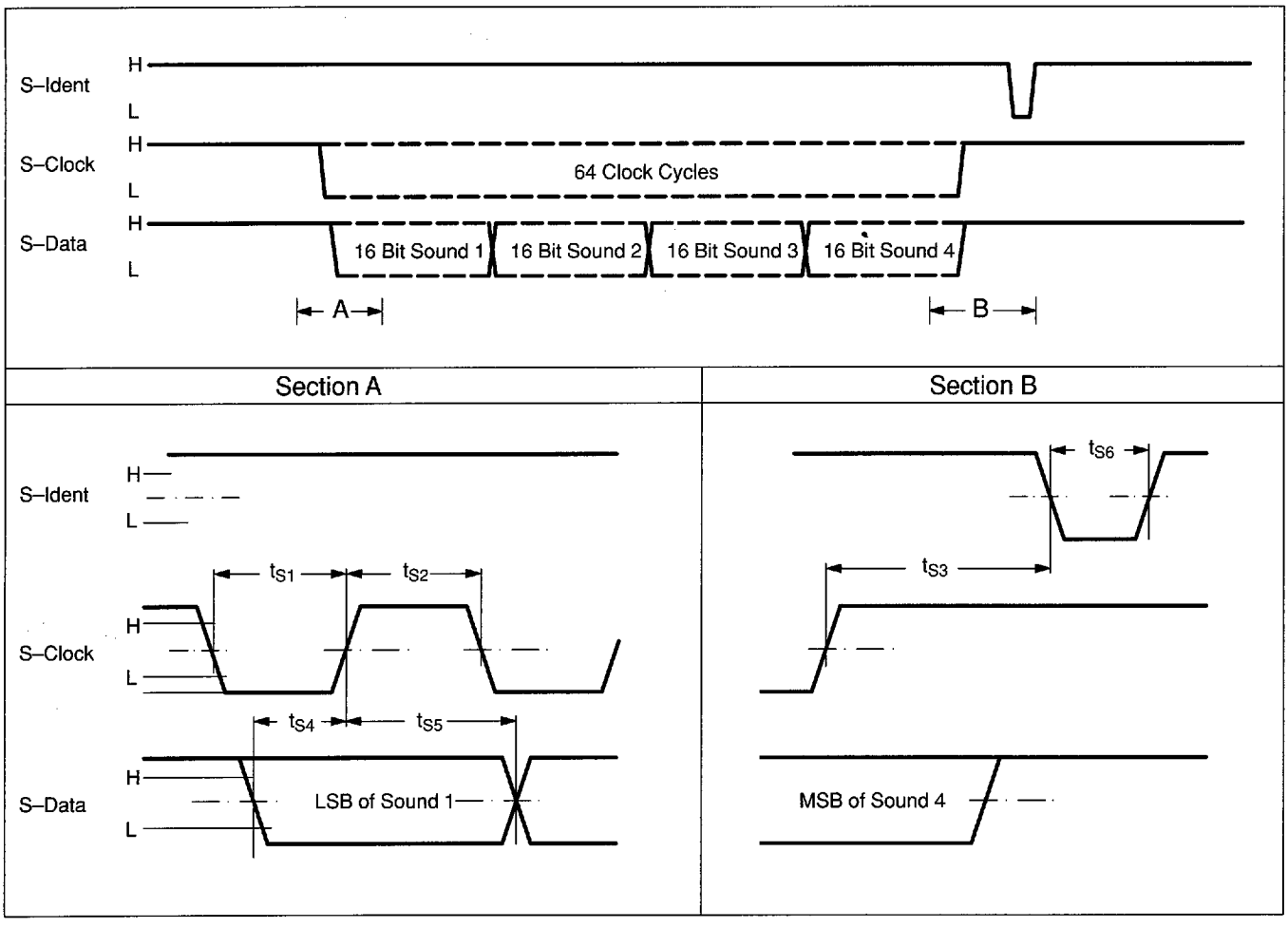


Fig. 2–1: S bus waveforms

The SBUS consists of the three lines SCLOCK, SIDENT and SDATA. The DMA 2271 or the MSP 2410 generates the signals SCLOCK and SIDENT, which control the data transfer to and between the various processors which follow the DMA 2271 or the MSP 2410. For this, the SCLOCK and SIDENT inputs of all processors in the system are connected to the SCLOCK and SIDENT outputs of the DMA 2271 or the MSP 2410. S–data output of the DMA 2271 or the MSP 2410 is connected to the SDATA input of the next following AMU, the AMU's SDATA output is connected to the APU's SDATA input and so on.

If the MSP2410 is used for FM–sound demodulation the SBUS transmits the data at twice the audio sampling rate (64 kHz). The final downsampling to 32 kHz is performed in the AMU's digital decimation filters. For this reason there is a data path from the SBUS interface to the decimation filters.

The sound information is transmitted in frames of 64 bits, divided into four successive 16–bit samples. Each sample represents one sound channel. The timing of a complete transmission of four samples is shown in Fig. 2–1, the times are specified in "Recommended Operating Conditions". The transmission starts with the LSB of the first sample. The SCLOCK signal is used to write the data into the receiver's input register. The SIDENT signal marks the end of one frame of 64 bits and is used as latch pulse for the input register. The repetition rate of the SIDENT pulses is identical to the sampling rate of the D2–MAC or NICAM sound signal; thus it is possible to transfer four sound channels simultaneously.

2.2.2. The SBUS Interface

The SBUS interface of the AMU 2481 VS mainly consists of an input and an output register, each 64–bit wide. The timing to write or read bit by bit is supplied by the SCLOCK signal. In the case of an SIDENT pulse, the contents of the input register are transferred to the data RAM and the contents of the output register are written to the SDATA output.

The SIDENT is also used as the sampling rate reference for the DSP software in the case of digital source mode. In this mode the IOSYNC generated by the decimation filters is locked to the SIDENT. This allows a mixed mode: SDATA and PDM Data can be processed simultaneously. In this case, however, there must be the same audio sample rate of PDM data and SBUS data. If this is not the case, the SIDENT line has to be disabled.

By means of coefficient k33 (see section 3.15.) the AMU 2481 VS can be switched to an SBUS slave mode (bit 4 = 0) or to an SBUS master mode (bit 4 = 1). The slave mode is required in an application as shown in Fig. 1–2 where the DMA 2271 D2–MAC Decoder or the MSP 2410 Multistandard Sound Processor acts as master on the SBUS, i.e. the DMA 2271 or the MSP 2410 supplies the SCLOCK and SIDENT signals as well as the SDATA input signal.

To enable parallel cascading of AMUs without external switches, (e.g. NICAM to SCART and D2MAC to TV) in the 44–PLCC package, the SBUS signals SIDENT and SCLOCK, (and the Main Clock, see section 2.5.) can be passed through the AMU 2481 VS . The corresponding open–drain outputs can be switched to high impedance, which is the default status after power–on reset. To switch them on or off (high imp.), use the same bit that controls the SBUS data output:

Table 2–1: Selection of operation mode

Output mode	k33 : Bit 3
active	0
high impedance	1

2.3. IM Bus Interface and IM Bus

2.3.1. Description of the IM Bus

The INTERMETALL Bus (IM Bus for short) was designed to control the DIGIT 2000 ICs by the CCU Central Control Unit. Via this bus the CCU can write data to the ICs or read data from them. This means the CCU acts as a master whereas all controlled ICs are slaves.The IM bus consists of three lines for the signals Ident (ID), Clock (CL) and Data (D). The clock frequency range is 50 Hz to 170 kHz. Ident and clock are unidirectional from the CCU to the slave ICs, Data is bidirectional. Bidirectionality is achieved by using open–drain outputs with On–resistances of 150 Ohm maximum. The 2.5 kOhm pull–up resistor common to all outputs is incorporated in the CCU.The timing of a complete IM bus transaction is shown in Fig. 2–2 and in the "Recommended Operating Conditions". In the non–operative state the signals of all three bus lines are High. To start a transaction the CCU sets the ID signal to Low level, indicating an address transmission, then sets the CL signal to Low level and switches the first bit on the Data line.Then eight address bits are transmitted, beginning with the LSB. Data takeover in the slave ICs occurs at the positive edge of the clock signal. At the end of the address byte the ID signal goes High, initiating the address comparison in the slave circuits. In the addressed slave the IM bus interface switches over to Data read or write, because these functions are correlated to the address.

Also controlled by the address the CCU now transmits eight or sixteen clock pulses, and accordingly one or two Bytes of data are written into the addressed IC or read out from it, beginning with the LSB. The completion of the bus transaction is signalled by a short Low state pulse of the ID signal. This initiates the storing of the transferred data.

It is permissible to interrupt a bus transaction for up to 10 ms.

For future software compatibility, the CCU must write a zero into all bits not used at present. When reading undefined or unused bits, the CCU must adopt "don't care" behavior.

2.3.2. IM Bus Interface

To write coefficient value(s) into the AMU2481 VS registers the following steps have to be taken:

1. addressing the AMU2481 VS (allows multiprocessor system)
2. writing of 8 bit data into the IM bus interface registers

After having completed step 1, step 2 can be performed as often as the communication between AMU 2481 VS and CCU is required, on the condition that the processor address has not been changed by the CCU.

Comments to the steps mentioned above: The syntax of step 1 is identical to that of step 2. The CCU transmits an 8–bit address to the IM bus interface of the AMU 2481 VS, addressing a certain register or C–RAM location of the AMU. The IM bus interface has to check this address and if necessary, to store it and the following 8 data bits into special IM bus interface registers. Transfer of the data bits to the corresponding C–RAM locations is then performed by the AMU hardware at the sampling rate. Transmission of one Byte (8 bits) takes 100 µs. A spacing of 30 µs must be provided between the end of one transmission and the start of the next one.

In the case of addressing the AMU 2481 VS (step 1 above), the address transmitted first is 102 (= select register). If the following 8–bit data is identical to 14, the AMU 2481 VS will accept further IM bus data. This kind of selective addressing allows controlling of different AMU and APU types (e.g. "selectword" of APU 2471 = 00) in a multi–APU system without using different address ranges. Each APU/AMU type will have its own mask–programmed "selectword".

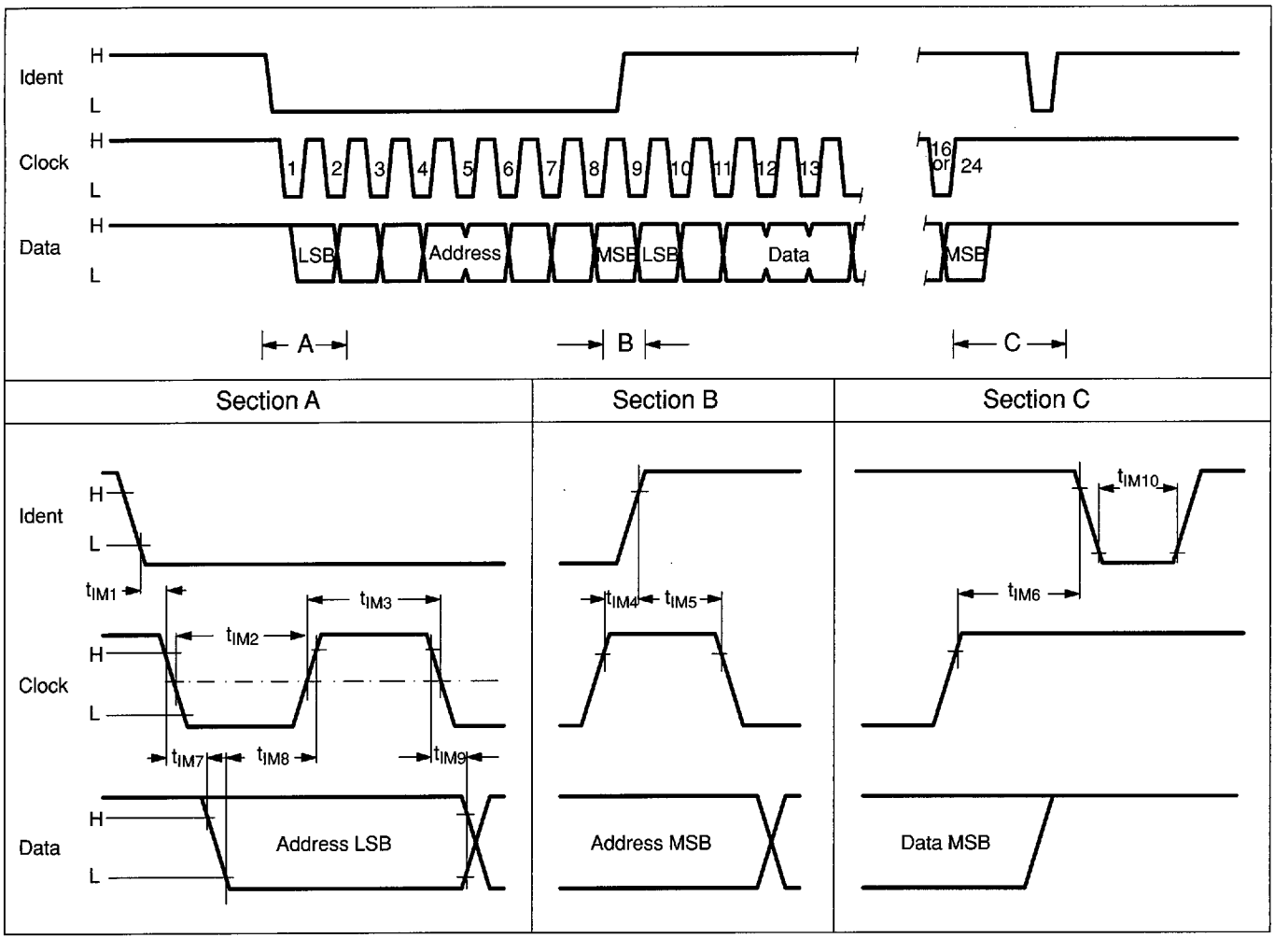


Fig. 2–2: IM bus waveforms

2.4. Digital/Analog Converter (DAC) and Volume

Digital to analog conversion is performed by four special conversion circuits. At any time, the current level of the output signals depends on the value of the reference currents, which are fed to pin 34 (for converters DAC1) and to pin 38 (for converters DAC2). Fig. 2–3 gives application diagrams for the DAC circuits.

The RC network connected to the outputs is required for suppressing the clock from the D/A conversion (1 nF). To achieve an analog deemphasis of 50 µs, the 1 nF capacitors must be enlarged to the 10 nF.

To improve the signal–to–noise ratio of the AMU 2481 VS (especially for low volume settings) an additional volume control facility is provided after the DACs. Digitally adjusted attenuators act in 29 steps of 1 dB each. More about analog Volume in section 3.4.1.

2.5. System Clock ΦM an PDM Sampling Rate

The clock at the AMU's ΦM input must be 18.432 MHz, due to the software oversampling. Therefore bit 2 of k33 has to be set to 1 all the time. The resulting PDM and sampling rate are:

PDM rate = ΦM : 4 = 4.608 MHz,

sampling rate = ΦPDM : 144 = 32 KHz

The physical source of the AMU's system clock is the MSP 2410, the DMA 2271 or the MCU.

To enable parallel cascading of AMUs without external switches, (e.g. NICAM to SCART and DMAC to TV) in the 44–PLCC package, the main clock (the SCLOCK and SIDENT see section 2.2.2.) can be passed through the AMU 2481 VS. The push–pull output can be switched to high impedance, which is default status after power–on reset.To switch it on or off, use the same bit that controls the SBUS output:

Table 2–2: Selection of operation mode

Output mode	k33 :	Bit 3	Bit 2
active		0	1
high impedance		1	1

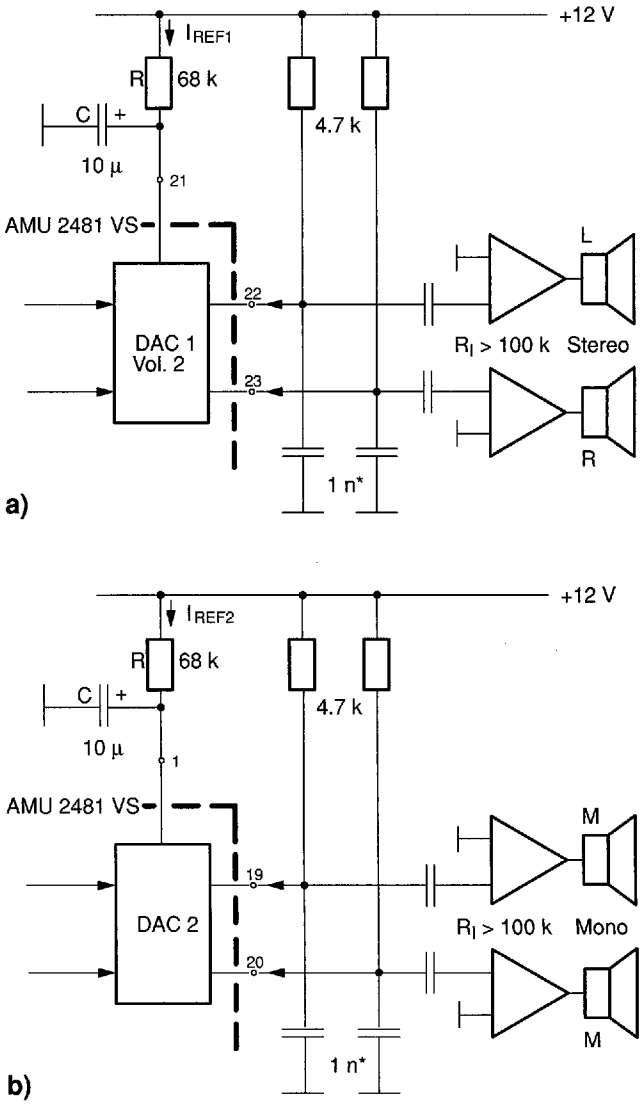


Fig. 2–3: DAC application diagrams
a) DAC 1 Interface
b) DAC 2 Interface

*) optionally 10 nF for 50 µs analog deemphasis

3. Functions Solved by DSP Software

3.1. Explanation of Typical DSP Symbols and Representation of Numbers

In the following, all software features are explained in terms of signal flow diagrams and coefficient tables. In the appendix there is also a complete program structure of the AMU 2481 VS software. To handle these instructions in a correct manner some explanations are required:

Symbols of Signal Flow Diagrams

⊕ adder

⊗ multiplication with coefficient

SHAL shift arithmetic left (multiplication by 2)

ki, Cj coefficient: AMU internal address (Table 5–21)
k = coefficients controlled by CCU and after transfer stored in the AMU's C–RAM,
C = fixed coefficient in the AMU's C–ROM

48/15 z^{1} Term: delay by one sampling clock cycle, realized by one or (in case of two parallel channels) two memory locations of the C–RAM. The numbers are the AMU memory addresses.

Representation of Numbers

The AMU 2481 VS has a two's complement, fixed point arithmetic with decimal point being left-hand and the MSB being the sign bit. The word lengths are defined as follows:

coefficients: 8 bits including sign bit

data at multiplier input: 16 bits including sign bit

intermediate results: 20 bits including sign bit

Table 3–1 shows as an example the range of the 8–bit coefficients, resulting from the conditions mentioned above. From the view of the CCU programmer this might be the most interesting case. Three formats are used to express the coefficient values: Integer decimal, integer hexadecimal and normalized.

Coefficient values must be transferred from the CCU to the AMU via the IM bus in binary format; therefore in most tables of this data sheet the values will be presented in HEX and additionally in the normalized format, to make the digital signal processing background more understandable. To save space the normalized values will be rounded.

Note: Coefficients kij have to be determined such that any overflow in the AMU arithmetic is excluded. Nevertheless, if overflow occurs, the ALU will deal it according to a saturation characteristic. Considering this restriction, for good S/N ratio the digital range must be optimally used.

3.2. Matrixing

To achieve compatibility with standard mono TV sets and to realize bilingual audio performance, the German TV stereo system was defined according to Table 3–2. Additionally, the sound format of SCART and NICAM sources is listed. In TV receivers, video recorders and satellite receivers, these characteristics require matrixing of the two channels.

After detection and evaluation of the identification signal,the NICAM mode (see section 3.10.) and the remote control status, the CCU transmits a coefficient set, according to the current operation mode. The AMU matrixing provides the following audio possibilities (Fig. 3–1):

– mono

– stereo Scart or NICAM:
L on channel 1L
R on channel 1R

– stereo TV: Matrixing L+R and 2R
on channel 1L and channel 1R

– bilingual 0: language A on channel 1L
language B on channel 1R

– bilingual 1: language B on channel1L
language A on channel 1R

– bilingual 2: language A on channel 1L and channel 1R

– bilingual 3: language B on channel 1L and channel 1R

Table 3–1: Range of an 8–bit coefficient value

Coefficient	AMU Internal Presentation	HEX	DEC	Normalized
Max. Value	0111 1111	7F	127	0.9921875
Min. Positive Number	0000 0001	01	001	0.0078125
Max. Negative Number	1111 1111	FF	255	–0.0078125
Min. Number	1000 0000	80	128	–1.0

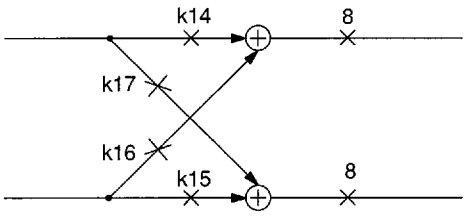


Fig. 3–1: Matrix filter structure

In Table 3–4 all relevant coefficients and the corresponding operation modes (see above) are listed.The values of the coefficients are in HEX format. To understand the dematrixing, there is an additional Table 3–3 giving the corresponding normalized values.

To avoid switching distortions during operation mode change, it is recommended to alter the coefficients in steps of 10 units maximum rather than instantaneously.

Table 3–2: Characteristics of German TV stereo system

	FM1 (Mono)	FM2
1. Sound Signal from TV Channel		
Mono Stereo Bilingual	Mono (L = R) L + R Language A	Mono (L = R) 2 R Language B
2. Sound signal from SCART Input		
Mono Stereo Bilingual	Mono (L = R) L Language A	Mono (L = R) R Language B

Table 3–3: Normalized values for Table 3–4

HEX	DEC	Normalized
10	16	0.125
20	32	0.25
23	35	0.274
F0	–16	–0.125

3.3. Input Select

3.3.1. Main Stereo Channel

As already mentioned, the AMU is provided to process audio data coming from four sources, whereby the controllable input select software switches to the one chosen by the CCU:

1. S_CH 1: stereo channel left (e.g. FM from MSP)
   S_CH 2: stereo channel right
2. S_CH 3: stereo channel left (e.g. NICAM from MSP)
   S_CH 4: stereo channel right
3. PDM_CH 1: stereo channel left
   PDM_CH 2: stereo channel right
4. S_CH 1 and 2 via CF2: PDM_CH 1, stereo ch left
   S_CH 3 and 4 via CF2: PDM_CH 2, stereo ch right

Note:
Switching is performed depending on the coefficient k24–k29; also bit 6 of k33 has to be matched by the CCU (Table 3–5), ordering the corresponding sampling rate (more about k33 in section 3.15.).

3.3.2. Mono Channel

Depending on bit 6 of k33 the source of the mono channel is PDM_CH1 or S_CH 1 and 2 via CF2. This feature is needed to be able to handle FM–Mono and NICAM at the same time.

3.3.3. Volume Prescale

Due to different deviation a volume prescale is necessary when SBUS via CF2 (MSP–FM–mode) is active.The corresponding coefficients are k22 for left and k23 for right channel (see table 3–6).

Table 3–4: Coefficients for different operation modes of channel 1 matrixing (hex)

	Operation Mode												
	Mono		Stereo			Bilingual							
						Mode 0		Mode 1		Mode 2		Mode 3	
Coeff.	FM/ SCART	NICAM	FM	SCART	NICAM	FM/ SCART	NICAM	FM/ SCART	NICAM	FM/ SCART	NICAM	FM/ SCART	NICAM
k14	10	23	20	10	23	10	23	00	00	10	23	00	00
k15	00	00	10	10	23	10	23	00	00	00	00	10	23
k16	00	00	F0	00	00	00	00	10	23	00	00	10	23
k17	10	23	00	00	00	00	00	10	23	10	23	00	00

Table 3–5: Coefficients k24 to k29 and k33 due to input source for stereo channel

Input Source	k24/k27	k25/k28	k26/k29	k33 bit 1
SBUS channel 1/2	7F	00	00	x
SBUS channel 3/4	00	7F	00	x
PDM1/2	00	00	7F	0
SBUS access to CF2 (e.g. FM–Stereo f. MSP)	00	00	7F	1

Table 3–6: Coefficients for full digital scale (FDS) at the DSP–Input

Input Source		k22	k23	k33 bit 1
1. PDM–DATA, max analog input to FDS AMU2481VS		0F	0F	0
2. FM via SBUS to FDS AMU2481VS				
Deviation :	50 kHz	5A	5A	1
	75 kHz	3B	3B	1
	150 kHz	1E	1E	1

3.4. Volume, Balance and Mute

3.4.1. Volume Control for Stereo Channel

To maintain high signal to noise ratio even with low input levels, the complete volume adjustment is performed behind the D/A conversion. An analog volume adjustment of 00 dB to –29 dB is possible. For the Stereo channel k34is to be set from 29 to 00, corresponding to an attenuation of 00 dB to –29 dB.

For the mono channel no volume control is performed.

3.4.2. Balance

The two coefficients k00 and k01 should be used only for balance and muting. An output scaling, left and right separately, can be achieved by varying the two coefficients independently. The allowed range is 00hex to 5Chex. Coefficient k06 should always be set to 5Chex except a mute is required.

3.4.3. Mute

If a mute function is required (e.g. while measuring S/N ratio) the coefficients k00,k01 and k06 must be set to zero. If they are set to 00 a hardware mute occurs.

Table 3–7: Volume control

Overall Level/dB	VOL 1 Stereo k34
0	1D; 0.227
–1	1C; 0.219
–2	1B; 0.211
–3	1A; 0.203
–4	19; 0.195
–5	18; 0.188
–6	17; 0.180
–7	16; 0.172
–8	15; 0.164
–9	14; 0.156
–10	13; 0.148
–11	12; 0.141
–12	11; 0.133
–13	10; 0.125
–14	0F; 0.117
–15	0E; 0.109
–16	0D; 0.102
–17	0C; 0.094
–18	0B; 0.086
–19	0A; 0.078
–20	09; 0.070
–21	08; 0.063
–22	07; 0.055
–23	06; 0.047
–24	05; 0.039
–25	04; 0.031
–26	03; 0.023
–27	02; 0.016
–28	01; 0.008
–29	00; 0.000

3.5. Oversampling Filter

Two oversampling filters in the stereo channels are implemented. The oversampling factor is two. Fig.3–2 shows the frequency response of the filters. Due to the fact that it is a software oversampling, the clock frequency must be fixed at 18.432 MHz.

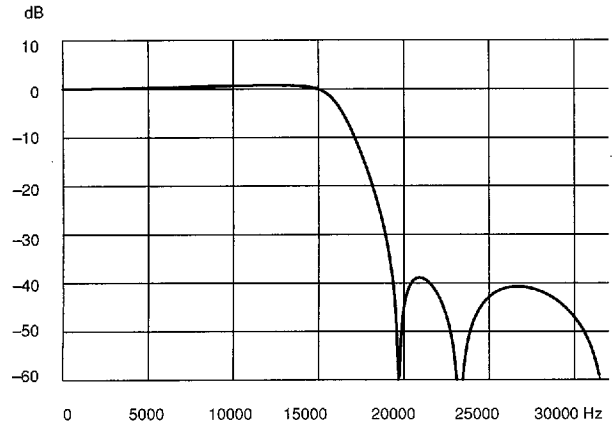


Fig. 3–2: Frequency response of the oversampling filter

3.6. Sin x/x Compensation

The sin x/x compensation results in an improved frequency response. It is a precompensation of the 4 dB loss at half the sampling rate, that happens due to the D/A conversion. Fig. 3–3 shows the frequency response of the sin x/x compensation.

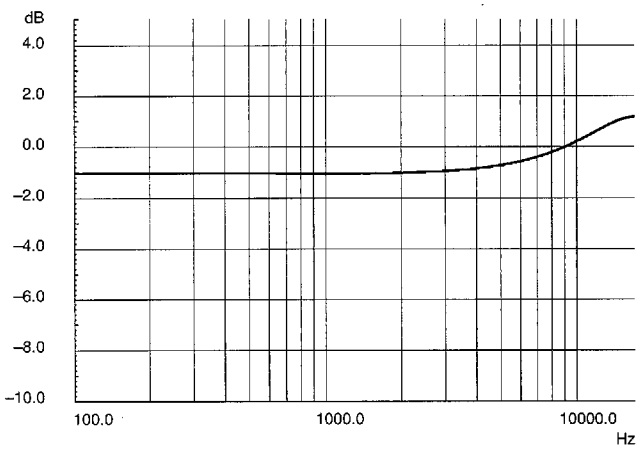


Fig. 3–3: Frequency response of the sin x/x compensation

Due to the fact, that the stereo channel has an oversampled output (fs=64KHz) a different sin x/x compensation has to be computed than in the mono channel (fs = 32KHz). Therefore two different coefficients have to be set.

Table 3–8: Coefficients for sinx/x compensation (hex/norm)

Coefficient	sinx/x comp. on	sinx/x comp. off
k18 (stereo)	EE –0.140	00 0.0
k19 (mono)	E4 –0.218	00 0.0

3.7. 50 µs Deemphasis for Mono Channel

In case of FM transmission (e.g. FM–Mono via CF2 from MSP, see also section 3.3.2.) a 50 µs deemphasis for the mono channel is required. Therefore set k30 to the corresponding value:

Table 3–9: Coefficient for deemphasis (hex/norm)

Coefficient	50 µs deem on	50 µs deem off
k30	44 –0.57	00 0.0

3.8. RMS Detection or Decoding of the Identification Signal

Due to the fact, that there is only one output address (IM–bus address 63) in the AMU 2481 VS it must be decided which value, RMSLEV or IDLEV, is given out. The adaptive deemphasis is only needed with satellite TV and the identification decoding is only required with terrestrial TV transmission. This makes it possible to run only one of both at the same time.Therefore coefficient k13 is to be understood as a switch between both modes.

Table 3–10: RMS detection or identification decoding active (hex/norm)

Coefficient	Value	Active
k13	00 0.0	Identification Dec.
k13	80 –1.0	RMS Detection

This means, that if adaptive deemphasis is required (active deemphasis needs the RMS value to be adjusted) k13 has to be set to 80hex.
If identification decoding is required k13 has to be set to 00hex.

3.9. Deemphasis for Stereo Channel

The AMU 2481 VS has a very powerful filter, to implement most of the known deemphasisfilters, that are used in terrestrial and satellite TV–broadcasting.

3.9.1. J17, 50 µs, 75 µs Deemphasis

For the function of fixed deemphasis 50 µs, 75 µs and J17 or to switch off the deemphasis function, the two coefficient sets have to be set to fixed values. They are presented in Table 3–11.

3.9.2. Wegener Panda 1

An adaptive deemphasis, e.g. Wegener Panda I, has a filter characteristic that depends on the RMS value of the input signal. Therefore, the AMU 2481 VS has a RMS–detector built-in. Its input can be weighted with a highpassfilter. The built-in highpassfilter of the AMU 2481 VS has a selectable gain and a selectable edge frequency. The corresponding coefficients are k11 and k12. They are described in Table 3–12.

The RMS values of the left and right channels (computed in the AMU) are given to IM bus address 63 with an alternation frequency of about 2 kHz. This means that the two deemphasis filters can be updated with a maximum frequency of 1 kHz. Left and right channels can be identified by interpreting the sign bit of the value read from addr.63 (left channel: sign bit = 0, right channel: sign bit = 1). The CCU has to change the corresponding filter coefficients (k02: left channel RMS, k03: right channel RMS) in the AMU's deemphasis block and herewith "adapt" the filter. The coefficients k02/k03 are found in Table 3–13.

It is very important, that left and right channel are updated as often as possible. Faster than once a ms should be the goal. If this can not be achieved with the used controller, adapting the filter should be done by pairs of left and right, with a minimum delay between both channels within one filterupdate. Stereo–failures would be the result of asynchronous updating. Regarding the speed of the CCU (time t for RMS read and k02/k03 write), there are two proposals how to control the AMU 2481 VS with its adaptive deemphasis filter block:

1. CCU faster than 2 kHz (t < 0.5 ms)

The CCU reads @63 and writes corresponding coefficients for deemphasis filter for left or right channel within less than 0.5 ms (less than 0.5 ms because it has to be sure that no RMS value for left or right channel is missed). Timing of the CCU control cycle is shown in Fig. 3–4.

2. CCU slower than 2 kHz (t > 0.5 ms)

The CCU reads three times @63 within a time range of 0.5 ms to 1.0 ms. This makes sure that one of the three values will be RMS value of the left (right) channel and the other two values will be the RMS values of the right (left) channel. Now the CCU can evaluate the new coefficients for the deemphasis filter of the left and the right channel. After that, both channels have to be updated within 1 ms to avoid problems with stereosynchronicity. Timing of the CCU control cycle is shown in Fig. 3–5.

Table 3–11: Coefficients for deemphasis (hex/norm)

Function	Coefficient	Value
J17	k02/k03 k04 k05 k07	2F; 0.367 20; 0.25 80 –1.0 09; 0.073
50 µs	k02/k03 k04 k05 k07	76; 0.92 40; 0.5 80 –1.0 00; 0.0
75 µs	k02/k03 k04 k05 k07	57; 0.68 40; 0.5 80 –1.0 00; 0.0
adaptive	k02/k03 k04 k05 k07	s. Table 3–13 20; 0.25 80 –1.0 00; 0.0
off	k02/k03 k04 k05 k07	00; 0.0 00; 0.0 00; 0.0 7F; 0.99

Table 3–12: Coefficients for highpassfilter at RMS–detector input (hex / norm))

Function	Coefficient	Value
1.5 kHz HP	k11 k12	09 0.0703 D8 –0.3125
0 Hz= Pass	k11 k12	08 0.0625 00 0.0

Table 3–13: Coefficients k02/k03 for adaptive deemphasis

RMS–value	k02/k03	RMS–value	k02/k03	RMS–value	k02/k03	RMS–value	k02/k03
0	4	20	18	40	2A	60	3A
1	5	21	18	41	2B	61	3A
2	6	22	19	42	2B	62	3B
3	7	23	19	43	2B	63	3B
4	8	24	1A	44	2C	64	3C
5	9	25	1A	45	2C	65	3D
6	9	26	1B	46	2D	66	3F
7	A	27	1C	47	2D	67	40
8	B	28	1C	48	2E	68	41
9	C	29	1D	49	2E	69	45
A	C	2A	1E	4A	2F	6A	49
B	D	2B	1E	4B	2F	6B	4D
C	D	2C	1F	4C	30	6C	52
D	E	2D	20	4D	30	6D	56
E	E	2E	20	4E	31	6E	5A
F	F	2F	21	4F	31	6F	5F
10	10	30	22	50	32	70	62
11	10	31	22	51	32	71	66
12	11	32	23	52	33	72	69
13	11	33	24	53	33	73	6C
14	12	34	24	54	34	74	70
15	12	35	25	55	34	75	73
16	13	36	26	56	35	76	75
17	13	37	26	57	35	77	77
18	14	38	27	58	36	78	79
19	14	39	27	59	36	79	7B
1A	15	3A	28	5A	37	7A	7D
1B	15	3B	28	5B	37	7B	7F
1C	16	3C	29	5C	38	7C	7F
1D	16	3D	29	5D	38	7D	7F
1E	17	3E	29	5E	39	7E	7F
1F	17	3F	2A	5F	39	7F	7F

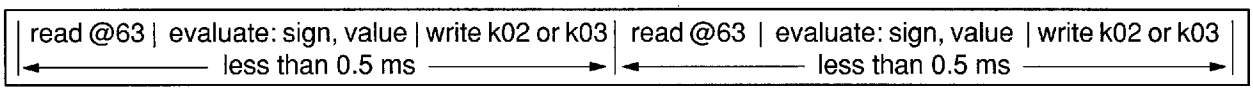


Fig. 3–4: Timing of constantly repeated CCU control cycle; CCU faster than 2 kHz (t < 0.5 ms)

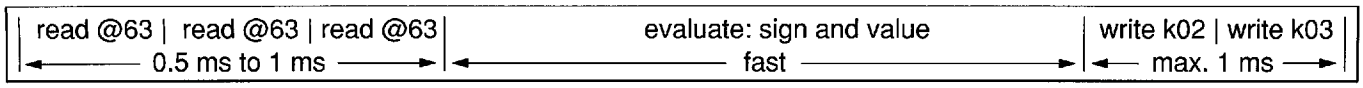


Fig. 3–5: Timing of CCU control cycle repeated as fast as possible; CCU slower than 2 kHz (t > 0.5 ms)

3.10. Decoding of the Identification Signal

Note: Detection of the identification signal is only possible if an ADC is used.

In the German TV standard audio information can be transmitted in three modes: Mono, stereo or bilingual. To detect information about the current audio operation mode, the AMU has to detect the so–called identification signal, which can then be evaluated by the CCU. This signal, generated at the transmitter, is a peak at the identification frequency depending on the operation mode shown in Table 3–14, which modulates the amplitude of a pilot carrier. After addition to the R channel the resulting sum modulates the FM carrier. The pilot carrier frequency is 54.6875 kHz, which corresponds to 3.5 times the horizontal frequency.

Table 3–14: Identification frequencies for different operation modes

Operation Mode	Identification Frequency
Mono	none (=Pilot is unmodulated)
Stereo	117.5 Hz
Bilingual	274.1 Hz

To detect the identification signal, the AMU has theoretically to perform an amplitude demodulation, filtering and measurement of the level of the two possible identification frequencies. The CCU may then read these values for evaluation by its software. To manage this, the AMU 2481 VS uses the output of the second decimation filter of the right channel (PDM2), which is intermediately stored in the corresponding RAM location. This signal is mixed in such a way, that the pilot falls to 618.98 Hz. After decimation to a sampling rate of 2 kHz, amplitude demodulation of the signal is then performed.

A bandpass filter working in succession with three different coefficient sets (Table 3–17), which are supplied by the CCU, extracts the identification frequency (if available), rectifies and smooths out variations in the signal's level, receiving a value for the identification signal strength. This value (IDLEV) is then ready to be read by the CCU, where the evaluation is performed, assigning the correct center frequency of the respective bandpass to the corresponding level value.

It is obvious, that the above bandpass filtering is a very critical item. The passband has to be extremely narrow (0.32 Hz bandwidth) resulting in a high sensitivity of the center frequency to clock jitter. Therefore, for proper execution, the clock tolerance is expected to be in the range of ±400 ppm, i.e. a deviation of the bandpass center frequency of ±0.1 Hz.

3.10.1. Recommended Software Frame for Detection of the Identification Signal

The CCU software for the complete task should contain the items listed in Table 3–18, which have to be sequenced according to Table 3–15 or Table 3–16. Two cases must be distinguished in sequencing the items of Table 3–18:

1. After reset, program or channel change the sequence according to Table 3–15 has to be applied.

2. For further decoding of the identification signal the sequence of Table 3–16 is valid. Now after each IDLEV, which has been read from the AMU, evaluation is performed. Also the "AMU transient times" for the calculation of the IDLEVs is now extended, because now precise information about IDLEV is more important than very fast information, as is the case after reset, program or channel change.

The evaluation of **two** IDLEVs belonging to the two possible identification frequencies consists of their subtraction, and the difference being compared with a user–definable threshold level (TL) stored in the EAROM. TL should be approximately 10 hex.

To evaluate the IDLEVs, the two cases already mentioned have also to be considered:

3. For further decoding of the identification signal a hysteresis loop shown in Fig. 3–6 is to apply.

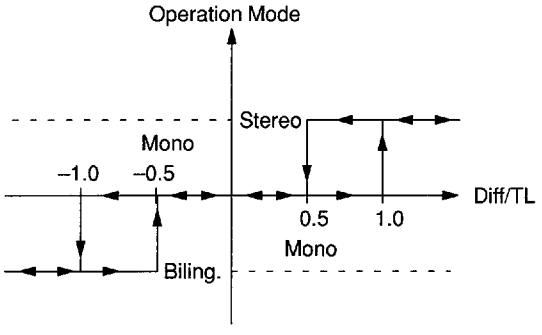


Fig. 3–6: Hysteresis loop for operation mode determination

Table 3–15: Instruction sequence for case 1

Step	Item (arg)
1	TRANSF (ICS)
2	WAIT (T > 1)
3	TRANSF (BCS)
4	WAIT (750)
5	FETCH (IDLEV)
6	TRANSF (ICS)
7	WAIT (T > 1)
8	TRANSF (SCS)
9	WAIT (750)
10	FETCH (IDLEV)
11	EVALUATION

Table 3–16: Instruction sequence for case 2

Step	Item (arg)
1	TRANSF (ICS)
2	WAIT (T > 1)
3	TRANSF (BCS)
4	WAIT (2000)
5	FETCH (IDLEV)
6	EVALUATION
7	TRANSF (ICS)
8	WAIT (T > 1)
9	TRANSF (SCS)
10	WAIT (2000)
11	FETCH (IDLEV)
12	EVALUATION

Table 3–17: Coefficients transmitted between CCU and AMU, necessary for identification detection

Coefficient Set	Coefficient	Value	Comment
BCS CCU to AMU	k12 k10 k11 k09 k08	38 ;0.4375000 2F ;0.3671875 7F ;0.9921875 27 ;0.3046875 7F ;0.9921875	BCS = Bilingual Coefficient Set Set belongs to a center frequency of 274.1 Hz (= bilingual)
ICS CCU to AMU	k12 k10 k11 k09 k08	0 ;0 0 ;0 0 ;0 81 ;–0.9921875 0 ;0	ICS = Intermediate Coefficient Set
SCS CCU to AMU	k12 k10 k11 k09 k08	38 ;0.4375000 29 ;0.3203125 7F ;0.9921875 6F ;0.8671875 3E ;0.4843750	SCS = Stereo Coefficient Set Set belongs to a center frequency of 117.5 Hz (= stereo)
Address 63 AMU to CCU	IDLEV	depending on operation mode	Calculated level to be evaluated by CCU

Note: The sequence of coefficients must be: k12, k10, k11, k09, k08

Table 3–18: Instructions for mode identification

Item Name (arg)	Comment
TRANSF (CSET)	CCU transfers coefficient set BCS, ICS or SCS to AMU
WAIT (T)	CCU Waiting Cycle of T ms
FETCH (IDLEV)	CCU fetches IDLEV from AMU and memorizes it
EVALUATION	CCU evaluates last two IDLEVs, determining mono, stereo and bilingual

3.11. SBUS Output

To be able to cascade the AMU 2481 VS and other ICs of the APU family, the SBUS output can be switched into different modes.

SBUS channel1 and SBUS channel3 carry always the samples of the left stereo channel. The samples of SBUS channel2 and SBUS channel4 can be switched between stereo right and FM–mono by means of coefficients k20 and k21 (see section 6. and Table 3–19).

Table 3–19: Stereo Right / FM–Mono to SBUS ch2 / SBUS ch 4, coefficients k20, k21 (hex/norm)

Coefficient/SBUS out		FM–Mono		Stereo R	
k20	SBUS ch2	80	–1.0	00	0.0
k21	SBUS ch4	80	–1.0	00	0.0

3.12. 50 µs Preemphasis for SBUS Output

The 50 µs digital preemphasis feature has been implemented to get compatibility to the former concept using the analog deemphasis network connected to the DAC outputs of the AMU or APU. In the case of NICAM operation mode, this analog deemphasis has to be precompensated. In the combined system shown in Fig. 1–2, the 50 µs deemphasis is now realized in the AMU 2481 VS by digital means, so that the preemphasis is not needed. In this case, it is possible to switch off the preemphasis by means of coefficient k31:

Table 3–20: 50 µs digital preemphasis (hex/norm.)

50 µs pre-emphasis	ON	OFF
k31	BB (–0.539)	0 (0.0)

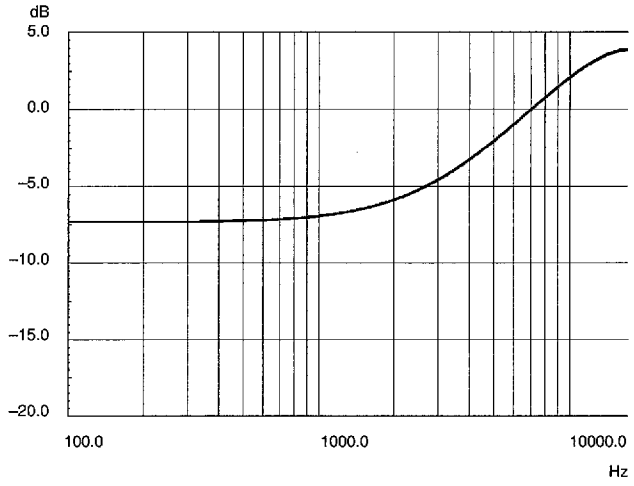


Fig. 3–7: 50 µs digital preemphasis frequency response

3.13. Controller Software for Wegener Panda 1

The following is a proposal describing the implementation of Wegener Panda 1 deemphasis in the CCU controller software. The algorithm shown in Fig. 3–8 should be repeated as often as possible. For best results, integration into the highest interrupt sequence is recommended.

While computing in the Audio Processor, the RMS–values for the right channel are multiplied by –1 in order to set the signbit. This must be reversed in the CCU before the new coefficient value can be read from the table. Using this algorithm, the table range must be 1 to 7F. Because zero does not have a valuable signbit, any zero–value which is read into the RMS register @63 should be ignored.

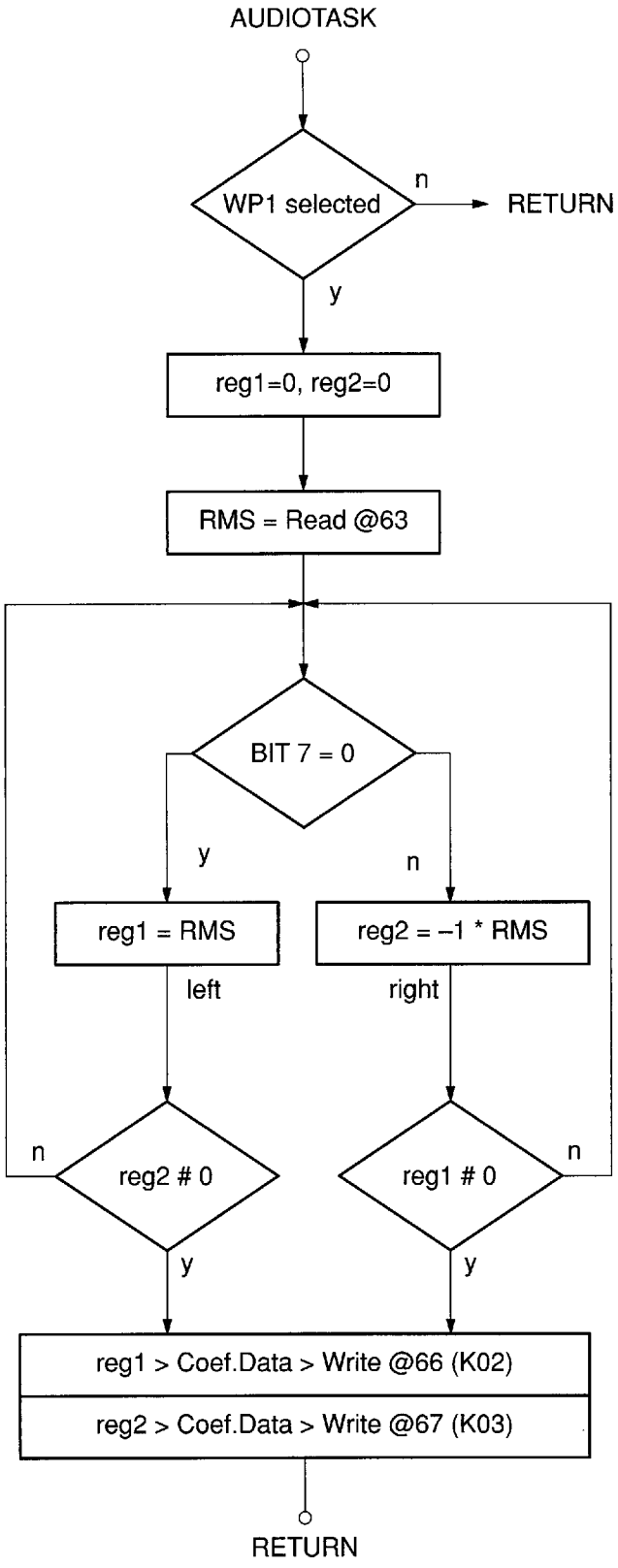


Fig. 3–8: Wegener Panda 1 controller software

3.14. AMU 2481 VS Initialization

After switching on the power or after reset the AMU 2481 VS requires a certain start–up time (Fig. 3–9) to accept coefficients and valid audio data.

– Immediately after a reset the VOL 1 (k0/1) is automatically set to zero

– After a delay of another 0.5 s (or 0.6 s after power–on) a complete set of coefficients is transferred by the CCU via the IM bus, beginning with the Select Register Coefficient (addr. 102) and keeping VOL 1 zero

– 20 ms later the mute function is switched off by the CCU

To transfer a complete set of coefficients to the AMU the following sequence is recommended:

1. Select register for processor selection

2. k33; input select

3. k02 to k05, k7 to k32

4. k00, k01, k06 (mute off)

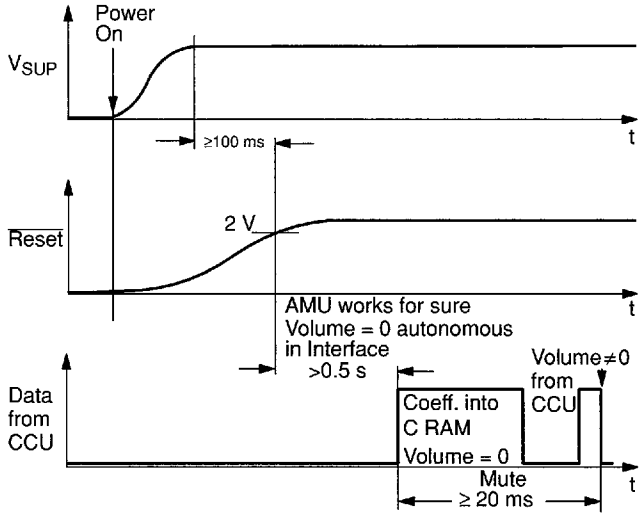


Fig. 3–9: Initialization of the AMU 2481 VS

3.15. Complete Coefficient Table

Table 3–21 details all coefficients and control words which can be influenced by the CCU. The chapters containing more details about certain coefficients are noted in the right-hand column.

Table 3–21: Available addresses in the AMU C–RAM and their applications

Address	Coefficient	Description	See Section
Value to be read from the AMU's Output Buffer to the CCU			
63	IDLEV/ RMSLEV	Identification Signal Strength / RMS Level	3.8.
Values to be written into the AMU's C–RAM			
64	k00	Balance, Mute Stereo Channel Left	3.4.2., 3.4.3.
65	k01	Balance, Mute Stereo Channel Right	3.4.2., 3.4.3.
66	k02	Coefficient for Deemphasis kw1l	3.9.
67	k03	Coefficient for Deemphasis kw1r	3.9.
68	k04	Coefficient for Deemphasis kw2	3.9.
69	k05	Coefficient for Deemphasis kw3	3.9.
70	k06	Mute mono channel	3.4.3.
71	k07	coefficient for deemphasis kw4	3.9.
72	k08	Coefficient for Identification Filter kv	3.10.
73	k09	Coefficient for Identification Filter k1h	3.10.
74	k10	Coefficient for Identification Filter k1l	3.10.
75	k11	Coefficient for Identification Filter k2h	3.10.
76	k12	Coefficient for Identification Filter k2l	3.10.
77	k13	Select: Pilot or RMS Detection	3.8.
78	k14	Dematrixing Stereo Channel	3.2.
79	k15	Dematrixing Stereo Channel	3.2.
80	k16	Dematrixing Stereo Channel	3.2.
81	k17	Dematrixing Stereo Channel	3.2.
82	k18	ksinx Stereo Channel	3.6.
83	k19	ksinx Mono Channel	3.6.
84	k20	Select SBUS 2 Output	3.11.
85	k21	Select SBUS 4 Output	3.11.
86	k22	Volume prescale FM1/PDM1	3.3.3.
87	k23	Volume prescale FM2/PDM2	3.3.3.
88	k24	Input Select L SBUS 1	3.3.
89	k25	Input Select L SBUS 3	3.3.
90	k26	Input Select L FM1/PDM1	3.3.
91	k27	Input Select R SBUS 2	3.3.
92	k28	Input Select R SBUS 4	3.3.
93	k29	Input Select R FM2/PDM2	3.3.
94	k30	Coefficient for 50 µs Deemphasis (Mono Channel)	3.7.
95	k31	Coefficient for 50 µs Preemphasis SBUS Output	3.12.

Table 3–21, continued

Address	Coefficient	Description	See Section
Values to be written into the AMU's C–RAM			
97	k33	Control Word for Standard Selection	3.15.
98	k34	VOL1 Analog Volume Control Stereo Channel	3.4.1.
102	Select Register	Processor Selection	2.3.2.

Notes to Table 3–21:

Note 1) k13 is to be interpreted as a switch between Identification decoding and RMS detection.

Note 2) Cascading of two or more AMUs for future applications requires additional control information concerning the SBUS. This is done by means of k33, and to ensure upward compatibility all bits are defined as follows:

k33:

Bit 7	= 0*	clock divider = 4; ΦPDM = ΦM: 4
	= 1	clock divider = 3; ΦPDM = ΦM: 3
Bit 6	= 0*	sampling rate is derived from system clock
	= 1	sampling clock according to SIDENT of digital source (SBUS)
Bit 5	= 0*	normal mode
	= 1	test mode

concerning the SBUS the AMU 2481 VS is:

Bit 4	= 0*	SBUS slave
	= 1	SBUS master (the AMU 2481 VS generates SCLK and SIDENT)
Bit 3	= 0	SBUS data output active
	= 1*	SBUS data output = high impedance
Bit 2	= 0*	Pal mode (sampling rate = ΦPDM : 128) (section 3.3.)
	= 1	D2MAC/NICAM mode (sampling rate = ΦPDM :144) (section 3.3.)
Bit 1	= 0*	normal SBUS input
	= 1	SBUS access to conversion filter
Bit 0	= 0	not used, for compatibility must be set to 0

For the additional outputs (SCLK, SIDENT, Audio–Clock) of the 44–pin PLCC version of the AMU 2481 VS:

Bit 3	= 0	active
	= 1*	high impedance

* Reset status

4. Specifications

4.1. Outline Dimensions

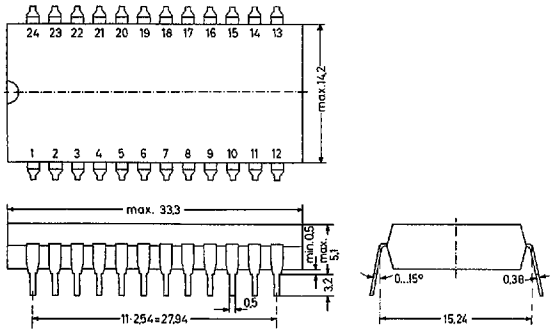


Fig. 4–1: AMU 2481 VS in 24–pin Dil Plastic Package, 20 B 24 according to DIN 41 870

Weight approx. 4.5 g Dimensions in mm

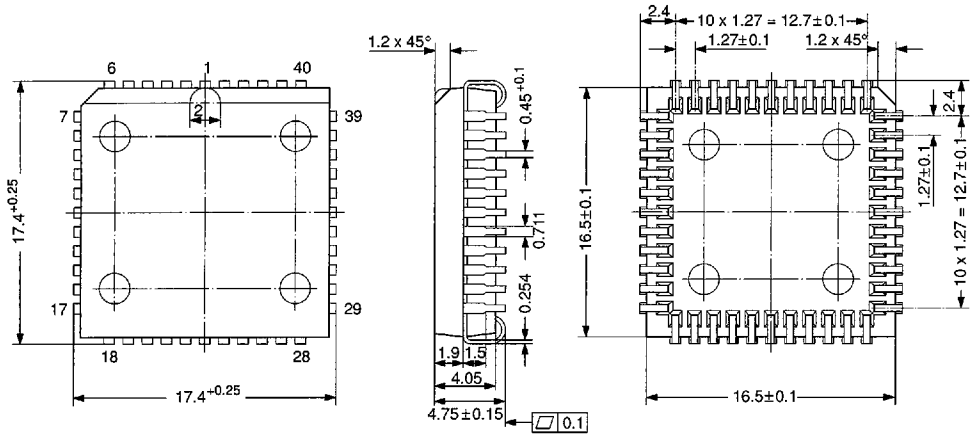


Fig. 4–2: AMU 2481 VS in 44–pin PLCC Package, Weight approx. 2.2 g Dimensions in mm

4.2. Pin Connections

4.2.1. 24–Pin DIL Package

1	I_{REF2} Reference Current Input (for DAC 2)
2	Leave Vacant
3	IM Bus Data Input/Output
4	IM Bus Ident Input
5	IM Bus Clock Input
6	SDATA Output
7	Leave Vacant
8	SCLOCK Input/Output
9	SDATA Input
10	V_{ISB} Internal Substrate Bias Voltage
11	$\overline{\text{Reset}}$ Input
12	Ground (Digital)
13	ΦM Clock Input
14	V_{SUP}
15	SIDENT Input/Output
16	PDM2 Digital Input (R)
17	PDM1 Digital Input (L)
18	Leave Vacant

19 DAC2M Output

20 DAC2M Output

21 I_{REF1} Reference Current Input (for DAC1)

22 DAC1L Output

23 DAC1R Output

24 Ground (Analog)

4.2.2. 44–Pin PLCC Package

1 ΦM Main Clock Input

2 Leave Vacant

3 Leave Vacant

4 Leave Vacant

5 Leave Vacant

6 Leave Vacant

7 SIDENT Input/Output

8 SIDENT Output 2**

9 PDM2 Digital Input (R)

10 Leave Vacant

11 PDM1 Digital Input (L)

12 Vacant*

13 DAC2M Output

14 Vacant*

15 DAC2M Output

16 Vacant*

17 I_{REF1} Reference Current Input (for DAC1)

18 DAC1L Output

19 Vacant*

20 DAC1R Output

21 Leave Vacant

22 Ground (Analog)

23 V_{ISB} Internal Substrate Bias Voltage

24 I_{REF2} Reference Current Input (for DAC2)

25 Leave Vacant

26 Leave Vacant

27 IM Bus Data Input/Output

28 Leave Vacant

29 IM Bus Ident Input

30 Leave Vacant

31 IM Bus Clock Input

32 Leave Vacant

33 SDATA Output

34 Leave Vacant

35 V_{SUP}

36 Ground Supply

37 SCLOCK Input/Output

38 Leave Vacant

39 SDATA Input

40 Leave Vacant

41 Leave Vacant

42 $\overline{\text{Reset}}$ Input

43 SCLOCK Output 2**

44 ΦM Main Clock Output**

* = In order to minimize crosstalk, these pins should be appropriately grounded.

** = additional outputs compared to 24–pin Dil package pins 8, 43 see section 2.2.2.; pin 44 see section 2.5.

4.3. Pin Descriptions (pin numbers for 24–pin DIL package)

Pins 1 and 21 – Reference Current Inputs (Fig. 4–3)
These inputs require a current of 150 µA called reference current I_{REF} and serving for volume adjustment in the DAC interfaces.

Pin 12 – Digital Ground, 0
This pin must be connected to the negative of the supply. It must be used for ground connections in conjunction with digital signals.

Pin 3 – IM Bus Input/Output (Fig. 4–8)
Via this pin, the AMU 2481 VS is connected to the IM bus and communicates with the CCU.

Pins 4 and 5 – IM Bus Inputs (Fig. 4–4)
Via these pins, the AMU 2481 VS is connected to the IM bus and receives instructions from the CCU.

Pins 6, 8, 9 and 15 – Serial Audio Interface (SBUS)
Pin 9 is the S– Data input (Fig. 4–7) and pin 6 the S– Data output (Fig. 4–9). Pins 8 and 15 are SCLOCK and SIDENT inputs/outputs (Fig. 4–10), the status depending on bit 4 in coefficient k33 (see sections 2.2.2. and 2.5.).

Pin 14 – V_{SUP} Supply Voltage
This pin must be connected to the positive of the supply.

Pin 10 – V_{ISB} Internal Substrate Bias Voltage
The AMU 2481 VS has an on–chip substrate bias generator which produces a negative bias voltage of about 3.4 V. Pin 10 should have a 0.1 µF capacitor to ground.

Pin 11 – $\overline{\text{Reset}}$ Input (Fig. 4–4)
In the steady state, high level is required at pin 11. A low level normalizes the AMU 2481 VS. Initialization is described in section 3.14.

Pin 13 – ΦM Main Clock Input (Fig. 4–5)
This pin receives the required main clock signal from the MCU 2600 or MCU 2632 Clock Generator IC or from the DMA 2271 D2–MAC Decoder or the MSP 2410 Multistandard Sound Processor.

Pins 16 and 17 – $\overline{\text{PDM2}}$ and $\overline{\text{PDM1}}$ Digital Input (Fig. 4–6)
These pins receive the pulse–density modulated output signals of the ADC 2311 E.

Pins 19 and 20 – DAC2M Outputs (Fig. 4–9)
These pins supply the audio output signals as output currents whose amplitude is determined by the reference current I_{REF2} fed to pin 1. The output signal of pins 19 and 20 is only influenced by the VOL 1 volume control.

Pins 22 and 23 – DAC1L and DAC1R Outputs (Fig. 4–9)
These pins supply the audio output signals as output currents whose amplitude is determined by the reference current I_{REF1} fed to pin 21. The output signal of pins 22 and 23 is influenced by the VOL 1 and VOL 2 volume control facilities.

Pin 24 – Analog Ground 0
This pin must be connected to the negative of the supply. It serves as ground connection for analog signals.

4.4. Pin Circuits (pin numbers for 24–pin DIL package)

The following figures schematically show the circuitry at the various pins. The integrated protection structures are not shown. The letter "E" means enhancement, the letter "D" depletion.

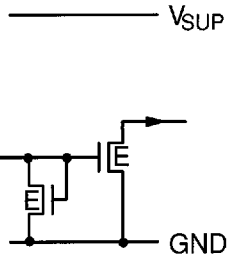


Fig. 4–3:
Input Pins 1, 21

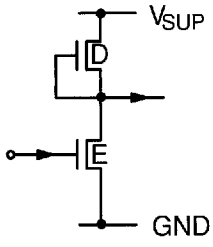


Fig. 4–4:
Input Pins 4, 5, 11

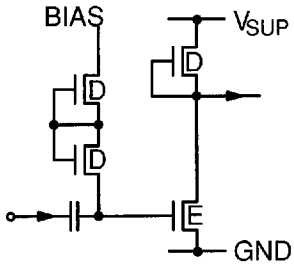


Fig. 4–5:
Input Pin 13

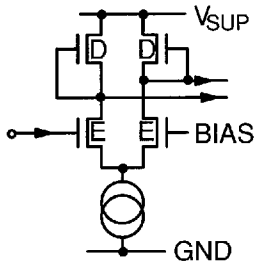


Fig. 4–6:
Input Pins 16, 17

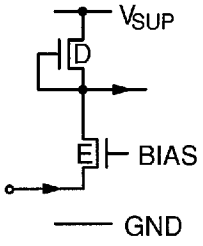


Fig. 4–7:
Input Pin 9

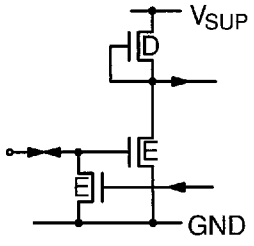


Fig. 4–8:
Input/Output Pin 3

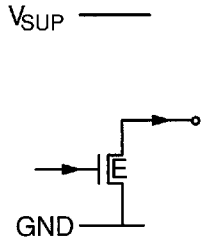


Fig. 4–9:
Output Pin 6,19, 20, 22

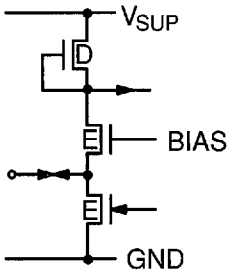


Fig. 4–10:
Input/Output Pins 8, 15

4.5. Electrical Characteristics (pin numbers for 24–pin DIL package)

All voltages are referred to ground.

4.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	–40	+125	°C
V_{SUP}	Supply Voltage	14	–	6	V
V_I	Input Voltage, all Inputs	–	–0.3 V	V_{SUP}	–
V_{DO}	DAC Output Voltage	19, 20, 22, 23	–0.3	+12	V
V_{SO}	SBUS Output Voltage	6, 8, 15	–0.3 V	V_{SUP}	–
I_{DSO}	DAC and SBUS Output Current	6, 8, 15, 19, 20, 22, 23	–	10	mA

4.5.2. Recommended Operation Conditions at T_A = 0 to 65 °C, $f_{\Phi M}$ = 14.3 to 18.4 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	14	4.75	5.0	5.25	V
$V_{\Phi MIDC}$	ΦM Clock Input D.C. Voltage	13	1.5	–	3.5	V
$V_{\Phi MIAC}$	ΦM Clock Input A.C. Voltage (p–p)		0.8	–	2.5	V
$\frac{t_{\Phi MIH}}{t_{\Phi MIL}}$	ΦM Clock Input High/Low Ratio		0.9	1.0	1.1	–
$t_{\Phi MIHL}$	ΦM Clock Input High to Low Transition Time		–	–	$\frac{0.15}{f_{\Phi M}}$	–
V_{REIL}	Reset Input Low Voltage	11	–	–	1.2	V
V_{REIH}	Reset Input High Voltage		2.4	–	–	V
I_{REF}	Reference Input Current	1, 21	–	0.15	–	mA
V_{IMIL}	IM Bus Input Low Voltage	3 to 5	–	–	0.8	V
V_{IMIH}	IM Bus Input High Voltage		2.4	–	–	V
$f_{\Phi I}$	ΦI IM Bus Clock Frequency		0.05	–	170	kHz
t_{IM1}	ΦI Clock Input Delay Time after IM Bus Ident Input		0	–	–	–
t_{IM2}	ΦI Clock Input Low Pulse Time		3.0	–	–	µs

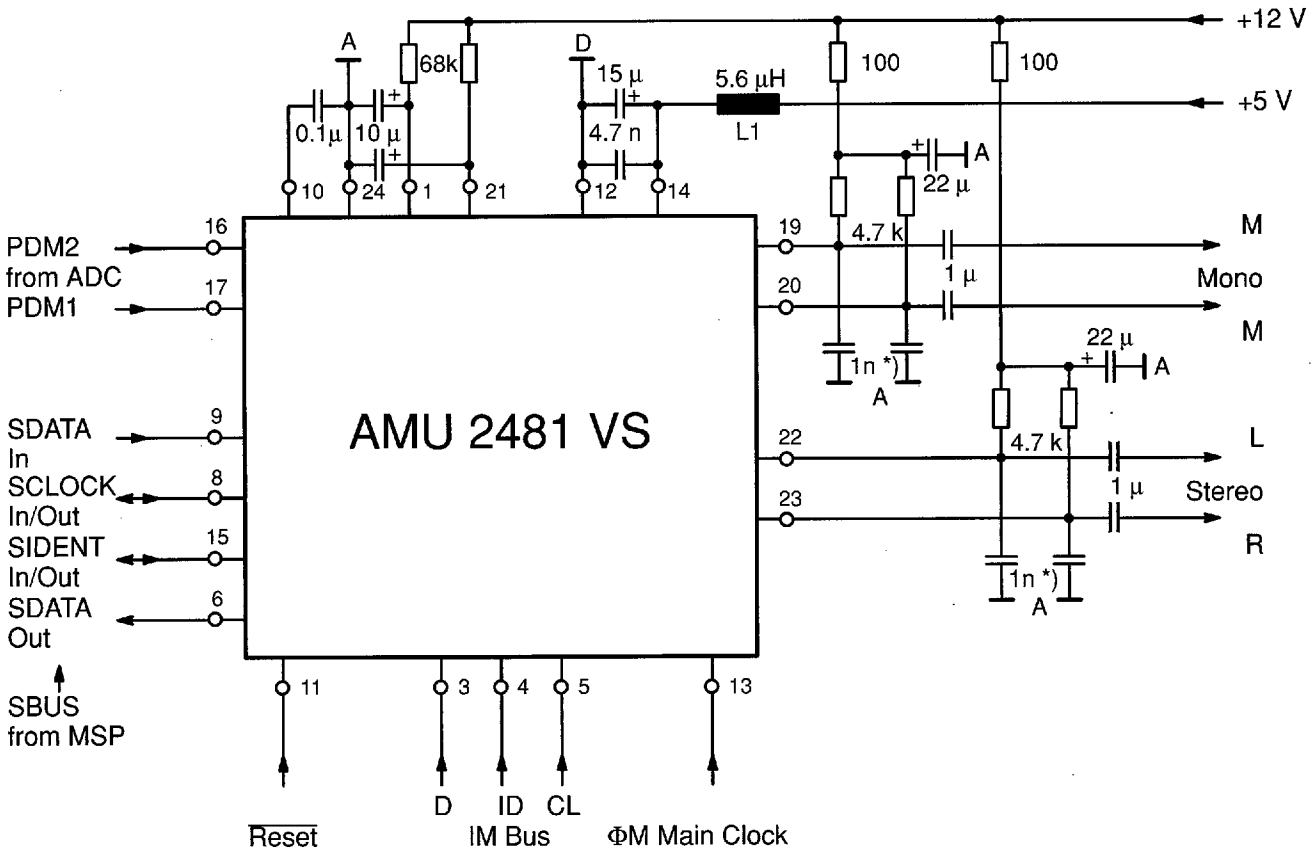
Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
t_{IM3}	ΦI Clock Input High Pulse Time	3 to 5	3.0	–	–	µs
t_{IM4}	ΦI Clock Input Setup Time before Ident Input High		0	–	–	–
t_{IM5}	ΦI Clock Input Hold Time after Ident Input High		1.5	–	–	µs
t_{IM6}	ΦI Clock Input Setup Time before Ident End–Pulse Input		6.0	–	–	µs
t_{IM7}	IM Bus Data Input Delay Time after ΦI Clock Input		0	–	–	–
t_{IM8}	IM Bus Data Input Setup Time before ΦI Clock Input		0	–	–	–
t_{IM9}	IM Bus Data Input Hold Time after ΦI Clock Input		0	–	–	–
t_{IM10}	IM Bus Ident End–Pulse Low Time		3.0	–	–	µs
V_{SIL}	SBUS Input Low Voltage	8, 9, 15	–	–	0.4	V
$-I_{SIH}$	SBUS Input High Current		–	–	20	µA
f_{IS}	ΦSCLOCK Input Frequency	8	–	$\frac{f_{\Phi M}}{4}$	–	–
$\frac{t_{S2}}{t_{S1}}$	ΦSCLOCK Input High/Low Ratio		0.8	1	1.2	–
t_{S3}	ΦSCLOCK Input Setup Time before Ident End–Pulse Input	8, 15	150	–	–	ns
t_{S4}	SDATA Input Setup Time before ΦSCLOCK Input	8, 9	50	–	–	ns
t_{S5}	SDATA Input Hold Time after ΦSCLOCK Input		50	–	–	ns
t_{S6}	SIDENT End–Pulse Input Low Time	15	150	–	–	ns
V_{DIL}	Digital Input Low Voltage	16, 17	–	–	$0.5 \cdot V_{SUP} - 0.3$ V	–
V_{DIH}	Digital Input High Voltage		$0.5 \cdot V_{SUP} + 0.3$ V	–	–	–
C_{ISB}	Internal Substrate Bias Voltage Filter Capacitor	10	–	100	–	nF

4.5.3. Characteristics at T_A = 0 to 65 °C, V_{SUP} = 4.75 to 5.25 V, $f_{\Phi M}$ = 14.3 to 18.4 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
I_{SUP}	Supply Current	14	–	140	170	mA	
V_{IMOL}	IM Bus Output Low Voltage	3	–	–	0.4	V	I_{IMO} = 3 mA
I_{IMOH}	IM Bus Output High Current		–	–	10	µA	V_{IMO} = 5 V
$-I_{SIL}$	SCLOCK/Ident/Data Input Low Current	8, 9, 15	–	1	2.7	mA	V_{SI} = 0.3 V
V_{SIH}	SCLOCK/Ident/Data Input High Voltage		–	–	1.2	V	I_{SI} = 0
V_{SOL}	SBUS Output Low Voltage	8, 9, 15	–	–	0.3	V	I_{SO} = 6 mA
I_{SOH}	SDATA Output High Current	6	–	–	10	µA	V_{SO} = 5 V
I_{OMAIN}	DAC1 Output Peak–to–Peak Current	22, 23	–	0.81	–	mA	I_{REF1} =0.15 mA, VOL2 = 0 dB
			–	25	–	µA	I_{REF1} =0.15 mA, VOL2 = –30 dB
I_{OAUX}	DAC2 Output Peak–to–Peak Current	19, 20	–	0.81	–	mA	I_{REF2} =0.15 mA
THD	Total Hamonic Distortion of DAC Output	19, 20, 22, 23	–	–	0.1	%	BW = 15 kHz
CA	Crosstalk Attenuation within Active Channel Pair		55	60	–	dB	
I_{DAC1O}	DAC1 Output Peak–to–peak Current	22, 23	–	0.81	–	mA	I_{REF1} = 0.15 mA, VOL2 = 0 dB
			–	25	–	µA	I_{REF1} = 0.15 mA, VOL2 = –30 dB
I_{DAC2O}	DAC2 Output Peak–to–peak Current	19, 20	–	0.81	–	mA	I_{REF2} = 0.15 mA,
V_{ISB}	Internal Substrate Bias Voltage	10	–	–3.4	–	V	C_{ISB} = 100 nF
V_{REF1}	Reference Input Voltage Drop	21	–	2.5	–	V	R_{REF1} = 68 kOhm from +12 V, VOL2 = 0 dB
			–	0.45	–	V	R_{REF1} = 68 kOhm from +12 V, VOL2 = –30 dB
V_{REF2}	Reference Input Voltage Drop	1	–	2.5	–	V	R_{REF2} = 68 kOhm from +12 V

5. Appendix 1: Application Circuit (pin numbers for 24–pin Dil package)



*optionally 10 nF for 50 µs analog deemphasis

Fig. 5–1: Application circuit

6. Appendix 2: Program Structure