Preliminary Data Sheet

1 GByte/sec SCI Compliant Switch Node Bypass Circuit

Features

- 2-port Switch Capable of Passing SCI Packets
- Multiplexers Allow Bypassing Around any Port for Faulty Node Isolation.
- Sends and Receives SCI Symbols Every 2 ns for 1 GB/s Data Rate Per Port.
- One Port Conforms to Low Voltage Differential Signalling (LVDS) Standard (IEEE Std. 1596.3)
- +3.3V and +2V Power Supplies
- 301 BGA Package (50 mil spacing, 27mm/side)
- IEEE Std 1149.1 Test Access Port for Diagnostics and Boundary Scan

Introduction

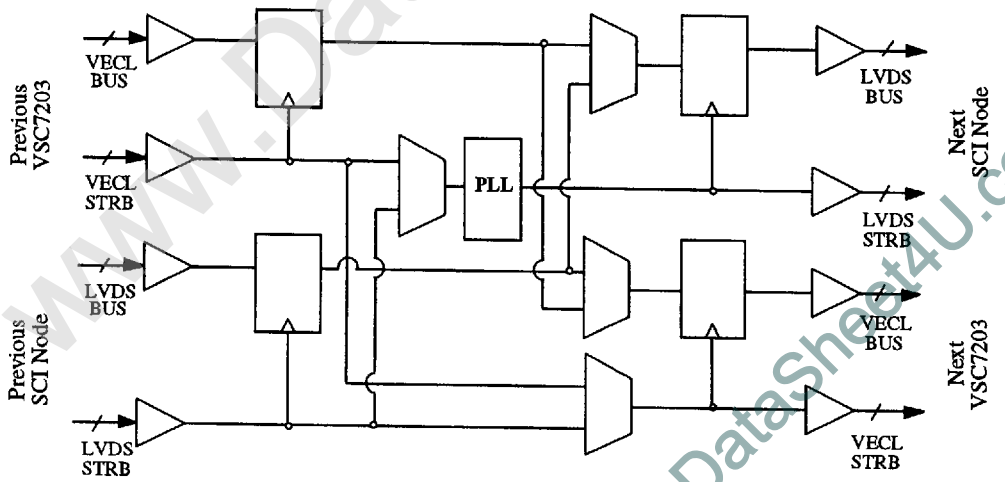
This Node Bypass circuit is intended to serve the purpose of isolation of SCI nodes. Multiple copies of this circuit would be interposed in a SCI ringlet, as required, and in normal operation pass SCI packets from one node to another while introducing minimum latency.

A faulty node can be electronically bypassed by assertion of the proper control signals.

The LVDS input and output busses are intended to connect SCI nodes controlled by VSC7201A "Data Pump" circuits. The other input and output busses use level-shifted ECL signaling (VECL) and are intended to connect to other VSC7203 Node Bypass circuits.

The node bypass circuit uses the input strobe for each input port as the source for the clock driving the two register pipeline to the selected output port. An internal 1 GHz PLL regenerates the selected input clock phase so that an unlimited number of circuits can be interconnected.

VSC7203 Functional Block Diagram



Functional Description

The node bypass circuit is a switch that has two basic modes of operation: NORMAL and BYPASS mode. In NORMAL mode, SCI packets are transmitted from the SCI node to a node bypass circuit and from a node bypass circuit to the SCI node. In BYPASS mode, SCI packets are transmitted from node bypass circuit to node bypass circuit. While in BYPASS mode, SCI packets may be sent to an SCI node, to the node bypass circuit, and back to the same SCI node for diagnostic checking without interfering with ringlet operation.

The node bypass circuit also has two modes which control clock generation through the PLL, HALFSPD and CLKSEL. The HALFSPD bit, when set high, allows the node bypass circuit to be run at 500MB/s instead of 1GB/s. This operation allows the chip to be compatible with a broader range of SCI systems. Whether in full speed or half speed mode, the LVDS BUS is two bytes wide and the VECL BUS is four bytes wide. The CLKSEL allows the user to bypass the internally generated PLL clock and use an external clock, TSTCLK, to control the LVDS STRB output. When bypassing the PLL, the externally supplied clock should be set at 500MHz regardless of the speed mode chosen.

It should be noted when the PLL output clock is being selected that, to ensure proper operation, the VECL STRB or LVDS STRB must be supplied to the node bypass circuit uninterrupted. Periodic interruption of the strobe signal to the PLL will cause the PLL to lose frequency lock and result in improper circuit operation.

The truth table in Table 1 details the operation of the node bypass circuit. LDATA represents data that is coming from the SCI node, and VDATA represents data that is coming from another node bypass circuit. PLL OUT represents an LVDS STRB generated by the PLL, and TSTCLK represents an LVDS STRB generated by the externally supplied clock. Finally, LSTRB represents a strobe signal from the SCI node, and VSTRB represents a strobe signal from another node bypass circuit.

Table 1: Truth Table

Control Inputs			*Data Outputs*				
HALFSPD	*BYPASS*	*CLKSEL*	*LVDS BUS*	*LVDS STRB*	*VECL BUS*	*VECL STRB*	*STRB SPEED*
0	0	0	VDATA	PLL OUT	LDATA	LSTRB	250MHz
1	0	0	VDATA	PLL OUT	LDATA	LSTRB	125MHz
0	1	0	LDATA	PLL OUT	VDATA	VSTRB	250MHz
1	1	0	LDATA	PLL OUT	VDATA	VSTRB	125MHz
0	0	1	VDATA	TSTCLK/2	LDATA	LSTRB	250MHz
1	0	1	VDATA	TSTCLK/4	LDATA	LSTRB	125MHz
0	1	1	LDATA	TSTCLK/2	VDATA	VSTRB	250MHz
1	1	1	LDATA	TSTCLK/4	VDATA	VSTRB	125MHz

Figure 1: Vitesse SCI Chipset, Typical Four Node Application using VSC7201A and VSC7203

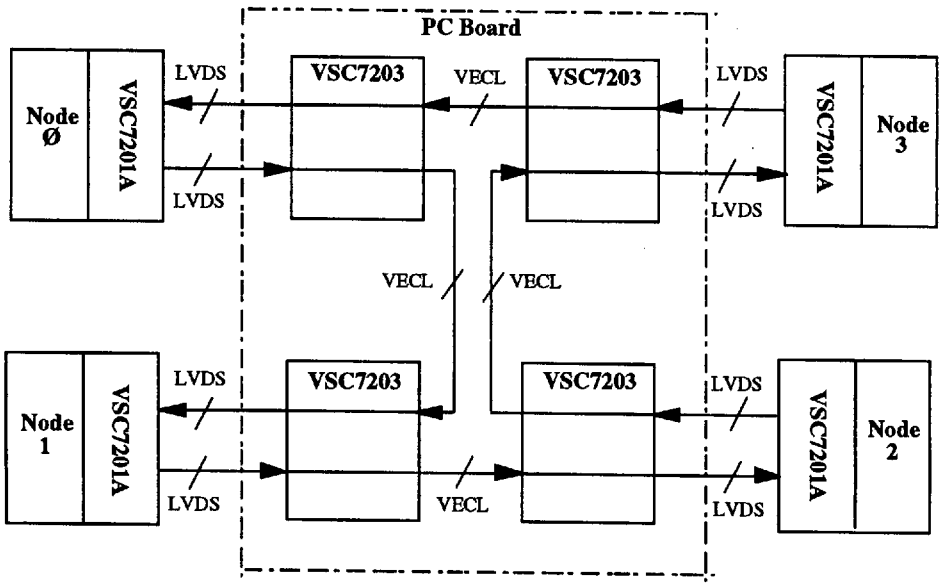


Figure 1 illustrates a typical application using the VSC7203. A 4 node ringlet is shown interconnected using VSC7203 Node Bypass Circuits. For example, in a multi-processor application, if each node contains 4 processors this configuration results in a 16 processor system. Of course this approach can be extended to a larger number by inserting additional nodes in the VECL path.

JTAG

The DataPump conforms to the IEEE Std 1149.1 Standard Test Access Port and Boundary Scan Architecture. This allows access to all the inputs and outputs of the VSC7203.

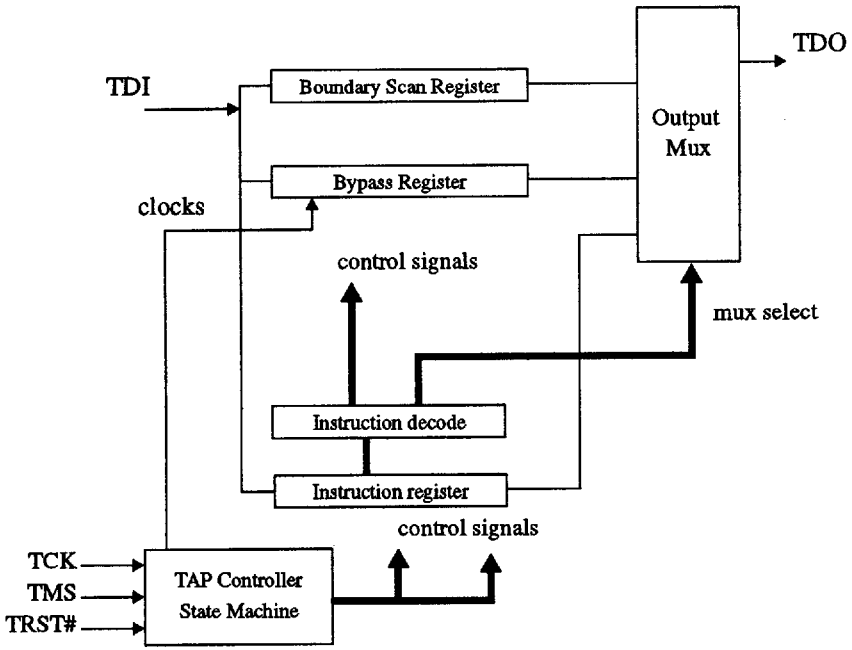
The Test Access Port uses the pins TCK, TMS, TRST, TDI, and TDO to perform serial shifting of data and control for testing the VSC7203.

A block diagram of the various scan chains accessible through JTAG is shown in Figure 2.

These registers operate like dual rank registers. That is, they have a shift register part and a parallel loading register part. In the case of boundary scan, the dual rank register is specified by the IEEE std.

The instruction register is a dual rank register made up of the shift register and a parallel load register. The outputs of the parallel load register actually provide the instruction data.

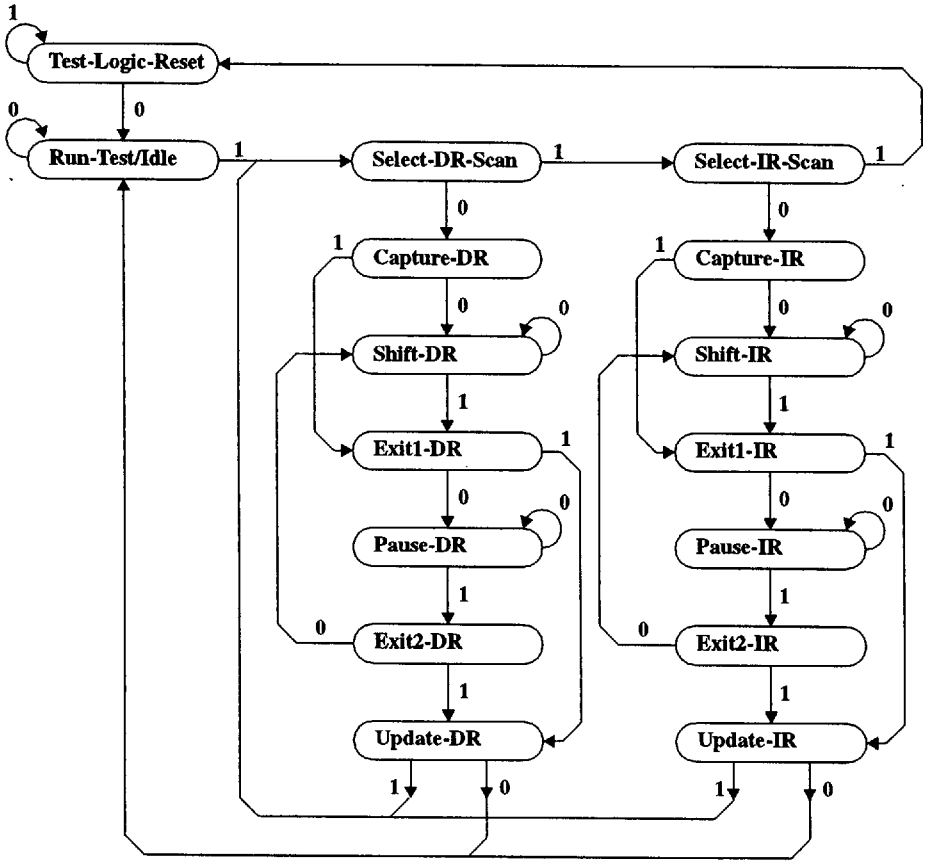
Figure 2: Scan Test Access Port Block Diagram



TAP Controller State Machine

The TAP controller state machine is clocked by TCK and controlled by TMS. It is asynchronously reset by TRST. Figure 3 shows the TAP controller state diagram. The TAP controller conforms to the specifications set forth in IEEE Std. 1149.1.

Figure 3: Test Access Port State Diagram



Note: The value (0 or 1) shown adjacent to each state transition represents the value of TMS sampled on the rising edge of TCK.

TAP Controller Instructions

Instructions are shifted into the instruction register using the IR (instruction register) state machine operations. The instructions supported include TAP mandatory BYPASS, SAMPLE/PRELOAD, and EXTEST. The instruction register is 8-bits long and each instruction code (inst[0:7] is given in hex form in Table 2. The shift order for inst[0:7] is inst0 to inst7. The basic instructions are listed in Table 2.

Table 2: TAP Controller Instructions

Instruction	*inst [7:0]*	*Description*
EXTEST	00_h	Provides external pin and board testing.
SAMPLE/ PRELOAD	$C0_h$	Allows sampling inputs and preloading outputs without affecting normal operation.
BYPASS	FF_h	Connects TDI to bypass register to TDO.

BYPASS Instruction

The BYPASS instruction selects the single stage BYPASS shift register to be connected between TDI and TDO. This allows for a minimum delay shift path through the VSC7203 in the Shift-DR state. Capture-DR and Update-DR have no effect during this instruction. Execution of this instruction does not affect normal VSC7203 operation.

EXTEST Instruction

The EXTEST instruction allows testing of off-chip connections to the I/O and PC-board interconnections. Data at the input pins is captured in the boundary scan shift register in the Capture-DR state. Data is shifted in the boundary scan shift register in the Shift-DR state. The boundary scan output registers are parallel loaded and the outputs of the DataPump driven on the rising edge of TCK in the Update-DR state.

Boundary Scan Register and Ordering

The boundary scan register consists of a bit for each I/O plus an extra bit which controls the capturing of output data by the boundary scan shift register during SAMPLE/PRELOAD. This bit is called ORCAPT. Table 3 on the following page gives the boundary scan ordering.

SAMPLE/PRELOAD Instruction

During SAMPLE/PRELOAD, inputs are registered into the boundary scan shift register in the Capture-DR state. When the ORCAPT bit is high (enabled), the outputs are registered into the boundary scan shift register as well. Otherwise, the boundary scan shift register does not load the output values when ORCAPT is low. Data is shifted in the boundary scan shift register in the Shift-DR state. The boundary scan output registers are parallel loaded and the outputs of the VSC7203 are driven on the rising edge of TCK on the Update-DR state.

Table 3: Boundary Scan Chain Ordering

Name	*Type*	*Position in B.S. Chain*
ORCAPT	internal	1
BYPASS	input	2
PSCISO	diff. output	3
PSCIFO	diff. output	4
PSCIDO[15:0]	diff. output	5-20
PSCISI	diff. input	21
PSCIFI	diff. input	22
PSCIDI[15:0]	diff. input	23-38
POCLK	diff. output	39
OFLAG[1:0]	output	40-41
ODATA[31:0]	output	42-73
PINCLK	diff. input	74
FLAG[1:0]	input	75, 76
DATA[31:0]	input	77-108

AC Characteristics

Table 4: VECL Port Specifications *(Over recommended operating conditions).*

Symbol	Parameter	Min	Max	Units
T_{PER}	INCLK period - full speed	4	-	ns
T_{PER}	INCLK period - half speed	8	-	ns
t_R	VECL input rise time	TBD	-	ps
t_F	VECL input fall time	TBD	-	ps
t_{PW}	INCLK pulse width - full speed	1.5	-	ns
t_{PW}	INCLK pulse-width - half speed	3	-	ns
t_{SU}	VECL input bus setup time	-0.40	-	ns
t_H	VECL input bus hold time	1.75	-	ns
t_{CK}	VECL clock to VECL output delay	TBD	-	ns
t_{CK}	LVDS clock to VECL output delay	.95	3.3	ns
t_R	VECL output rise time	TBD		
t_F	VECL output fall time	TBD		

Table 5: LVDS Port Specifications *(Over recommended operating conditions).*

Symbol	Parameter	Min	Max	Units
t_{R4}	LVDS output rise time	300	500	ps
t_{F4}	LVDS output fall time	300	500	ps
t_{OSKEW1}	LVDS output differential skew	-	50	ps
t_{OSKEW2}	LVDS output to output skew	-	100	ps
t_{OSKEW3}	LVDS output pulse distortion	-	200	ps
t_{R5}	LVDS input rise time	300	800	ps
t_{F5}	LVDS input fall time	300	800	ps
t_{ISKEW1}	LVDS input to input skew	-	500	ps
t_{CKO2}	PSCISO to PSCIDO and PSCIFO delay	1800	2200	ps

AC Timing Waveforms

Figure 4: Period, Pulse Width, Rise, and Fall Time Definitions

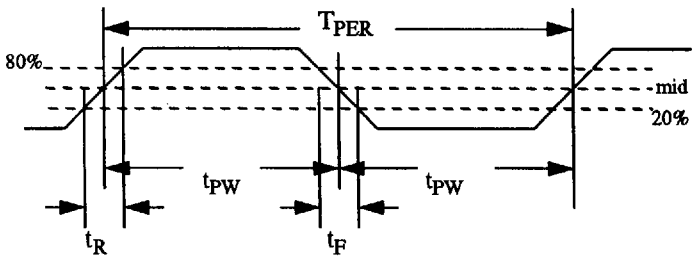
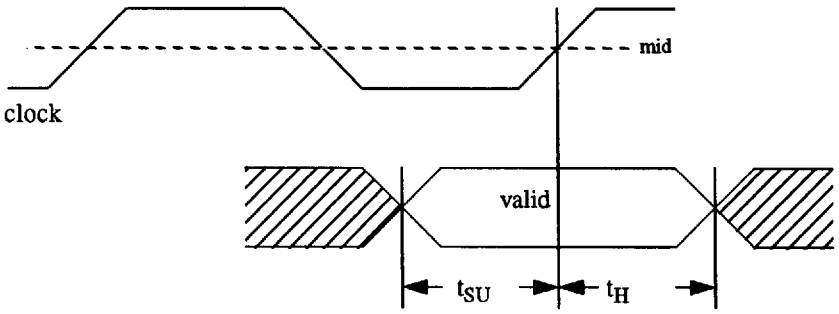


Figure 5: Setup and Hold Time Definitions



DC Characteristics

Table 6: Power Dissipation *(Over recommended operating conditions. VECL output open circuit, LVDS outputs terminated with 100 ohms.)*

Symbol	Parameter	Min	Typ	Max	Units
I_{MM}	Power supply current from V_{MM}	-	-	2.43	A
I_{TTL}	Power supply current from V_{TTL}	-	-	0.26	A
Pd	Total Power Dissipation	-	-	6.5	W

Table 7: TTL Input/Output *(Over recommended operating conditions.)*

Symbol	Parameter	Min	Typ	Max	Units
V_{OH}	Output high, I_{OH} = -2.4 mA	2.4	-	-	V
V_{OL}	Output low, I_{OL} = 8 mA	-	-	0.4	V
V_{IH}	Input high voltage [Not 5V tolerant]	2.0	-	V_{TTL} + 1.0	V
V_{IL}	Input low voltage	- 1.0	-	0.8	V
I_{IH}	Input high current, V_{IN} = 2.4 V	-	-	50	uA
I_{IL}	Input low current, V_{IN} = 0.4 V	1000	-	-	uA

Table 8: VECL Input/Output *(Over recommended operating conditions. Termination resistance = 50 ohms.)*

Symbol	Parameter	Min	Typ	Max	Units
V_{TT}	Termination voltage	-0.1	0	0.1	V
V_{OL}	Output low	0	-	0.38	V
V_{OH}	Output high	0.98	-	1.3	V
V_{IH}	Input high voltage	0.9	-	1.3	V
V_{IL}	Input low voltage	0	-	0.46	V
I_{IL}	Input low leakage current	-50	-	-	µA
I_{IH}	Input high leakage current	-	-	200	µA

Table 9: LVDS Output Driver *(Over recommended operating conditions.)*

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output voltage high	Rload = 100 ohms	1250	1475	mV
V_{OL}	Output voltage low	Rload = 100 ohms	925	1150	mV
V_{OD}	Output differential voltage	Rload = 100 ohms	250	400	mV
V_{OS}	Output offset voltage	Rload = 100 ohms	1125	1275	mV
dV_{OD}	Change in differential voltage between complementary states.	Rload = 100 ohms	-	25	mV
dV_{OS}	Change in offset voltage between complementary states.	Rload = 100 ohms	-	25	mV
R_O	Output impedance	Iload = 2 to 2.5 mA	40	60	ohms
dR_O	Ro mismatch between	Iload = 2 to 2.5 mA	-	10	%

Table 10: LVDS Input Receiver *(Over recommended operating conditions.)*

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Input voltage high	V_{ID}= 100mV	100	2200	mV
V_{IL}	Input voltage low	V_{ID}= 100mV	0	2100	mV
+/- V_{ID}	Input differential voltage		100	500	mV
V_{ICM}	Input voltage common mode	V_{ID}= V_{IDMIN}	50	2150	mV
		V_{ID}= V_{IDMAX}	250	1950	
R_{IN}	Input impedance	0 < V_{IN} < 2.4V	80	120	ohm

Absolute Maximum Ratings

Symbol	Rating	Limit
V_{MM}	+2 V power supply voltage	-0.5 to 2.6 V
V_{TTL}	+3.3 V power supply voltage	-0.5 to 4.0 V
Vin	Any pad voltage except LVDS outputs	-1.0 to V_{TTL} + 1.0 V
Vin	LVDS output voltage	-1.0 to V_{DD} + 1.0 V
I_{OUTT}	TTL output short circuit current	-50mA
Tc	Case temperature under bias	-55°C to +125°C
Tstg	Storage temperature	-65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{MM}	+2 V power supply voltage	1.9	2.0	2.1	V
V_{TTL}	+3.3 V power supply voltage	3.1	3.3	3.5	V
Tc	Operating case temperature	0	-	75	°C

Notes:

1) *CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*
2) *Vitesse guarantees the functional and parametric operation of the part under "Recommended Operating Conditions" except where specifically noted in the AC and DC Parametric Tables*

Package Pin Description

Signal	Type	Level	#Pins	Description
VSCIPNC	Input	ECL	1	Factory Test. Tie to V_{CC}
VSCOPNC	Output	ECL	1	Factory Test. Do not connect.
PSCIDI[15:0], NSCIDI[15:0]	Input	LVDS	32	SCI Link Data Bus, Complementary Pairs
PSCISI, NSCISI	Input	LVDS	2	SCI Link Strobe Input, Complementary Pairs
PSCIFI, NSCIFI	Input	LVDS	2	SCI Link Flag Input, Complementary Pairs
PSCIDO[15:0], NSCIDO[15:0]	Output	LVDS	32	SCI Link Data Bus, Complementary Pairs
PSCISO, NSCISO	Output	LVDS	2	SCI Link Strobe Output, Complementary Pairs
PSCIFO, NSCIFO	Output	LVDS	2	SCI Link Flag Output, Complementary Pairs
DATA[31:0]	Input	VECL	32	Port Input Data Bus
FLAG[1:0]	Input	VECL	2	Port Input Flag Bits
PINCLK, NINCLK	Input	VECL	2	Port Input Clock, Complementary Pairs
ODATA[31:0]	Output	VECL	32	Port Output Data Bus
OFLAG[1:0]	Output	VECL	2	Port Output Flag Bits
POCLK, NOCLK	Output	VECL	2	Port Output Clock, Complementary Pairs
CLKSEL	Input	VECL	1	Bypass PLL Selection Input
TSTCLK	Input	VECL	1	External Clock Input
HALFSPD	Input	VECL	1	Speed Selection
RESET	Input	TTL	1	Chip Reset Input
TMS	Input	TTL	1	JTAG Mode Select Input
TRST	Input	TTL	1	JTAG Reset, Active Low, Input
TDI	Input	TTL	1	JTAG Scan Input
TDO	Input	TTL	1	JTAG Scan Output
TCK	Input	TTL	1	JTAG Clock Input
BYPASS	Input	TTL	1	Chip Mode Select Input
VSCTE	Input	TTL	1	Factory Test. Tie to V_{CC}
VMM		Power	78	+2V Power Supply
VTTL		Power	4	+3.3V Power Supply (for TTL)
VCC		Ground	27	Ground
INC			31	Internally connected to an unused pad. Do not connect.
N/C			4	Not Connected

Package Pinout [by Pin Number]

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
A02	CLKSEL	AA17	VMM	C11	ODATA14
A03	INC	AA18	PSCIDO2	C12	VMM
A04	ODATA0	AA19	NSCIDO3	C13	ODATA18
A05	VMM	AA20	NSCIDO0	C14	ODATA22
A06	ODATA3	AA21	VMM	C15	ODATA23
A07	ODATA6	B01	INC	C16	VMM
A08	VMM	B02	TSTCLK	C17	ODATA27
A09	ODATA11	B03	VMM	C18	VMM
A10	ODATA12	B04	ODATA1	C19	ODATA31
A11	VMM	B05	ODATA2	C20	POCLK
A12	ODATA16	B06	ODATA4	C21	VMM
A13	ODATA20	B07	VMM	D01	NSCIDI15
A14	VMM	B08	ODATA7	D02	NSCIDI11
A15	ODATA24	B09	ODATA10	D03	PSCIDI11
A16	ODATA25	B10	ODATA13	D04	INC
A17	VMM	B11	ODATA15	D05	INC
A18	ODATA29	B12	ODATA17	D06	VCC
A19	OFLAG0	B13	ODATA19	D07	VCC
A20	OFLAG1	B14	ODATA21	D08	VCC
A21	VMM	B15	VMM	D09	VMM
AA01	VMM	B16	ODATA26	D10	VCC
AA02	INC	B17	ODATA28	D11	VMM
AA03	INC	B18	ODATA30	D12	VCC
AA04	NSCIDO15	B19	VMM	D13	VMM
AA05	VMM	B20	INC	D14	VCC
AA06	NSCIDO9	B21	NOCLK	D15	VCC
AA07	PSCIDO9	C01	VMM	D16	VCC
AA08	VMM	C02	INC	D17	INC
AA09	NSCIDO14	C03	HALFSPD	D18	INC
AA10	PSCIDO14	C04	VMM	D19	NINCLK
AA11	VMM	C05	INC	D20	PINCLK
AA12	NSCISO	C06	VMM	D21	FLAGI
AA13	PSCISO	C07	ODATA5	E01	VSCTE
AA14	VMM	C08	ODATA8	E02	VMM
AA15	NSCIDO6	C09	ODATA9	E03	PSCIDI15
AA16	PSCIDO6	C10	VMM	E04	NC

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
E05	VMM	H05	VCC	N03	VMM
E06	VTTL	H17	VCC	N04	PSCIDI2
E07	VTTL	H18	DATA3	N18	DATA14
E08	VMM	H19	DATA5	N19	VMM
E09	VMM	H20	DATA27	N20	DATA18
E10	VMM	H21	DATA28	N21	DATA22
E12	VMM	J01	PSCIDI10	P01	NSCIDI4
E13	VMM	J02	NSCIDI14	P02	NSCIDI2
E14	VMM	J03	VMM	P03	PSCIDI3
E15	VMM	J04	NSCIDI8	P04	NSCIDI3
E16	VMM	J18	DATA6	P05	VCC
E17	VMM	J19	VMM	P17	VCC
E18	NC	J20	DATA25	P18	DATA15
E19	DATA1	J21	DATA26	P19	DATA16
E20	VMM	K01	PSCIFI	P20	DATA20
E21	DATA31	K02	NSCISI	P21	DATA19
F01	NSCIDI13	K03	PSCISI	R01	VMM
F02	NSCIDI9	K04	NSCIDI10	R02	INC
F03	INC	K18	DATA7	R03	NSCIDI1
F04	VMM	K19	DATA11	R04	NSCIDI0
F05	VCC	K20	DATA8	R18	INC
F17	VCC	K21	DATA23	R19	INC
F18	VMM	L02	VCC	R20	DATA17
F19	DATA0	L03	NSCIFI	R21	VMM
F20	DATA30	L04	PSCIDI7	T01	PSCIDI1
F21	FLAG0	L18	DATA10	T02	PSCIDI0
G01	VMM	L19	DATA9	T03	RESET
G02	INC	L20	VCC	T04	VMM
G03	PSCIDI13	M01	NSCIDI7	T05	VCC
G04	PSCIDI9	M02	PSCIDI6	T17	VCC
G18	DATA2	M03	NSCIDI6	T18	VMM
G19	DATA4	M04	PSCIDI5	T19	INC
G20	DATA29	M18	DATA13	T20	INC
G21	VMM	M19	DATA12	T21	INC
H01	PSCIDI14	M20	DATA21	U01	TCK
H02	PSCIDI8	M21	DATA24	U02	VMM
H03	NSCIDI12	N01	NSCIDI5	U03	TRST
H04	PSCIDI12	N02	PSCIDI4	U04	NC

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
U05	VCC	V12	VCC	W18	VMM
U06	VTTL	V13	VMM	W19	NSCIDO4
U07	VTTL	V14	VCC	W20	PSCIDO1
U08	VMM	V15	VCC	W21	VMM
U09	VMM	V16	VCC	Y01	INC
U10	VMM	V17	PSCIDO4	Y02	INC
U12	VMM	V18	INC	Y03	VMM
U13	VMM	V19	INC	Y04	NSCIDO11
U14	VMM	V20	INC	Y05	PSCIDO11
U15	VMM	V21	INC	Y06	INC
U16	VMM	W01	VMM	Y07	VMM
U17	VMM	W02	VSCOPNC	Y08	PSCIDO13
U18	NC	W03	TDO	Y09	PSCIDO12
U19	INC	W04	VMM	Y10	NSCIFO
U20	VMM	W05	INC	Y11	PSCIFO
U21	INC	W06	VMM	Y12	PSCIDO8
V01	TMS	W07	PSCIDO15	Y13	NSCIDO10
V02	TDI	W08	NSCIDO13	Y14	NSCIDO7
V03	BYPASS	W09	NSCIDO12	Y15	VMM
V04	VSCIPNC	W10	VMM	Y16	INC
V05	INC	W11	NSCIDO8	Y17	NSCIDO5
V06	VCC	W12	VMM	Y18	PSCIDO5
V07	VCC	W13	PSCIDO10	Y19	VMM
V08	VCC	W14	PSCIDO7	Y20	PSCIDO0
V09	VMM	W15	NSCIDO2	Y21	NSCIDO1
V10	VCC	W16	VMM		
V11	VMM	W17	PSCIDO3		

Preliminary Data Sheet

1 GByte/sec SCI Compliant Switch Node Bypass Circuit

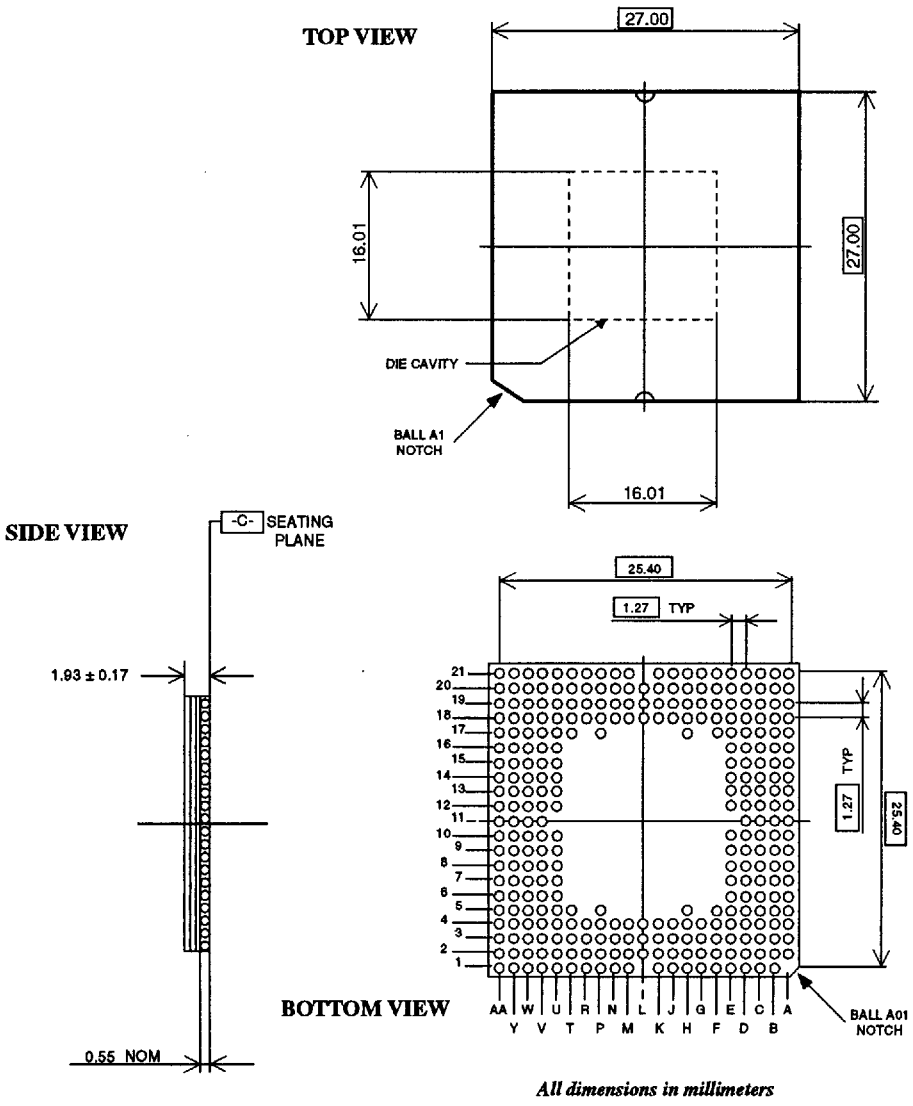
Package Pinout *[by Signal Name]*

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
BYPASS	V03	INC	A03	NSCIDI0	R04
CLKSEL	A02	INC	AA02	NSCIDI1	R03
DATA0	F19	INC	AA03	NSCIDI10	K04
DATA1	E19	INC	B01	NSCIDI11	D02
DATA10	L18	INC	B20	NSCIDI12	H03
DATA11	K19	INC	C02	NSCIDI13	F01
DATA12	M19	INC	C05	NSCIDI14	J02
DATA13	M18	INC	D04	NSCIDI15	D01
DATA14	N18	INC	D05	NSCIDI2	P02
DATA15	P18	INC	D17	NSCIDI3	P04
DATA16	P19	INC	D18	NSCIDI4	P01
DATA17	R20	INC	F03	NSCIDI5	N01
DATA18	N20	INC	G02	NSCIDI6	M03
DATA19	P21	INC	R02	NSCIDI7	M01
DATA2	G18	INC	R18	NSCIDI8	J04
DATA20	P20	INC	R19	NSCIDI9	F02
DATA21	M20	INC	T19	NSCIDO0	AA20
DATA22	N21	INC	T20	NSCIDO1	Y21
DATA23	K21	INC	T21	NSCIDO10	Y13
DATA24	M21	INC	U19	NSCIDO11	Y04
DATA25	J20	INC	U21	NSCIDO12	W09
DATA26	J21	INC	V05	NSCIDO13	W08
DATA27	H20	INC	V18	NSCIDO14	AA09
DATA28	H21	INC	V19	NSCIDO15	AA04
DATA29	G20	INC	V20	NSCIDO2	W15
DATA3	H18	INC	V21	NSCIDO3	AA19
DATA30	F20	INC	W05	NSCIDO4	W19
DATA31	E21	INC	Y01	NSCIDO5	Y17
DATA4	G19	INC	Y02	NSCIDO6	AA15
DATA5	H19	INC	Y06	NSCIDO7	Y14
DATA6	J18	INC	Y16	NSCIDO8	W11
DATA7	K18	NC	E04	NSCIDO9	AA06
DATA8	K20	NC	E18	NSCIFI	L03
DATA9	L19	NC	U04	NSCIFO	Y10
FLAG0	F21	NC	U18	NSCISI	K02
FLAG1	D21	NINCLK	D19	NSCISO	AA12
HALFSPD	C03	NOCLK	B21	ODATA0	A04

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
ODATA1	B04	PSCIDI12	H04	VCC	D06
ODATA10	B09	PSCIDI13	G03	VCC	D07
ODATA11	A09	PSCIDI14	H01	VCC	D08
ODATA12	A10	PSCIDI15	E03	VCC	D10
ODATA13	B10	PSCIDI2	N04	VCC	D12
ODATA14	C11	PSCIDI3	P03	VCC	D14
ODATA15	B11	PSCIDI4	N02	VCC	D15
ODATA16	A12	PSCIDI5	M04	VCC	D16
ODATA17	B12	PSCIDI6	M02	VCC	F05
ODATA18	C13	PSCIDI7	L04	VCC	F17
ODATA19	B13	PSCIDI8	H02	VCC	H05
ODATA2	B05	PSCIDI9	G04	VCC	H17
ODATA20	A13	PSCIDO0	Y20	VCC	L02
ODATA21	B14	PSCIDO1	W20	VCC	L20
ODATA22	C14	PSCIDO10	W13	VCC	P05
ODATA23	C15	PSCIDO11	Y05	VCC	P17
ODATA24	A15	PSCIDO12	Y09	VCC	T05
ODATA25	A16	PSCIDO13	Y08	VCC	T17
ODATA26	B16	PSCIDO14	AA10	VCC	U05
ODATA27	C17	PSCIDO15	W07	VCC	V06
ODATA28	B17	PSCIDO2	AA18	VCC	V07
ODATA29	A18	PSCIDO3	W17	VCC	V08
ODATA3	A06	PSCIDO4	V17	VCC	V10
ODATA30	B18	PSCIDO5	Y18	VCC	V12
ODATA31	C19	PSCIDO6	AA16	VCC	V14
ODATA4	B06	PSCIDO7	W14	VCC	V15
ODATA5	C07	PSCIDO8	Y12	VCC	V16
ODATA6	A07	PSCIDO9	AA07	VMM	A05
ODATA7	B08	PSCIFI	K01	VMM	A08
ODATA8	C08	PSCIFO	Y11	VMM	A11
ODATA9	C09	PSCISI	K03	VMM	A14
OFLAG0	A19	PSCISO	AA13	VMM	A17
OFLAG1	A20	RESET	T03	VMM	A21
PINCLK	D20	TCK	U01	VMM	AA01
POCLK	C20	TDI	V02	VMM	AA05
PSCIDI0	T02	TDO	W03	VMM	AA08
PSCIDI1	T01	TMS	V01	VMM	AA11
PSCIDI10	J01	TRST	U03	VMM	AA14
PSCIDI11	D03	TSTCLK	B02	VMM	AA17

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
VMM	AA21	VMM	E16	VMM	U20
VMM	B03	VMM	E17	VMM	V09
VMM	B07	VMM	E20	VMM	V11
VMM	B15	VMM	F04	VMM	V13
VMM	B19	VMM	F18	VMM	W01
VMM	C01	VMM	G01	VMM	W04
VMM	C04	VMM	G21	VMM	W06
VMM	C06	VMM	J03	VMM	W10
VMM	C10	VMM	J19	VMM	W12
VMM	C12	VMM	N03	VMM	W16
VMM	C16	VMM	N19	VMM	W18
VMM	C18	VMM	R01	VMM	W21
VMM	C21	VMM	R21	VMM	Y03
VMM	D09	VMM	T04	VMM	Y07
VMM	D11	VMM	T18	VMM	Y15
VMM	D13	VMM	U02	VMM	Y19
VMM	E02	VMM	U08	VSCIPNC	V04
VMM	E05	VMM	U09	VSCOPNC	W02
VMM	E08	VMM	U10	VSCTE	E01
VMM	E09	VMM	U12	VTTL	E06
VMM	E10	VMM	U13	VTTL	E07
VMM	E12	VMM	U14	VTTL	U06
VMM	E13	VMM	U15	VTTL	U07
VMM	E14	VMM	U16		
VMM	E15	VMM	U17		

Package Information



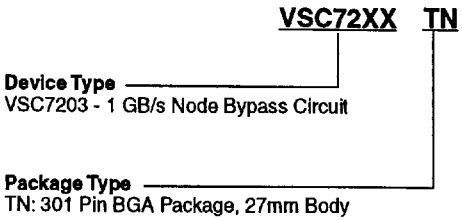
All dimensions in millimeters

Preliminary Data Sheet

1 GByte/sec SCI Compliant Switch Node Bypass Circuit

Ordering Information

The order number for this product is formed by a combination of the device number and package type.



Notice

This document contains information on products that are in the preproduction phase of development. The information contained in this document is based on test results and initial product characterization. Characteristic data and other specifications are subject to change without notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing orders.

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