AN1327/D

Very Wide Input Voltage Range, Off-Line Flyback Switching Power Supply

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APPLICATION NOTE

One of the many problems besetting the power supply designer today is being able to design a switching power supply that is able to operate in all the power systems within their international marketplaces. Forward-mode switching power supplies typically operate over a single power system's range of voltage, that is, 90 to 130 VAC or 200 to 270 VAC. Boost-mode converters can just make the range of 90 to 270 VAC. Any higher input voltages would then require a different design.

This leads companies to create products targeted at specific marketplaces, which can be costly, or to have their customers arrange jumpers to accommodate their power system which can be annoying or lead to costly errors.

Added to this are those industrial companies which may not only have their products reside on residential power systems but also have the varied international industrial power systems. This means that a single product family might have to operate from an input voltage of 90 to 600 VAC, well beyond the residential limits of 90 to 270 VAC.

This paper reviews one method of enabling a discontinuous-mode flyback converter to operate beyond its traditional range of input voltage of 3:1 to a range of more than 6.6:1 without affecting the reliability of its operation. This is done by changing its mode of operation and the use of recently available power MOSFETs with breakdown voltage ratings of 1,200 V.
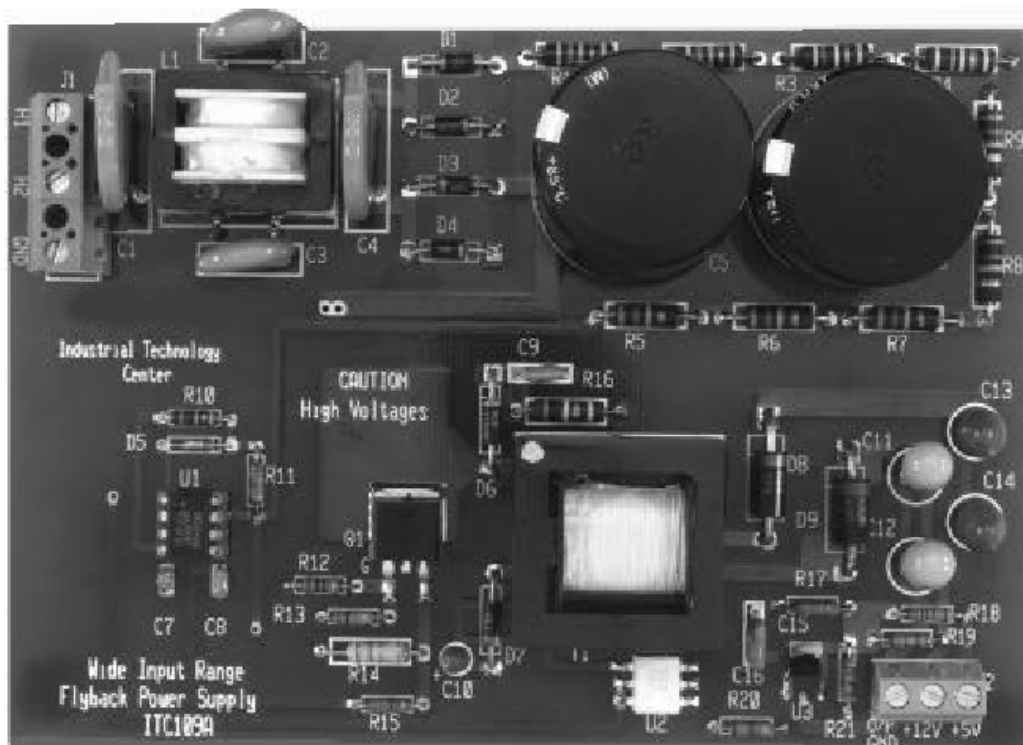

Figure 1. The Wide Input Range Flyback Power Supply Demonstration Board

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A Summary of the Operation of Fixed Frequency Flyback Converters

The most common topology for those applications less than 150 W has been the fixed frequency, current-mode controlled, flyback converter. Its block diagram can be seen in Figure 2.
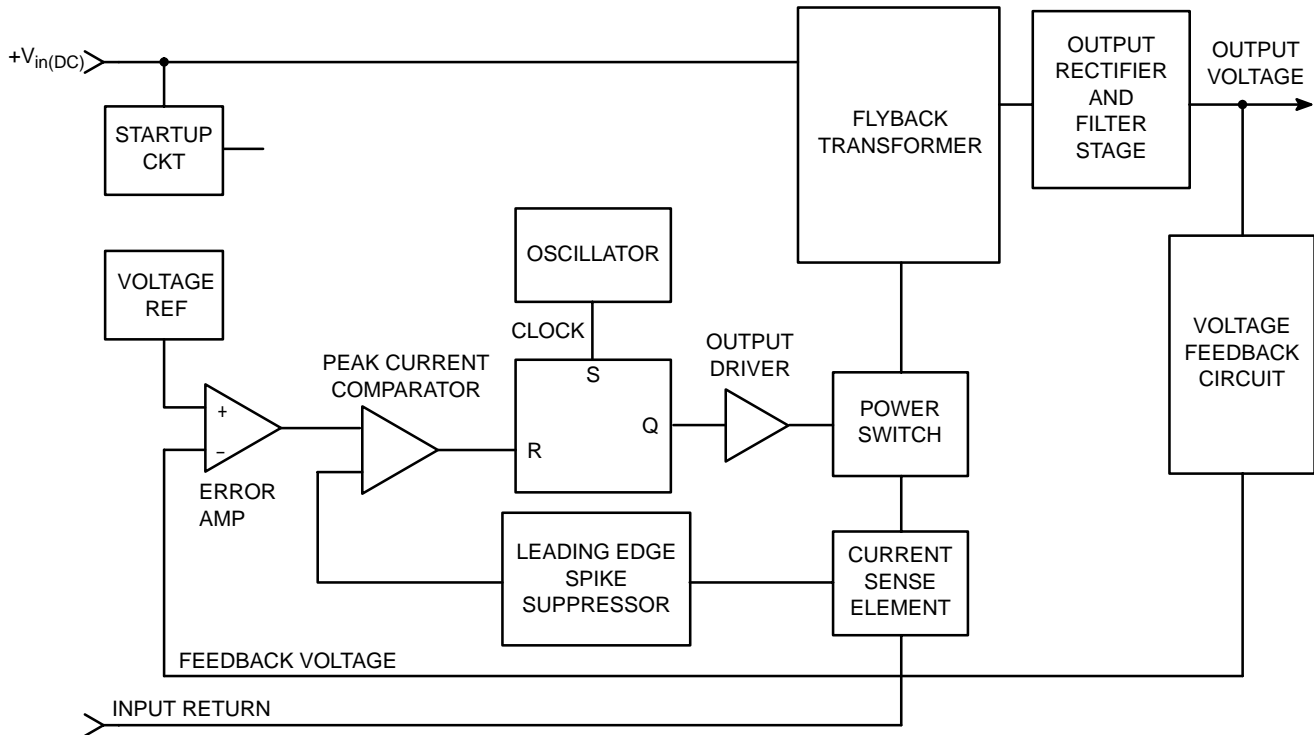

Figure 2. Block Diagram of a Fixed Frequency Current-Mode, Flyback Converter

Here a fixed frequency oscillator initiates a power switch conduction period which is terminated by either the current within the power switch reaching a predetermined limit as set by the error amplifier or the oscillator terminating the period and initiating the next power switch conduction period.

A representative flyback converter can be seen in Figure 3.

Figure 3. A Simplified Schematic of a Flyback Converter

The power switch essentially places the primary inductance of the flyback transformer across the input voltage source when it is turned on. The secondary is disconnected because the output rectifier (D) is reverse biased. The primary winding's current takes the form of a linear ramp starting from zero amps and whose peak value is given by:

$$i_{pk} = \frac{V_{in} \cdot T_{on}}{L_{pri}} \qquad \text{(eq. 1)}$$

The slope of the current ramp is V_{in}/L_{pri}.

The flyback topology, as with all boost-mode converters, operate under the principle of storing energy within the core material of the transformer. The energy stored during each conduction period is given by:

$$E_{sto} = \frac{L_{pri} \cdot i_{pk}^2}{2} \qquad \text{(eq. 2)}$$

To meet the short-term steady-state power demands of the load(s), the following relationship must be met:

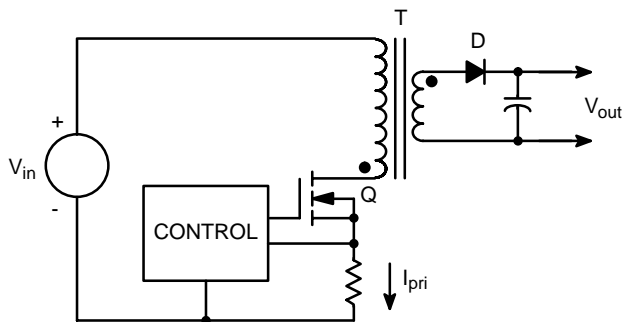$$P_{out} \leq \frac{f_{op} \cdot L_{pri} \cdot i_{pk}^2}{2} \qquad \text{(eq. 3)}$$

In reality, for any one output power, the current-mode controller strives to maintain a constant value for I_{pk} over the entire range of input voltages as visualized in Figure 4.
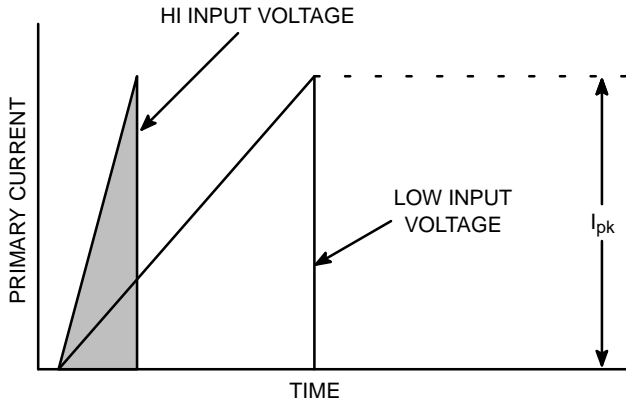

Figure 4. Peak Currents at Differing Input Voltages

The shortcoming arises in the output drivers of the typical current-mode control IC and the power switch. Typically a power MOSFET is used as the power switch in most modern flyback power supplies. At high input voltages, the on-time of the power switch becomes so short (300 - 600 nS) that the output driver cannot source enough instantaneous current to drive the MOSFET into a saturated condition before turning it back off. The effect is the power switch operates in the linear conduction mode during these short "on" pulses. This causes a drastic drop in power switch operating efficiency and jeopardizes the power supply's reliability.

The New Method of Control

By a very simple modification to the traditional fixed frequency current-mode controlled flyback converter design, one can greatly extend its operational input voltage range. The modifications make the control method one of variable on-time, and variable frequency. Figure 5 illustrates the newly added and redefined functional blocks of this new method of control.
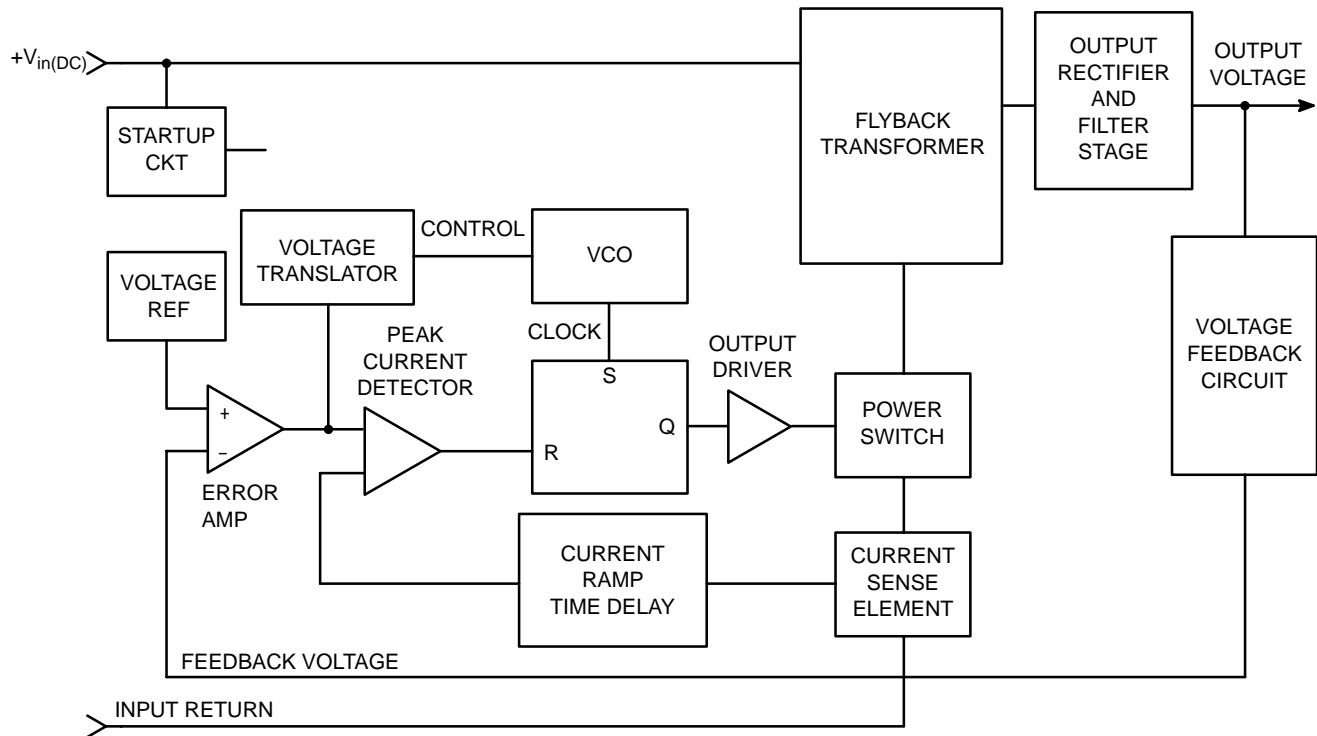

Figure 5. Block Diagram of the Wide Input Range, Flyback Converter

A VCO (voltage-controlled oscillator) is created by removing the timing capacitor's charging circuit from a fixed voltage or current source and placing it under the control of the error voltage. In the design example shown later, it means simply removing the timing resistor from the voltage reference and wiring it to a variable voltage created by the output of the error amplifier. A voltage translator is placed between the output of the error amplifier and the control input to the VCO. It consists of a simple biased 3.3 V zener diode so that the error amplifier may make use of its entire output voltage swing. The other new block is really a redefinition of an old familiar function - the leading edge spike filter from the current sensing element. Here, the formerly annoying parasitic of time lag serves an important function within the control algorithm. It now delays the actual current ramp prior to being sensed by the control IC. It allows the actual peak current to increase with increasing input voltages while the controller sees a lowering peak current needed by this control strategy. This will be discussed later.

The ultimate goal of the new control methodology is to force the on-time of the power switch to be greater than this minimum effective on-time over the power supply's entire line/load operating range. Its operation can be best understood by examining equation 3. The error amplifier/VCO section of the circuit lowers the operating frequency as the input voltage is increased. This requires the energy stored per conduction period to increase to meet the short-term power requirement of the output. This is done by extending the on-time of the power switch. If the key component parameters such as maximum operating flux density (B_{max}) of the transformer, the avalanche ratings of the diodes and power switch, and the current ratings of the output rectifiers are adequate, then no degradation in the reliable operation of the supply is experienced.

Its operation can be better defined by rearranging equation 3 and neglecting any power loss due to the inefficiency of the supply one gets:

$$i_{pk} = \sqrt{\frac{2\,P_{out}}{L_{pri} \cdot f_{(f(Ve))}}} \qquad \text{(eq. 4)}$$

where $f(f(Ve))$ is the controlled frequency of the power supply.

As one can see, the peak current is inversely proportional to the square root of the frequency of operation, since all the other terms are fixed in the short-term operation and by the circuit design.

By substituting equation 1 into equation 4 one further gets:

$$t_{on} = \frac{1}{V_{in}} \cdot \sqrt{\frac{2\,P_{out} \cdot L_{pri}}{f_{(f(Ve))}}} \qquad \text{(eq. 5)}$$

There are more unknowns than there are independent equations, but at the low input line voltage and at the rated output load, one can solve equation 5. The input voltage is known to be 125 VDC (90 VAC), the frequency will be at its highest point as designated by the designer, the on-time will be one-half of the entire operating period and the peak current will be calculated as it is in a common

fixed-frequency flyback converter. This will allow us to determine the appropriate value for the primary inductance.

In the sample design, the frequency of operation at the highest input voltage will drop to one-half from that at the lowest input voltage. Equation 4 then dictates:

$$i_{pk(hi)} \approx \sqrt{2}\, i_{pk(lo)} \qquad \text{(eq. 6)}$$

If the desired maximum operating flux density (B_{max}) is one-half the core material's saturation flux density at 100°C and at the high input line, then the operating flux density at the low input voltage should be:

$$B_{max(lo)} \approx \frac{B_{sat(min)}}{2\sqrt{2}} \qquad \text{(eq. 7)}$$

For most common ferrite materials such as 3C8, N27, or F, the operating flux density at low line will be at approximately 1,300 gauss. The B_{max} at the high input voltage will be no more than one-half the saturation flux density at 100°C.

The inductance can now be calculated by using equation 1 at the low input voltage, and an air gap calculated using any one of the common methods.

It is important to determine the secondary inductance such that the core's energy can be emptied as close to 50 percent duty-cycle ($1/f_{op}(hi)$) as possible. This will minimize the RMS currents to their lowest possible point over the entire operating range. The output peak current at any operating point is described as:

$$i_{pk(out)} \approx 2 \cdot I_{out(av)} \cdot T_{disch} \cdot f_{op} \qquad \text{(eq. 8)}$$

This would describe both the peak currents flowing through the output rectifiers and the peak ripple currents flowing into and out of the output filter capacitors. Within the sample design with one ampere rated outputs, at low line the peak-to-peak rectifier currents would be four times the average output current. At the high line, the peak-to-peak currents would be eight times the average output current for the rated output current.

The Wide-Range Flyback Converter Demonstration Board

The wide-input range off-line flyback converter described has the following maximum and performance ratings.

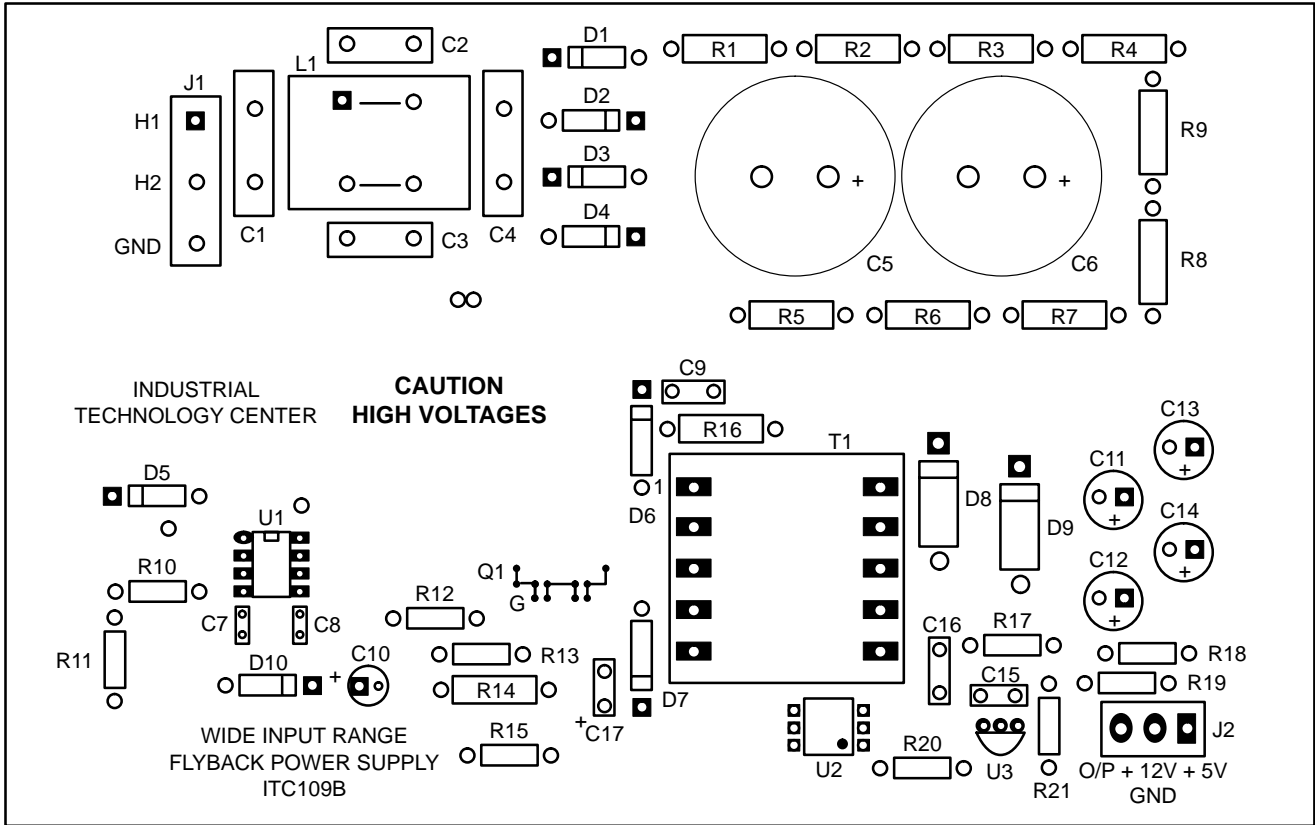|	
Output Power:	17 Watts
Outputs:	+5.0 Vdc @ 1.0 Amp Max
	+12 Vdc @ 1.0 Amp Max
Input Voltage Range:	90 V_{RMS} - 600 V_{RMS}
Maximum Input Voltage:	675 V_{RMS}

Figure 6. Printed Circuit Board Layout

Table 1. Parts List

Designator	Quantity	Value/Rating	Description
C1, C4	2	0.1 μF, 1.0 kV	Capacitor, Ceramic
C2, C3	2	0.0047 μF, 3.0 kV	Capacitor, Ceramic
C5, C6	2	100 μF, 450 V	Capacitor, Electrolytic
C7	1	220 pF, 50 V	Capacitor, Ceramic
C8	1	1000 pF, 50 kV	Capacitor, Ceramic
C9	1	1000 pF, 1.0 kV	Capacitor, Ceramic
C10	1	10 μF, 25 V	Capacitor, Tantalum
C11, C12	2	100 μF, 20 V	Capacitor, Tantalum
C13, 14	2	100 μF, 10 V	Capacitor, Tantalum
C15	1	1500 pF, 50 V	Capacitor, Ceramic
C16	1	1.3 μF, 50 V	Capacitor, Mylar
C17	1	0.22 μF, 35 V	Capacitor, Ceramic
D1-D4	4	1.0 A, 1.0 kV	Diode, 1N4007
D5	1	3.3 V, 500 mW	Zener Diode, 1N5226B
D6	1	1.0 A, 1.0 kV	Diode, UF, MUR1100E
D7	1	4.0 A, 300 V	Diode, UF, MUR430E
D8	1	3.0 A, 70 V	Diode, Schottky, MBR370
D9	1	1.0 A, 300 V	Diode, UF, MUR130E
D10	1	-	Diode, SIGNAL, 1N4148
J1	1	-	Connector
J2	1	-	Connector
L1	1	-	Coil Craft P/N E3493
Q1	1	3.0 A, 1.2 kV	MOSFET, MTB3N120E
R1-R4	4	470 kΩ, 1/2 W	Resistor
R5-R9	5	82 kΩ, 1/2 W	Resistor
R10	1	1.8 kΩ, 1/4 W	Resistor
R11	1	27 kΩ, 1/4 W	Resistor
R12	1	10 Ω, 1/4 W	Resistor
R13	1	1.0 kΩ, 1/4 W	Resistor
R14	1	1.2 Ω, 1/2 W	Resistor
R15	1	680 Ω, 1/4 W	Resistor
R16	1	100 kΩ, 1/2 W	Resistor
R17	1	7.5 kΩ, 1/4 W	Resistor
R18	1	3.57 kΩ, 1/4 W	Resistor
R19	1	32.4 kΩ, 1/4 W	Resistor
R20	1	120 Ω, 1/4 W	Resistor
R21	1	2.49 kΩ, 1/4 W	Resistor
T1	1	Transformer	Cramer, CSM, 3015-027
U1	1	-	IC, UC3845B
U2	1	-	Optoisolator, MOC8102
U3	1	-	IC, TL431CLP

Figure 7. AC Input/Filter Circuit Section

Figure 8. DC/DC Converter Circuit Section

Design of the Wide Input Range Flyback Converter

Predesign Considerations

Output Power:

P_o $= (5.0 \text{ V})(1.0 \text{ A}) + (12 \text{ V})(1.0 \text{ A}) = 17 \text{ Watts}$

DC Input Voltages:

$V_{in(low)}$ $= 1.414 \cdot V_{in\text{-}ac(low)}$
    $= 1.414(90 \text{ VAC}) = 127 \text{ VDC}$

$V_{in(hi)}$ $= 1.414 \cdot V_{in(hi)}$
    $= 1.414(600 \text{ VAC}) = 854 \text{ VDC}$

Maximum Average Input:

Current:

$I_{in\text{-}av(max)} = P_{out}/(\text{eff} \cdot V_{in(min)})$
    $= (17 \text{ W})/(0.8)(127 \text{ VDC})$
    $= 167 \text{ mA}$

NOTE: The primary winding's AWG should be #30 AWG.

Nominal Peak Current:

I_{pk} $= 5.5 \cdot P_{out}/V_{in(min)}$
    $= 5.5(17 \text{ W})/127 \text{ V} = 0.74 \text{ Amps}$

The desired maximum frequency of operation is 140 kHz.

Designing the Transformer

After reviewing the core sizing information provided by the various core manufacturers, it is decided that an E-E core of about 1.2 inches (30.5 mm) on a side will adequately fit the windings and insulation needed by this application. This corresponds to a Magnetics Inc. part number 43007-EC core (or Philips 782E272 (E 30)). The core material should be a Magnetics P, F or N material or Philips 3C85 or 3F3 material. A Magnetics part number F-43007-EC will be used.

Calculating the primary inductance needed for this application:

$$L_{pri} = \frac{\partial \text{ max } V_{in(min)}}{I_{pk}f \text{ max}}$$

(eq. 9)

$$= \frac{0.5(127 \text{ V})}{(0.82 \text{ A})(140 \text{ kHz})} = 553 \text{ } \mu\text{H}$$

Using equation 6, one gets the maximum operating flux density at the low input voltage of:

$$B_{max(lo)} \approx \frac{3500 \text{ G}}{2\sqrt{2}} = 1237 \text{ G}$$

(eq. 10)

The minimum length of the airgap for the core is then:

$$l_g = \frac{0.4 \text{ } \pi \text{ } L_{pri}i_{pk}^2 10^8}{A_C B_{max}^2}$$

(eq. 11)

$$= \frac{0.4 \text{ } \pi \text{ } (553 \text{ } \mu\text{H})(0.82 \text{ A})^2 \text{ } 10^8}{(0.6 \text{ cm}^2)(1300 \text{ G})^2} = 0.046 \text{ cm or } 18 \text{ mils}$$

An airgap that produces an A_L of 100 mH/1000T is larger than this, so that is what is used.

The number of turns needed to produce the required primary inductance is:

$$N_{pri} = 1000 \sqrt{\frac{L_{pri}}{A_L}}$$

(eq. 12)

$$= 1000 \sqrt{\frac{0.553 \text{ mH}}{100 \text{ mH}}} = 74.4 \text{ turns, make 74 turns}$$

The number of turns needed by the +12 V secondary, and assuming ultrafast recovery rectifier is:

$$N_{sec} = \frac{(V_{out} + V_{fwd})(1 - \partial \text{ max}) \cdot N_{pri}}{\partial \text{ max} \cdot V_{in(min)}}$$

(eq. 13)

$$= \frac{(12 \text{ V} + 0.9 \text{ V})(0.5)(74T)}{(0.5)(127 \text{ VDC})} = 7.5 \text{ turns, make 8 turns}$$

The auxiliary winding to power the control IC is also +12 V, so it will have the same number of turns.

The number of turns needed for the +5.0 volt winding is:

$$N(+5) = \frac{(5 \text{ V} + 0.5 \text{ V})(8T)}{(12.9 \text{ V})} = 4 \text{ turns}$$

(eq. 14)

The amount of error between the actual transformer output voltages and the required output voltages are:

+5 V: +5.0 V
+12 V: +10.1 V after the rectifier drop.

Add one turn (9 turns) to the +12 V outputs. The resulting output voltage, including the rectifier drop is 11.5 volts.

The physical winding of the transformer is extremely important (refer to Figure 9). First, there are the creepage requirements (space between windings over surface) of the safety agencies. Secondly, with 850 volts across the primary winding at the high input voltage, the interlayer voltage could cause arcing between layers of the primary winding. A layer of Mylar tape must be placed between adjacent layers of the primary. The final transformer construction is given below.

Sizing the Output Filter Capacitors

Since this is a variable frequency system, all the calculations for the value of the output filter capacitors will be done at the lowest frequency since the ripple voltage will be greatest at this frequency. Since capacitor values are determined by the output current, and both the +5.0 V and the +12 V outputs have the same maximum output current rating, their capacitance values will be equal.

$$C_o \approx \frac{I_{o(max)}}{f_{est(min)} \cdot V_{ripple(max)}}$$

(eq. 15)

$$\approx \frac{(1 \text{ A})}{(70 \text{ kHz})(0.1 \text{ V})} = 142 \text{ } \mu\text{F}$$

Make the output capacitors two 100 µF capacitors placed in parallel for each output (C11 and C13, C13 and C14).

Designing the Voltage Feedback Section

The internal error amplifier in the UC3845 (U1) will not be used. The inverting input pin should be grounded to ensure that the output will be always high. The error amplifier function will be provided by a TL431 (U3) on the secondary being connected to the primary side via an optoisolator, the MOC8102 (U2).

The collector of the MOC8102 optoisolator represents the key control node for power supply. The value of the voltage at this node sets both the frequency of operation and the peak current flowing through the power switch during each cycle. The collector of the U2 will be connected to the compensation pin of the UC3845 which will directly set the peak current. Then a 3.3 volt zener diode (D5) will elevate this voltage to a higher voltage to set the frequency of the voltage controlled oscillator. Choosing the maximum

current from the output of the MOC8102 optoisolator to be 5.0 mA, an external resistor (R11) from the V_{CC} of the IC to the VCO input is needed. Its value is set when the MOC8102's output is at saturation and is:

$$R11 = (12\ V - 3.3\ V)/5\ mA = 1740\ ohms,\ make\ 1.8\ k$$

(eq. 16)

The MOC8102 has a C_{trr} of 100 percent. That makes the LED current 6.0 mA (5.0 mA from R10, 1.0 mA from pin 1 of U1). A margin of 30 percent should be added for variations in the gain of the optoisolator. That would make the LED current 8.0 mA.

The value of the current limiting resistor for the optoisolator LED (R20) is:

$$R20 = [5\ V - (V_{U3} + V_{LED})]/8\ mA$$
$$= 138\ ohms,\ make\ 120\ k$$

(eq. 17)
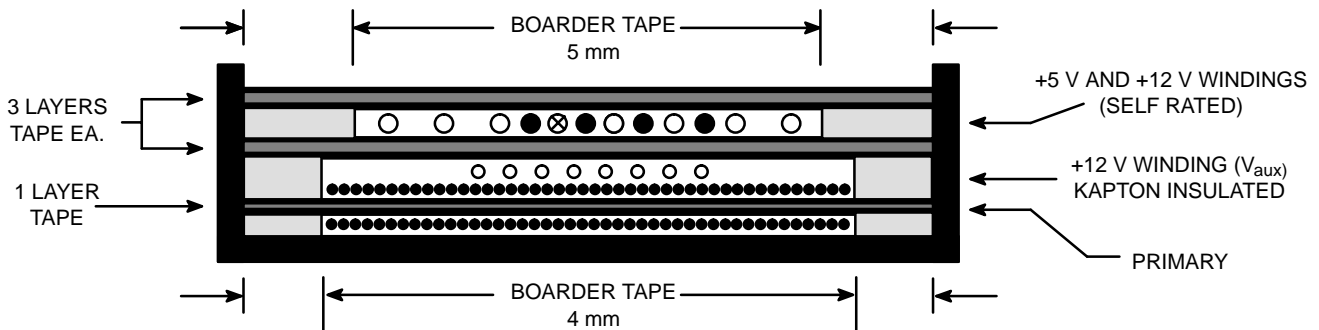
Figure 9. Construction of the Transformer

The lower resistor of the voltage sensing network (R21) is set by assuming a sense current. One milliamp yields 1.0 k ohm per volt, which is easy. So:

$$R21 = V_{ref}/I_{sense} = 2.5\ V/1\ mA$$
$$= 2.5\ k\ make\ 2.49\ k\ 1\%$$

(eq. 18)

Splitting the output voltage sensing between more than one output will improve the cross regulation of all the outputs. The +5.0 V output is usually connected to MCUs which are voltage sensitive. Usually, the loads connected to the +12 V output are less susceptible to voltage variations. Select the proportion of sense current to be 70 percent from the +5.0 V and 30 percent from the +12 V outputs. The value of the +5.0 V sense resistor (R18) is:

$$R18 = \frac{(5\ V - 2.5\ V)}{0.7(1\ mA)} = 3.57\ k,\ 1\%$$ (eq. 19)

The +12 V sense resistor (R19) is:

$$R19 = \frac{(12.2\ V - 2.5\ V)}{0.3(1\ mA)} = 32.3\ k$$
$$make\ it\ 32.4\ k,\ 1\%$$

(eq. 20)

Designing the Voltage Controlled Oscillator

One designs the VCO component values when the power supply is at the lowest input voltage. Here the frequency will

be at its highest and the duty cycle will be 50 percent. The VCO control node will be at its highest linear value which is 7.7 volts.

One starts by selecting the size of the timing capacitor (C_t, C7). This is done by referring to UC3845 data sheet, Figure 2 "deadtime vs. frequency." It is desired that the deadtime be a minimum, since the UC3845 is already 50 percent duty cycle limited. At an oscillator frequency of 280 kHz, which is divided by 2 for an operating frequency of 140 kHz, the largest capacitor that yields the least deadtime is approximately 220 pF.

Using Figure 1 from the UC3845 data sheet "Timing Resistor vs. Oscillator Frequency" and knowing the VCO control voltage will be 2.2 V higher than the +5.0 V reference assumed by the chart, one can "scale" Figure 1 so that the same charging current is flowing through the timing resistor (R10) but from the higher voltage source. So by multiplying the ratio of 7.7 V divided by 5.0 V by the value of the resultant resistor value from Figure 1, one gets the approximate final resistor value. Figure 1 results in a value of 18 k ohms for the timing resistor for a timing capacitor of 220 pF. The final value of R10 is then:

$$R_t = \frac{7.7\ V\ (18\ k)}{5.0\ V} = 27.7\ k\ make\ 27\ k$$ (eq. 21)

The lowest frequency that the power supply is capable occurs when the error amplifier is at its lowest output which is about 0.8 V. The lowest operating frequency would then be:

$$f_{low} = \frac{(0.8 \text{ V} + 3.3 \text{ V})}{7.7 \text{ V}} \cdot 140 \text{ kHz} = 75 \text{ kHz} \quad \text{(eq. 22)}$$

The Current Sense Resistor

Determining the value of the current sense resistor (R14), one uses the peak current determined in the predesign considerations and at the minimum input voltage. To keep the current-mode operation linear, the peak currents must be kept less than 1.0 volt in normal operation. So to find the current sensing resistor (R14) value:

$$R_{sc} = \frac{V_{sc}}{I_{pk}} = \frac{1.0 \text{ V}}{0.74 \text{ A}} = 1.35 \text{ } \Omega \text{ make } 1.2 \text{ ohms, } 1/2 \text{ W}$$

(eq. 23)

The Current Ramp Time Delay Circuit

This circuit is very important to the operation of the overall circuit. Aside from providing the usual spike elimination to the current comparator, it also provides a time delay function from the current sense resistor to the input to the current comparator. Although a wide range of resistor and capacitor values will work, some minimum time delay is required to avoid instabilities due to too short an on-time at the high range of input voltages.

One starts by selecting a value for the capacitor (C8). The common range of values for this function are 470 pF to 1000 pF. For this particular application a value of 1,000 pF was selected for C8. A good estimate of the time delay needed would be approximately 0.7 μS. This is also the approximate minimum on-time at the high input voltage. The value of the resistor (R15) would then be:

$$R_f = \frac{T_d}{C_f}$$

$$= \frac{(700 \text{ nS})}{(1000 \text{ pF})} = 700 \text{ } \Omega \text{ make } 680 \text{ ohms}$$

(eq. 24)

The Start-Up Circuit

A passive start-up circuit is used. That is, resistors will bring current from the input line to start-up the control IC. It is desired that a "hiccup" mode of overcurrent protection be implemented, which means that the amount of current that flows through the start-up circuit must be less than the current needed to run the control IC. The UC3845B uses approximately 10 mA during normal operation and draws between 0.3 to 0.5 mA in standby. The start-up energy will be stored in the 10 μF filter capacitor.

To meet the breakdown rating of the half watt resistors (approximately 250 V), a minimum of four resistors in series will be needed to accommodate the 854 VDC maximum input voltage. The total start-up resistance will be:

$$R_{st} = \frac{V_{in(min)}}{I_{start(min)}} = \frac{127 \text{ V}}{0.3 \text{ mA}} = 423 \text{ k} \quad \text{(eq. 25)}$$

Each resistor is then 110 k.
The power dissipated is:

$$P_D = \frac{(V_{in(max)})^2}{R_{st}} = \frac{(854)^2}{4(110 \text{ k})} = 1.66 \text{ W} \quad \text{(eq. 26)}$$

This makes the power dissipated in each resistor 0.41 watts. This is a little high, so place five resistors (R5-R9) each having a value of 82 k ohms and each will dissipate 0.36 watts which is below a 25 percent derating point.

The Voltage Feedback Loop Compensation

The output that is most heavily sensed is the +5.0 V output, so that will be the output that is used as the reference input for the feedback loop analysis.

The output filter pole at light load (0.1 A) of this output is:

$$f_{fp(+5)} = \frac{1}{2\pi R_o C_o}$$

$$= \frac{1}{2\pi (50 \text{ } \Omega)(200 \text{ μF})} = 15.9 \text{ Hz}$$

(eq. 27)

The +5.0 V output filter pole at rated load (1.0 A) is 159 Hz.

The zero contributed by the ESR of the output filter capacitors will be approximately 15 kHz.

The gain exhibited by the open loop power supply at the high input voltage will be:

$$A_{DC} = \frac{(V_{in} - V_{out})^2 \text{ N}_{sec}}{V_{in} \cdot V_e \cdot N_{pri}}$$

$$= \frac{(854 \text{ V} - 5 \text{ V})^2 \text{ 4T}}{(854 \text{ V})(1)(70\text{T})} = 48.3$$

(eq. 28)

or $G_{DC} = 33.6$ dB. This is the highest DC gain that will be exhibited by the open loop power supply and will reduce to 16.5 dB at the low input line. This will reduce the bandwidth of the closed loop power supply by almost a decade when going from high input line to low input line. This is marginally acceptable. By setting the widest allowable bandwidth at the high input line, then one can be assured of a reasonable bandwidth at the low input line. The maximum recommended bandwidth is approximately:

$$f_{xo} = \frac{f_{sw(min)}}{5} = \frac{75 \text{ kHz}}{5} = 15 \text{ kHz} \quad \text{(eq. 29)}$$

The gain needed to be contributed by the error amplifier to achieve this bandwidth is calculated at rated load because that will yield the widest bandwidth condition which is:

$$G_{xo} = 20 \text{ Log} \left(\frac{f_{xo}}{f_{fp}}\right) - G_{DC}$$

$$G_{xo} = 20 \text{ Log} \left(\frac{15 \text{ kHz}}{159 \text{ Hz}}\right) - 33.6 \text{ dB} = 5.9 \text{ dB}$$

(eq. 30)

The gain in absolute terms (needed later) is:

$$A_{XO} = 10 \left(\frac{G_{XO}}{20} \right)$$ (eq. 31)

$$A_{XO} = 10(5.9 \text{ dB}/20) = 1.97$$

Now the compensating circuit elements can be calculated.

$$C15 = \frac{1}{2 \cdot \pi \cdot A_{XO} \cdot R19 \cdot f_{XO}}$$

$$= \frac{1}{2 \cdot \pi (1.97)(3.57 \text{ k})(15 \text{ kHz})}$$ (eq. 32)

$$= 1500 \text{ pF}$$

$$R17 = A_{XO} \cdot R18$$

$$= (1.97)(3.57 \text{ k}) = 7033 \text{ ohms, make R20 7.5 k}$$

The compensating zero must be placed at or below the light load filter pole.

$$C16 = \frac{1}{2 \cdot \pi \cdot R20 \cdot f_{ze}}$$

$$= \frac{1}{2 \cdot \pi (7.5 \text{ k})(15.9 \text{ Hz})} = 1.3 \text{ μF}$$ (eq. 33)

Design of the Input Rectifier/Filter Circuit

This circuit provides EMI filtering, rectification and bulk energy storage for the power supply. It has some severe operating conditions it must withstand, such as very high AC and DC voltages at the high input voltage range. High voltage ratings for the rectifiers and bulk filter capacitors are needed. Also large creepage distances, the distance an arc must travel over a surface, must be maintained to meet the requirements of the safety regulatory agencies.

1N4007's will be used as the input rectifiers because of their 1000 V reverse voltage ratings and the average input current of the power supply is less than 1.0 amp.

The Bulk Input Filter Capacitor

The approximate value of capacitance needed is:

$$C_{in} \approx \frac{T_{off} \cdot I_{in - av(max)}}{V_{ripple}}$$

$$\approx \frac{(5 \text{ mS})(0.167 \text{ A})}{20 \text{ V}} = 42 \text{ μF}$$ (eq. 34)

make this two 100 μF, 450 VDC capacitors in series (C5 and C6).

The EMI Filter

A second order, common-mode filter is used. The lowest frequency of operation occurs at the low input voltages. The estimated lowest frequency of operation is 75 kHz. This is important to attenuate the switching noise sufficiently to pass EMI testing.

A good starting point is to assume that 24 dB of attenuation at 75 kHz is needed. That makes the corner frequency of the common-mode filter as:

$$f_C = f_{SW} \cdot 10 \left(\frac{Att}{40} \right)$$ (eq. 35)

where Att is the attenuation needed at the switching frequency in negative dB.

$$f_C = (75 \text{ kHz}) 10 \left(\frac{-24}{40} \right) = 18.8 \text{ kHz}$$ (eq. 36)

A damping factor of 0.707 or greater is good and it provides a -3.0 dB attenuation at the corner frequency and does not produce ringing in the filter reactances. Assume that the input line impedance is 50 ohms since the regulatory agencies use a LISN (Line Impedance Stabilization Network) which makes the line impedance equal this value. Calculating the values needed in the common-mode inductor (L1) and "X" capacitors (C1 and C4):

$$L = \frac{R_L \cdot \zeta}{\pi \cdot f_C} = \frac{(50)(0.707)}{\pi (18.8 \text{ kHz})} = 598 \text{ μH}$$

$$C = \frac{1}{(2\pi f_C)2L} = \frac{1}{[2\pi (18.8 \text{ kHz})]^2 (598 \text{ μH})}$$ (eq. 37)

$$= 0.1 \text{ μF}$$

Coilcraft offers off-the-shelf common-mode filter chokes (transformers) and the part number closest to this value is E3493. With this filter design a minimum of -40 dB between the frequencies of 500 kHz and 10 MHz can be expected. If later during the EMI testing stage, additional filtering is needed, a third order to the filter design will be added by using a differential-mode filter.

Post Design Modifications

It was found that the control circuitry drew more quiescent current than anticipated. That made the start-up voltage higher than desired. It was also found that the optoisolator's dark collector leakage current and the timing capacitor's leakage current were responsible for this behavior. D10 and C17 which isolated these elements behind a low reverse leakage diode during the start-up process were added.

Performance of the Sample Design

Output Regulation:

+5.0 V	-1.2%
+12 V	-1.5%

Input Regulation:

+5.0 V	+0.4%
+12 V	+0.5%

Output Ripple:

+5.0 V	100 mV (@ 90 VAC)
+12 V	130 mV (@ 90 VAC)

Figures 10 through 13 graphically represent some of the parameters of the evaluation board that are important to its operation. These parameters were measured at full-rated load for all of the outputs.
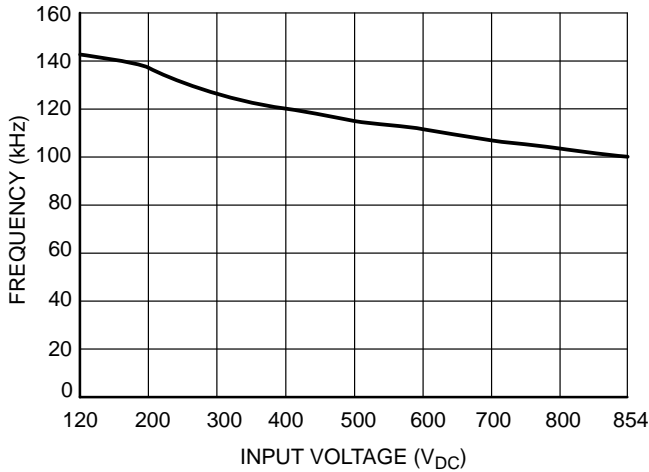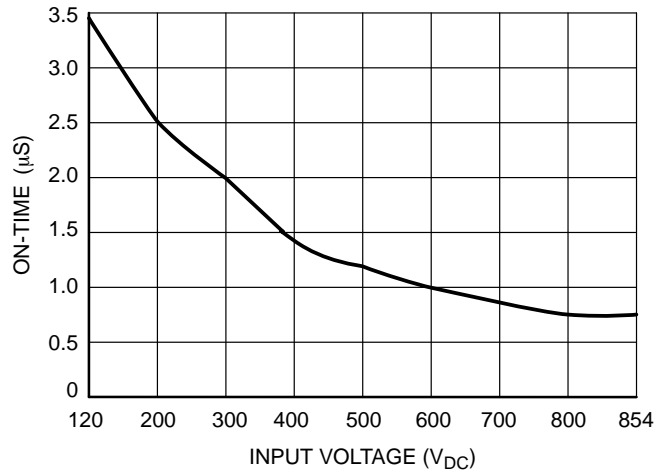

Figure 10. Frequency vs. Input Voltage
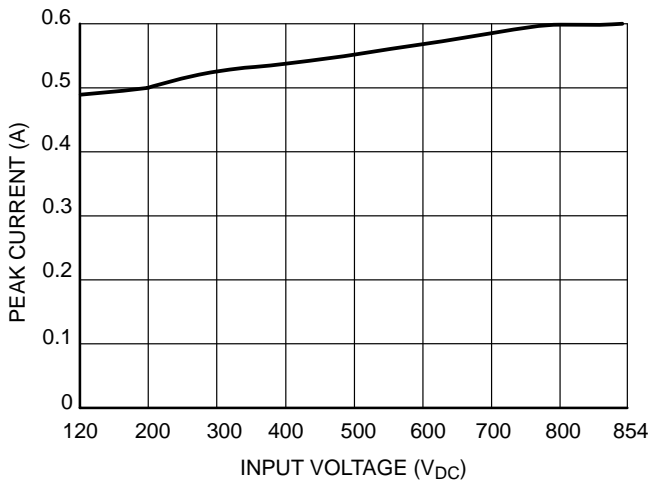

Figure 11. On-Time vs. Input Voltage

Figure 12. Actual Peak Current vs
Input Voltage

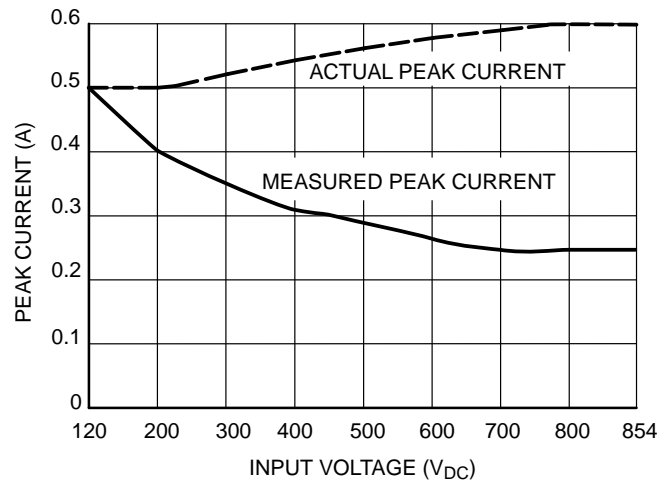Figure 13. Actual and Measured Peak Current
vs. Input Voltage