

TC5588P/J-15,-20,-25,-35

8,192 WORD × 8 BIT CMOS STATIC RAM

DESCRIPTION

The TC5588P/J is a 65,536 bits high speed static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit from provides high speed feature.

The TC5588P/J has low power feature with device control using Chip Enable ($\overline{CE1}/\overline{CE2}$), and has Output Enable Input (\overline{OE}) for fast memory access. Also the device power at memory access is reduced by automatic power down circuit form.

The TC5588P/J is suitable for use in cache memory where high speed is required, and high speed storage. All Inputs and Outputs are directly TTL compatible.

The TC5588P/J is moulded in 28 pin standard DIP and SOJ with 300 mil width for high density surface assembly.

FEATURES

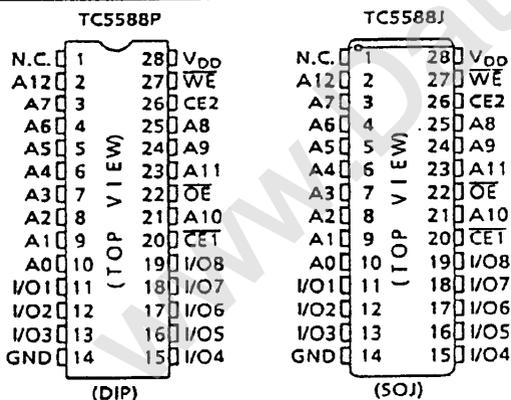
- Fast access time:

TC5588P/J-15	15ns (MAX.)
TC5588P/J-20	20ns (MAX.)
TC5588P/J-25	25ns (MAX.)
TC5588P/J-35	35ns (MAX.)
- Low power dissipation:

Operation	TC5588P/J-15	135mA (MAX.)
	TC5588P/J-20	115mA (MAX.)
	TC5588P/J-25	115mA (MAX.)
	TC5588P/J-35	115mA (MAX.)
Standby		1mA (MAX.)
- 5V single power supply : $5V \pm 10\%$
- Fully static operation
- Directly TTL compatible : All Input and Output
- Output buffer control : \overline{OE}
- Package

TC5588P	: DIP28-P-300B
TC5588J	: SOJ28-P-300A

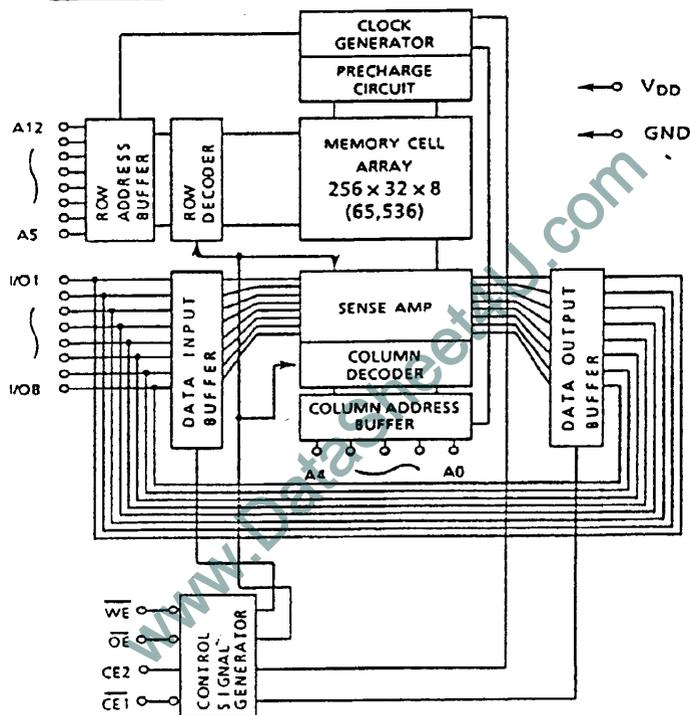
PIN CONNECTION



PIN NAMES

A0~A12	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
$\overline{CE1}, \overline{CE2}$	Chip Enable Inputs
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5~7.0	V
V _{IN}	Input Voltage	-2.0~7.0	V
V _{OUT}	Output Voltage	-0.5~V _{DD} +0.5	V
P _D	Power Dissipation	1.0	W
T _{solder}	Soldering Temperature · Time	260 · 10	°C · sec
T _{strg}	Storage Temperature	-65~150	°C
T _{oor}	Operating Temperature	-10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	-	V _{DD} +0.5	V
V _{IL}	Input Low Voltage	*-3.0	-	0.8	V

* Pulse width ≤ 10ns, DC: -0.5V (min)

DC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I _{IL}	Input Leakage Current	V _{IN} = 0~V _{DD}	-	-	±1	μA	
I _{OH}	Output High Current	V _{OH} = 2.4V	-4	-	-	mA	
I _{OL}	Output Low Current	V _{OL} = 0.4V	8	-	-	mA	
I _{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, V _{OUT} = 0~V _{DD}	-	-	±1	μA	
I _{DDO}	Operating Current	V _{DD} = 5.5V t _{cycle} = Min cycle $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ Other Inputs = V _{IH} /V _{IL} I _{OUT} = 0mA	-15	-	-	135	mA
			-20	-	-	-	
			-25	-	-	115	
			-35	-	-	-	
I _{DDs1}	Standby Current	V _{DD} = 5.5V t _{cycle} = Min cycle $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ Other Inputs = V _{IH} /V _{IL}	-	-	-	25	mA
			I _{DDs2} *	$\overline{CE1} = V_{DD} - 0.2V$ or $CE2 = 0.2V$ Other Inputs = V _{DD} - 0.2V or 0.2V	-	-	

*: In standby mode with $\overline{CE1} \geq V_{DD} - 0.2V$, these specification limits are guaranteed under the condition of $\overline{CE2} \geq V_{DD} - 0.2V$ or $CE2 \leq 0.2V$.

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	5	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	7	pF

NOTE : This parameter periodically sampled is not 100% tested.

AC CHARACTERISTICS (Ta = 0~70°C ⁽¹⁾, VDD = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC5588P/J-15		TC5588P/J-20		TC5588P/J-25		TC5588P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	15	-	20	-	25	-	35	-	ns
t _{ACC}	Address Access Time	-	15	-	20	-	25	-	35	
t _{CO1}	CE1 Access Time	-	15	-	20	-	25	-	35	
t _{CO2}	CE2 Access Time	-	15	-	20	-	25	-	35	
t _{OE}	OE Access Time	-	9	-	10	-	12	-	12	
t _{OH}	Output Data Hold Time From Address Change	5	-	5	-	5	-	5	-	
t _{COE}	Output Enable Time from CE1 or CE2	5	-	5	-	5	-	5	-	
t _{COO}	Output Disable Time from CE1 or CE2	-	6	-	6	-	6	-	6	
t _{OEE}	Output Enable Time from OE	0	-	0	-	0	-	0	-	
t _{ODO}	Output Disable Time from OE	-	5	-	5	-	5	-	5	
t _{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	0	-	
t _{PD}	Chip Deselection to Power Down Time	-	15	-	20	-	25	-	35	

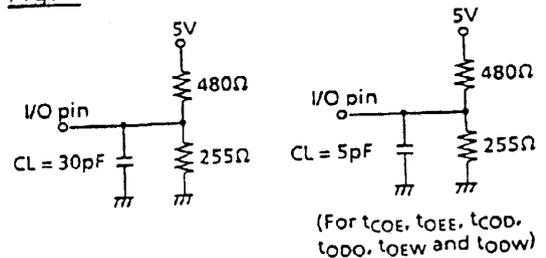
WRITE CYCLE

SYMBOL	PARAMETER	TC5588P/J-15		TC5588P/J-20		TC5588P/J-25		TC5588P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	15	-	20	-	25	-	35	-	ns
t _{CW}	Chip Enable to End of Write	12	-	13	-	15	-	15	-	
t _{AS}	Address Set Up Time	0	-	0	-	0	-	0	-	
t _{WP}	Write Pulse Width	12	-	13	-	15	-	15	-	
t _{WR}	Write Recovery Time	0	-	0	-	0	-	0	-	
t _{DS}	Data Set Up Time	9	-	10	-	12	-	12	-	
t _{DH}	Data Hold Time	0	-	0	-	0	-	0	-	
t _{OEW}	Output Enable Time from WE	0	-	0	-	0	-	0	-	
t _{ODW}	Output Disable Time from WE	-	6	-	6	-	6	-	6	

AC TEST CONDITIONS

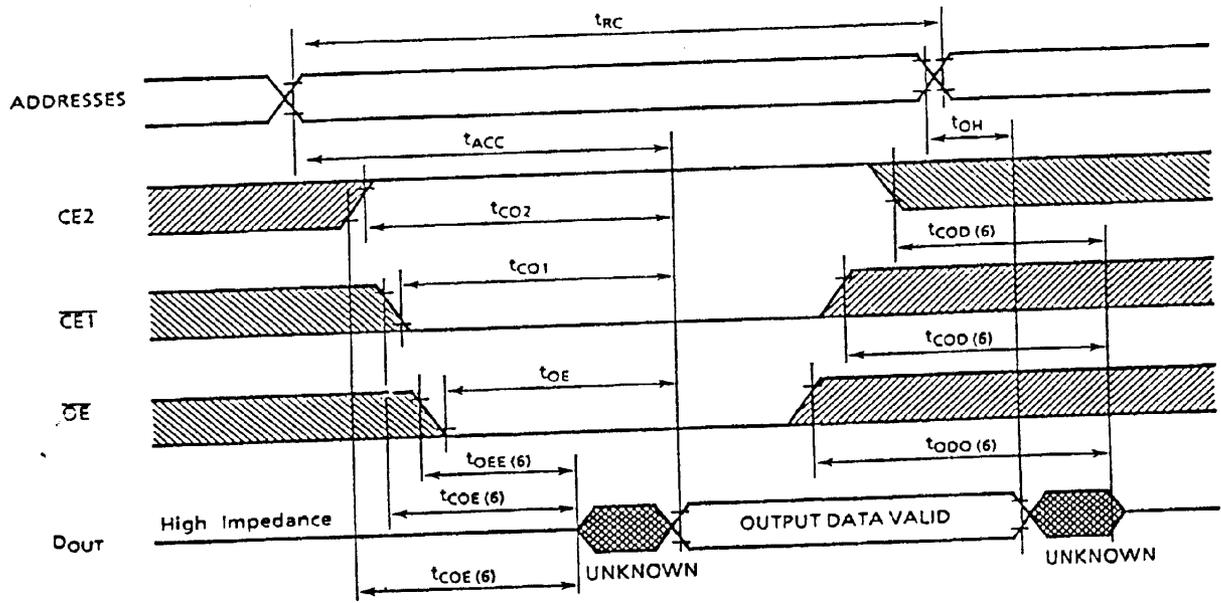
Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

Fig. 1

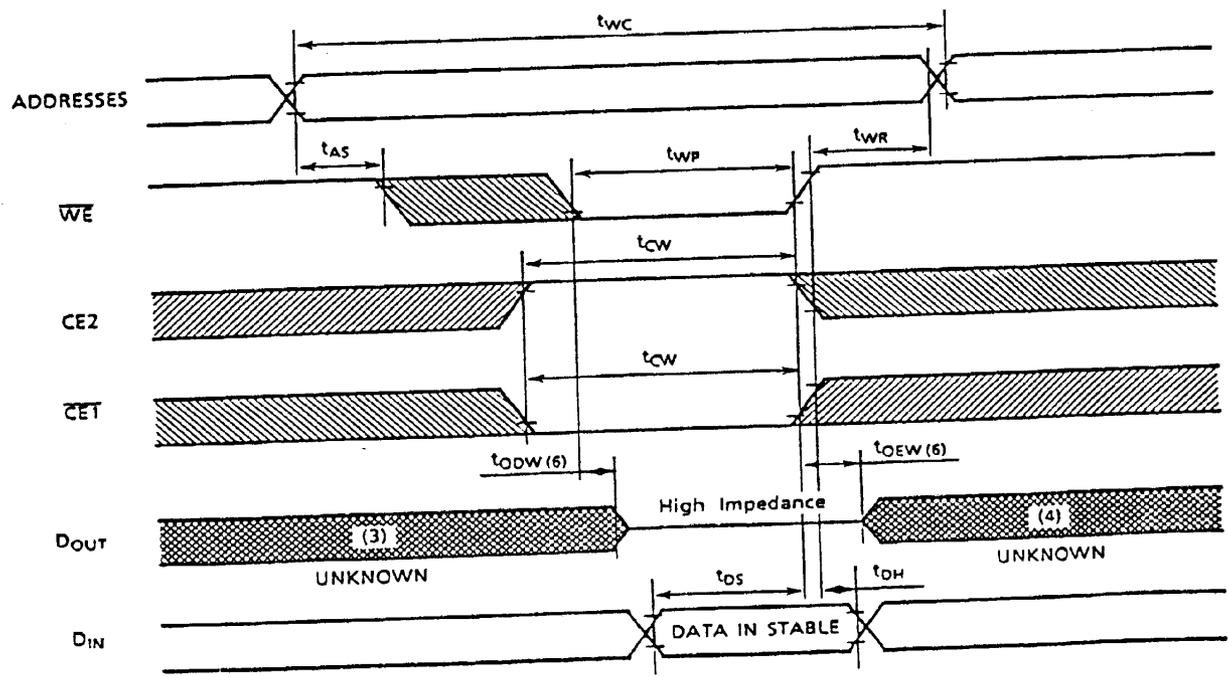


TIMING WAVEFORMS

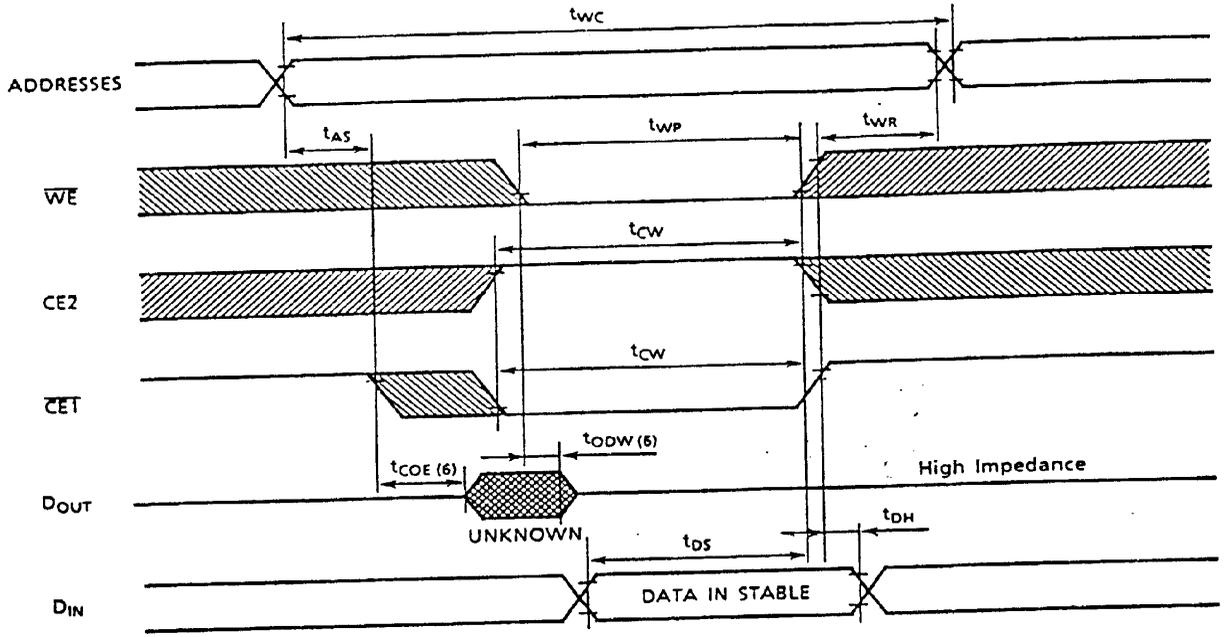
READ CYCLE (2)



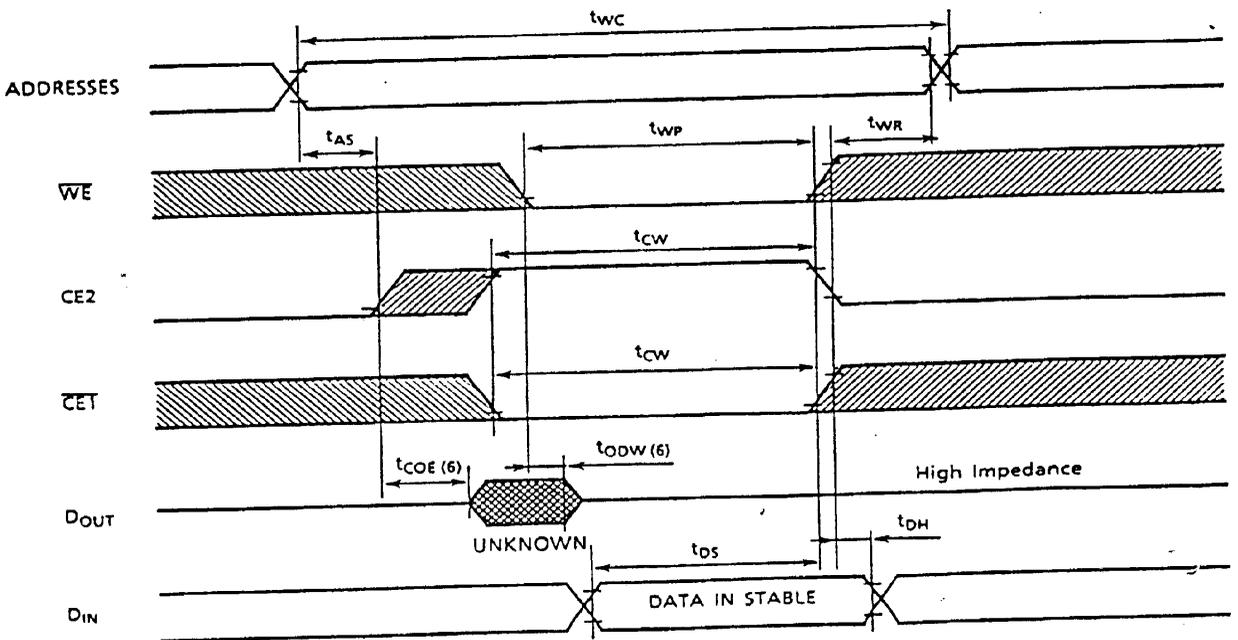
WRITE CYCLE 1 (5) (\overline{WE} Controlled Write)



WRITE CYCLE 2 (5) ($\overline{CE1}$ Controlled Write)



WRITE CYLCE 3 (5) ($CE2$ Controlled Write)

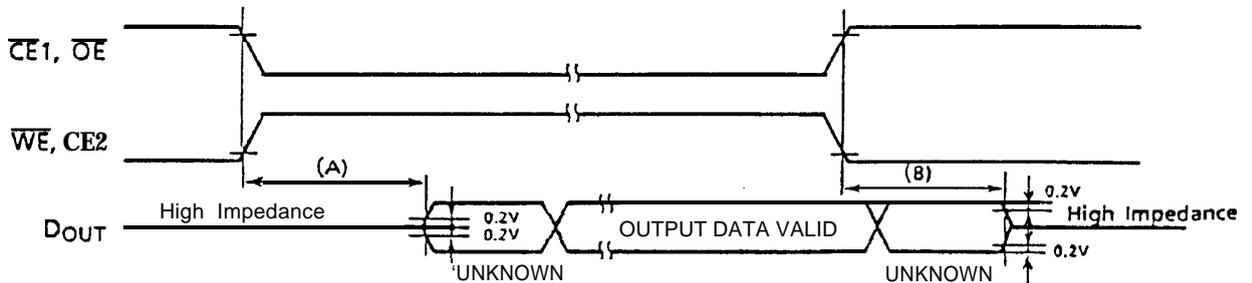


- NOTES: 1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is High for Read Cycle.
3. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after \overline{WE} Low transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to \overline{WE} High transition, Outputs remain in a high impedance state.
5. Assuming that \overline{OE} is High for Write Cycle, Outputs are in a high impedance state during this period.
6. These Parameters are specified as follows and measured by using the load shown in

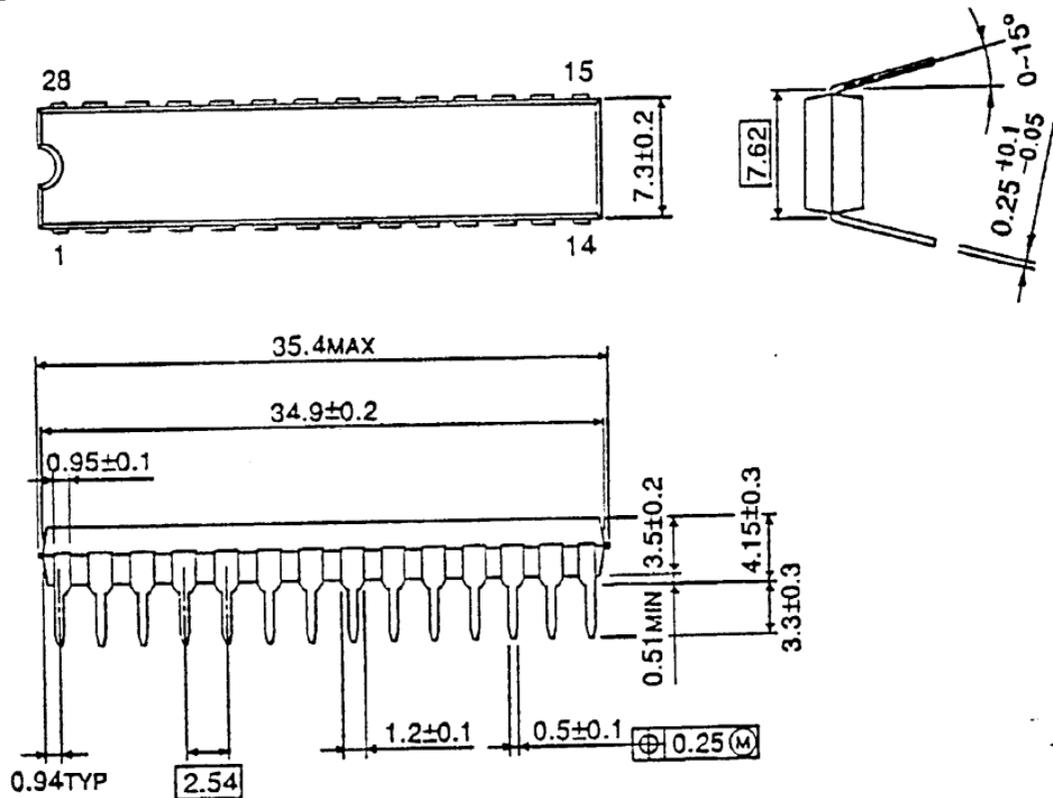
Fig. 1.

(A) $t_{COE}, t_{OEE}, t_{OE\overline{W}}$ Output Enable Time

(B) $t_{COD}, t_{ODO}, t_{OD\overline{W}}$ Output Disable Time



DIP28-P-300B



SOJ28-P-300A

