5-BIT REGISTERED TRANSCEIVER

SY100S891

FEATURES

- **25Ω cut-off bus outputs**
- **50Ω receiver outputs**
- **Transmit and receive registers with separate clocks**
- **1500ps max. delay from CLK_1 to Bus Outputs (BUS)**
- **1500ps max. delay from CLK_2 to Receiver Outputs (Q)**
- **Individual bus enable pins**
- **Internal 75KΩ input pull-down resistors**
- **Voltage and temperature compensation for improved noise immunity**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option: V_{EE} = –4.2V to –5.5V**
- **Available in 28-pin PLCC package**

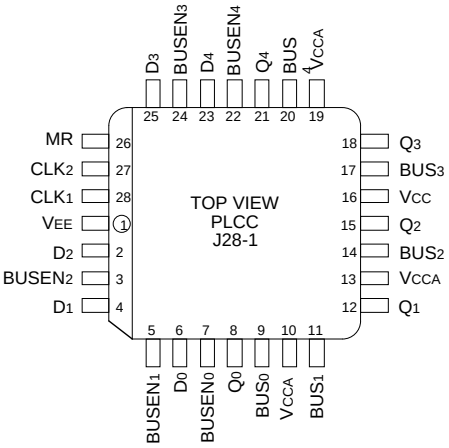
DESCRIPTION

The SY100S891 is a 5-bit registered transceiver containing five bus transceivers with both transmit and receive registers. The bus outputs (BUS_0 – BUS_4) are specified for driving a 25 ohm bus and the receive outputs (Q_0 – Q_4) are specified for driving a 50 ohm line. The bus outputs have a normal high level output voltage and a normal low level output voltage when the bus enable ($BUSEN_0$ – $BUSEN_4$) is high. However, the output is switched to a cut-off level when a bus-enable is low. This cut-off level is sufficiently low that a relatively high impedance is presented to the bus in order to minimize reflections. There is one bus-enable for each bus driver; a clock (CLK_1) which is common to all five bus driver registers; and a separate clock (CLK_2) which is common to all five receive registers. Data at the D inputs is clocked to the Bus register by a positive transition of CLK_1 and data on the bus is clocked into the Receiver register by a positive transition of CLK_2. A high on the Master Reset clears all registers.

PIN NAMES

Pin	Function
$BUSEN_{0–4}$	Bus Enable Inputs
D_0 – D_4	Data Inputs
CLK_1	Bus Driver Clock Input
CLK_2	Receive Register Clock
MR	Master Reset
Q_0 – Q_4	Bus Receive Outputs
$BUS_{0–4}$	Bus Outputs

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

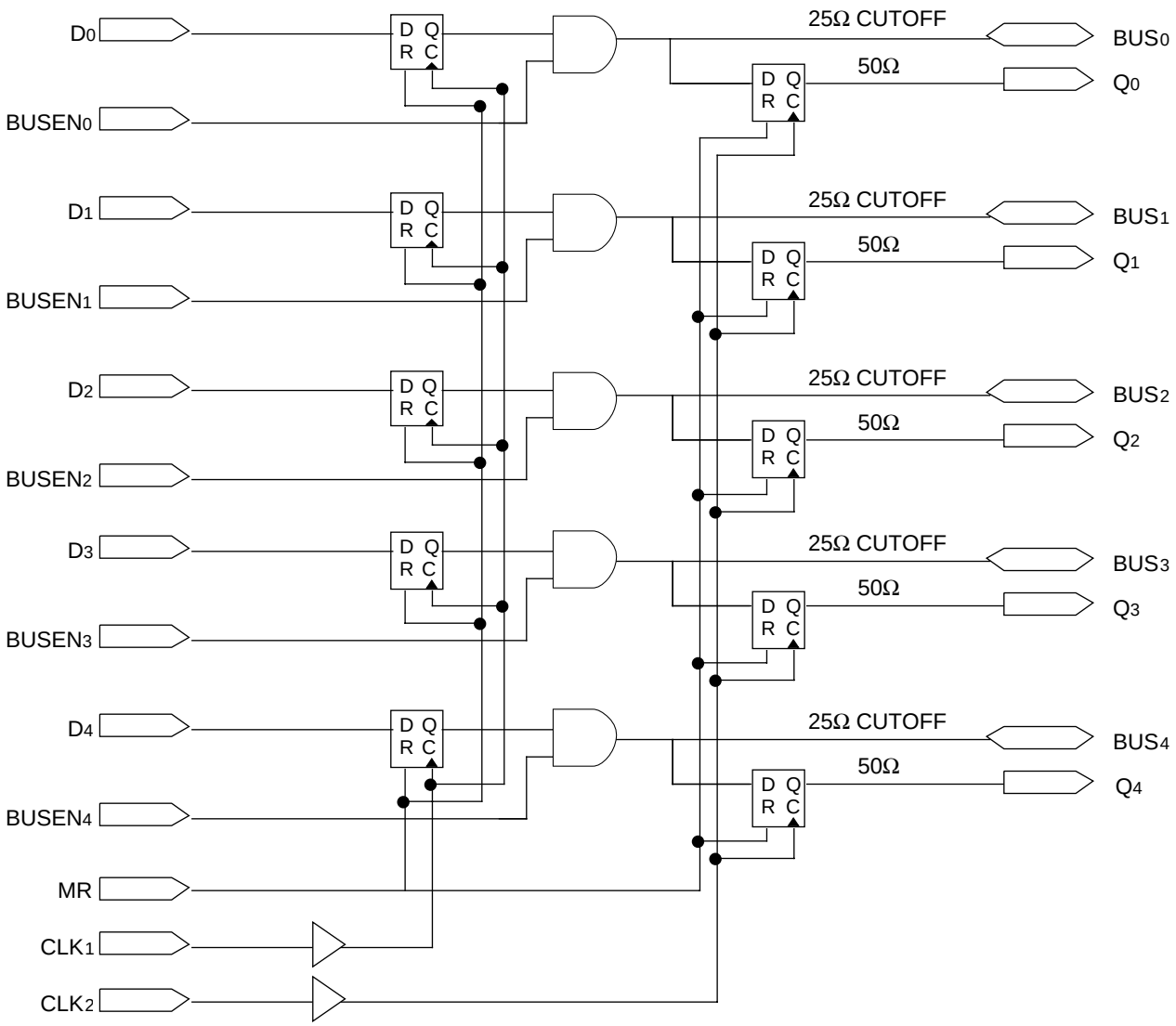
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S891JC	J28-1	Commercial	SY100S891JC	Sn-Pb
SY100S891JCTR[1]	J28-1	Commercial	SY100S891JC	Sn-Pb
SY100S891JZ[2]	J28-1	Commercial	SY100S891JC with Pb-Free bar-line indicator	Matte-Sn
SY100S891JZTR[1, 2]	J28-1	Commercial	SY100S891JC with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V_{CUT}	Cut-off Bus Output Voltage	–2200	–2160	–2100	mV	V_{IN} = V_{IH} (Max.) or V_{IL} (Min.)	Loading with 25Ω to –2.20V
V_{OH}	Output HIGH Voltage Bus	–1025	–955	–880	mV	V_{IN} = V_{IH} (Max.) or V_{IL} (Min.)	Loading with 25Ω to –2.0V
V_{OL}	Output LOW Voltage Bus	–1810	–1705	–1620	mV		
V_{OHA}	Output HIGH Voltage Bus	–1035	—	—	mV	V_{IN} = V_{IH} (Min.) or V_{IL} (Max.)	
V_{OLA}	Output LOW Voltage Bus	—	—	–1610	mV		
V_{OH}	Output HIGH Voltage Receiver	–1025	–955	–880	mV	V_{IN} = V_{IH} (Max.) or V_{IL} (Min.)	Loading with 50Ω to –2.0V
V_{OL}	Output LOW Voltage Receiver	–1810	–1705	–1620	mV		
V_{OHA} V_{OLA}	Output HIGH Voltage Receiver Output LOW Voltage Receiver	–1035 —	— —	— –1610	mV mV	V_{IN} = V_{IH} (Min.) or V_{IL} (Max.)	
V_{IH}	Input HIGH Voltage	–1165	—	–880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	–1810	—	–1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5	—	—	µA	V_{IN} = V_{IL} (Min.)	
I_{IH}	Input High Current	—	—	150	µA	V_{IN} = V_{IH} (Max.)	
I_{EE}	Power Supply Current	–216	—	—	mA	Inputs Open	
C_{IN}	Input Pin Capacitance	—	4	—	pF		
C_{OUT}	Output Pin Capacitance	—	5	—	pF		

AC ELECTRICAL CHARACTERISTICS

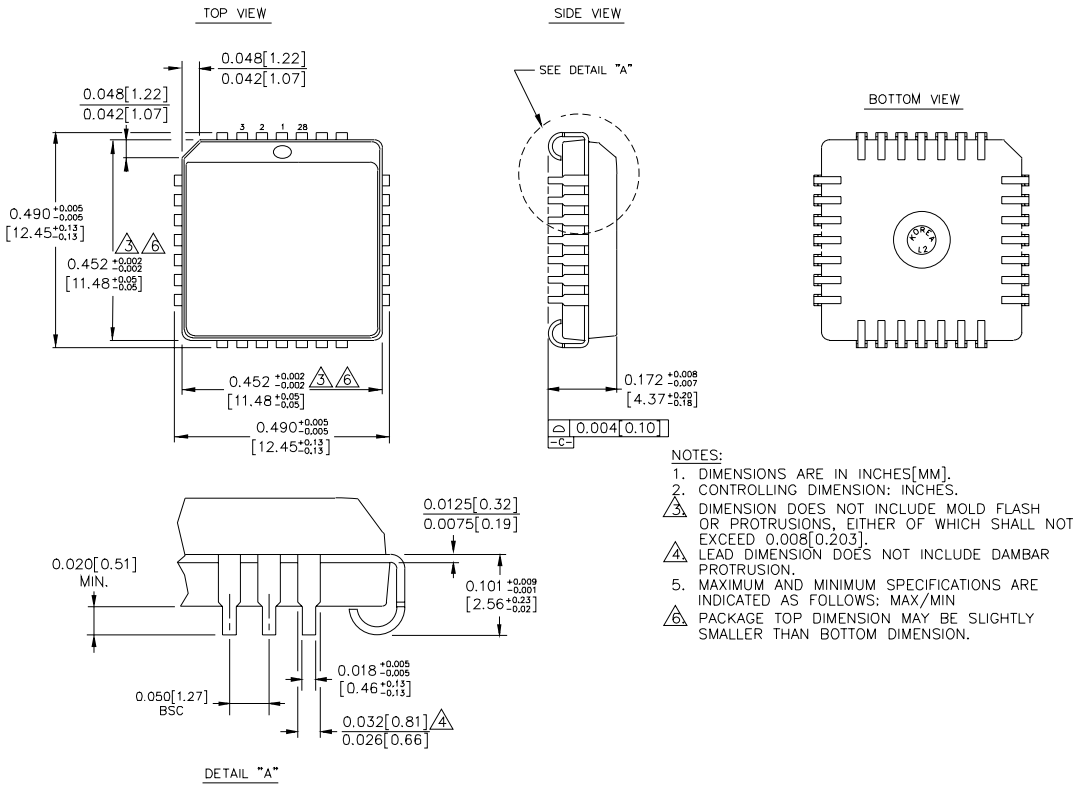
V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay[1] CLK_1 to Bus	600	1000	1500	600	1000	1500	600	1000	1500	ps	
t_{PLH} t_{PHL}	Propagation Delay[2] CLK_2 to Q	500	800	1200	500	800	1200	500	800	1200	ps	
t_{PLH} t_{PHL}	Propagation Delay[1] BUSEN to Bus	500	800	1200	500	800	1200	500	800	1200	ps	
t_{PLH} t_{PHL}	Propagation Delay[1] Master Reset to Bus	600	1000	1500	600	1000	1500	600	1000	1500	ps	
t_{PLH} t_{PHL}	Propagation Delay[2] Master Reset to Q	500	800	1200	500	800	1200	500	800	1200	ps	
t_S	Set-up Time Bus Wrt CLK_2 D Wrt CLK_1	 — —	 — —	 400 400	 — —	 — —	 400 400	 — —	 — —	 400 400	ps	
t_{REL}	Master Reset Release Time	—	—	1000	—	—	1000	—	—	1000	ps	
t_H	Hold Time Bus Wrt CLK_2 D Wrt CLK_1	 — —	 — —	 400 400	 — —	 — —	 400 400	 — —	 — —	 400 400	ps	
t_r	Output Rise Time Bus[3] Q[4]	 500 300	 — —	 1000 900	 500 300	 — —	 1000 900	 500 300	 — —	 1000 900	ps	
t_f	Output Fall Time Bus[3] Q[4]	 500 300	 — —	 1000 900	 500 300	 — —	 1000 900	 500 300	 — —	 1000 900	ps	
t_{skew}	Skew (Maximum difference between slowest and fastest path)	—	100	—	—	100	—	—	100	—	ps	

Notes:

1. Loaded with 25Ω to –2.0V
2. Loaded with 50Ω to –2.0V
3. 25Ω Load
4. 50Ω Load

28-PIN PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com