

# KM416C1000B, KM416C1200B KM416V1000B, KM416V1200B

# CMOS DRAM

## 1M x 16Bit CMOS Dynamic RAM with Fast Page Mode

### DESCRIPTION

This is a family of 1,048,576 x 16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), refresh cycle (1K Ref. or 4K Ref.), access time (-5,-6 or -7), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 1Mx16 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

### FEATURES

#### Part Identification

- KM416C1000B/B-L (5V, 4K Ref.)
- KM416C1200B/B-L (5V, 1K Ref.)
- KM416V1000B/B-L (3.3V, 4K Ref.)
- KM416V1200B/B-L (3.3V, 1K Ref.)

#### Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	1K	4K	1K
-5	396	576	605	880
-6	360	540	550	825
-7	324	504	495	770

#### Refresh Cycles

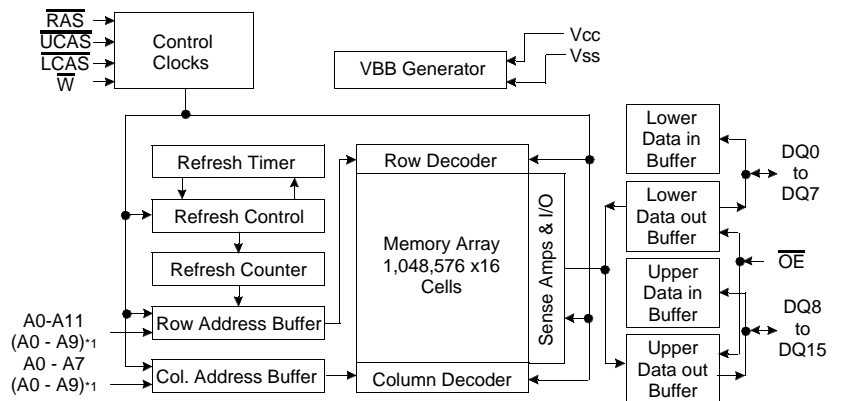
Part NO.	VCC	Refresh cycle	Refresh period	
			Normal	L-ver
C1000B	5V	4K	64ms	128ms
V1000B	3.3V			
C1200B	5V	1K	16ms	
V1200B	3.3V			

#### Performance Range

Speed	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>	t <sub>PC</sub>	Remark
-5	50ns	15ns	90ns	35ns	5V/3.3V
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V

- Fast Page Mode operation
- 2  $\overline{\text{CAS}}$  Byte/Word Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in 42-pin SOJ 400mil and 50(44)-pin TSOP(II) 400mil packages
- Single +5V;  $\pm 10\%$  power supply (5V product)
- Single +3.3V;  $\pm 0.3V$  power supply (3.3V product)

### FUNCTIONAL BLOCK DIAGRAM



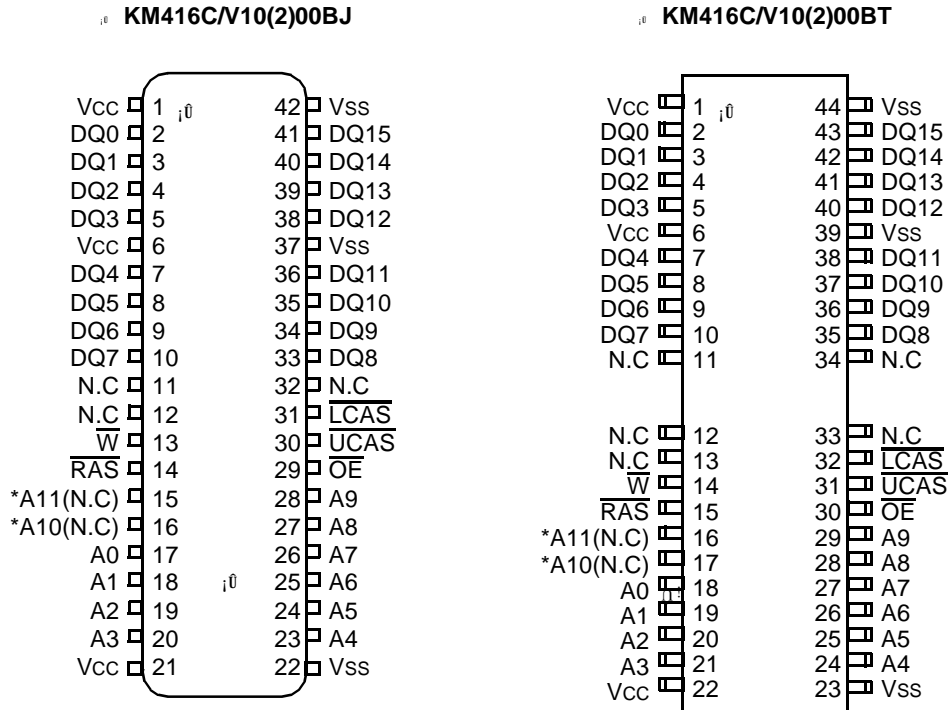
Note) \*1 : 1K Refresh

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**PIN CONFIGURATION (Top Views)**



\*A10 and A11 are N.C for KM416C/V1200B(5V/3.3V, 1K Ref. product)

J : 400mil 42 SOJ  
T : 400mil 50(44) TSOP II

Pin Name	Pin Function
A0 - A11	Address Inputs (4K Product)
A0 - A9	Address Inputs (1K Product)
DQ0 - 15	Data In/Out
Vss	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
Vcc	Power(+5V)
	Power(+3.3V)
N.C	No Connection

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### ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	T <sub>stg</sub>	-55 to +150	-55 to +150	°C
Power Dissipation	P <sub>D</sub>	1	1	W
Short Circuit Output Current	I <sub>OS</sub>	50	50	mA

\* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T<sub>A</sub> = 0 to 70°C)

Parameter	Symbol	3.3V			5V			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.0	-	V <sub>CC</sub> +0.3 <sup>*1</sup>	2.4	-	V <sub>CC</sub> +1.0 <sup>*1</sup>	V
Input Low Voltage	V <sub>IL</sub>	-0.3 <sup>*2</sup>	-	0.8	-1.0 <sup>*2</sup>	-	0.8	V

\*1 : V<sub>CC</sub>+1.3V/15ns(3.3V), V<sub>CC</sub>+2.0V/20ns(5V), Pulse width is measured at V<sub>CC</sub>

\*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at V<sub>SS</sub>

### DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Max	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0 ≤ V <sub>IN</sub> ≤ V <sub>IN</sub> +0.3V, all other input pins not under test=0 Volt)	I <sub>I(L)</sub>	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> )	I <sub>O(L)</sub>	-5	5	μA
	Output High Voltage Level(I <sub>OH</sub> =-2mA)	V <sub>OH</sub>	2.4	-	V
	Output Low Voltage Level(I <sub>OL</sub> =2mA)	V <sub>OL</sub>	-	0.4	V
5V	Input Leakage Current (Any input 0 ≤ V <sub>IN</sub> ≤ V <sub>IN</sub> +0.5V, all other input pins not under test=0 Volt)	I <sub>I(L)</sub>	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> )	I <sub>O(L)</sub>	-5	5	μA
	Output High Voltage Level(I <sub>OH</sub> =-5mA)	V <sub>OH</sub>	2.4	-	V
	Output Low Voltage Level(I <sub>OL</sub> =4.2mA)	V <sub>OL</sub>	-	0.4	V



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### DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max				Units
			KM416V1000B	KM416V1200B	KM416C1000B	KM416C1200B	
I <sub>CC1</sub>	Don't care	-5	110	160	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
I <sub>CC2</sub>	Normal L	Don't care	2	2	2	2	mA
			1	1	1	1	mA
I <sub>CC3</sub>	Don't care	-5	110	160	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
I <sub>CC4</sub>	Don't care	-5	100	100	100	100	mA
		-6	90	90	90	90	mA
		-7	80	80	80	80	mA
I <sub>CC5</sub>	Normal L	Don't care	1	1	1	1	mA
			200	200	200	200	uA
I <sub>CC6</sub>	Don't care	-5	110	160	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
I <sub>CC7</sub>	L	Don't care	400	300	450	350	uA
I <sub>CCS</sub>	L	Don't care	200	200	250	250	uA

I<sub>CC1</sub>\* : Operating Current ( $\overline{RAS}$  and  $\overline{UCAS}$ ,  $\overline{LCAS}$  cycling @trc=min.)

I<sub>CC2</sub> : Standby Current ( $\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{IH}$ )

I<sub>CC3</sub>\* :  $\overline{RAS}$ -only Refresh Current ( $\overline{UCAS}=\overline{LCAS}=V_{IH}$ ,  $\overline{RAS}$  cycling @trc=min.)

I<sub>CC4</sub>\* : Fast Page Mode Current ( $\overline{RAS}=V_{IL}$ ,  $\overline{UCAS}$  or  $\overline{LCAS}$ , Address cycling @tpc=min.)

I<sub>CC5</sub> : Standby Current ( $\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{CC}-0.2V$ )

I<sub>CC6</sub>\* :  $\overline{CAS}$ -Before- $\overline{RAS}$  Refresh Current ( $\overline{RAS}$ ,  $\overline{UCAS}$  or  $\overline{LCAS}$  cycling @trc=min.)

I<sub>CC7</sub> : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage( $V_{IH}$ )= $V_{CC}-0.2V$ , Input low voltage( $V_{IL}$ )= $0.2V$ ,  $\overline{UCAS}$ ,  $\overline{LCAS}=0.2V$ ,

Din=Don't care, TRC=31.25us(4K/L-ver), 125us(1K/L-ver),

TRAS=TRASmin~300ns

I<sub>CCS</sub> : Self Refresh Current

$\overline{RAS}=\overline{UCAS}=\overline{LCAS}=V_{IL}$ ,  $\overline{W}=\overline{OE}=A0 \sim A11=V_{CC}-0.2V$  or  $0.2V$ ,

DQ0 ~ DQ15= $V_{CC}-0.2V$ ,  $0.2V$  or Open

**\*Note** : I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> are dependent on output loading and cycle rates. Specified values are obtained with the output open. I<sub>CC</sub> is specified as an average current. In I<sub>CC1</sub>, I<sub>CC3</sub> and I<sub>CC6</sub>, address can be changed maximum once while  $\overline{RAS}=V_{IL}$ . In I<sub>CC4</sub>, address can be changed maximum once within one fast page mode cycle time, tpc.



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### CAPACITANCE ( $T_A=25^\circ\text{C}$ , $V_{CC}=5\text{V}$ or $3.3\text{V}$ , $f=1\text{MHz}$ )

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A11]	CIN1	-	5	pF
Input capacitance [ $\overline{\text{RAS}}$ , $\overline{\text{UCAS}}$ , $\overline{\text{LCAS}}$ , $\overline{\text{W}}$ , $\overline{\text{OE}}$ ]	CIN2	-	7	pF
Output capacitance [DQ0 - DQ15]	CDQ	-	7	pF

### AC CHARACTERISTICS ( $0 \leq t_{\text{A}} \leq 70^\circ\text{C}$ , See note 1,2)

Test condition (5V device) :  $V_{CC}=5.0\text{V} \pm 10\%$ ,  $V_{\text{IH}}/V_{\text{IL}}=2.4/0.8\text{V}$ ,  $V_{\text{OH}}/V_{\text{OL}}=2.4/0.4\text{V}$

Test condition (3.3V device) :  $V_{CC}=3.3\text{V} \pm 0.3\text{V}$ ,  $V_{\text{IH}}/V_{\text{IL}}=2.2/0.7\text{V}$ ,  $V_{\text{OH}}/V_{\text{OL}}=2.0/0.8\text{V}$

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		ns	
Read-modify-write cycle time	trWC	133		155		185		ns	
Access time from $\overline{\text{RAS}}$	trAC		50		60		70	ns	3,4,9
Access time from $\overline{\text{CAS}}$	tcAC		15		15		20	ns	3,4
Access time from column address	tAA		25		30		35	ns	3,9
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	ns	5
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	trP	30		40		50		ns	
$\overline{\text{RAS}}$ pulse width	trAS	50	10K	60	10K	70	10K	ns	
$\overline{\text{RAS}}$ hold time	trSH	13		15		20		ns	
$\overline{\text{CAS}}$ hold time	tcSH	50		60		70		ns	
$\overline{\text{CAS}}$ pulse width	tcAS	13	10K	15	10K	20	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	trCD	20	37	20	45	20	50	ns	4
$\overline{\text{RAS}}$ to column address delay time	trAD	15	25	15	30	15	35	ns	9
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tcRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	trAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	10
Column address hold time	tCAH	10		10		15		ns	10
Column address to $\overline{\text{RAS}}$ lead time	trAL	25		30		35		ns	
Read command set-up time	trCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	trCH	0		0		0		ns	7
Read command hold time referenced to $\overline{\text{RAS}}$	trRH	0		0		0		ns	7
Write command hold time	twCH	10		10		15		ns	
Write command pulse width	twP	10		10		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	trWL	15		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tcWL	13		15		20		ns	



**AC CHARACTERISTICS** (Continued)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	8,16
Data hold time	tDH	10		10		15		ns	8,16
Refresh period (1K, Normal)	tREF		16		16		16	ms	
Refresh period (4K, Normal)	tREF		64		64		64	ms	
Refresh period (L-ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	6
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	36		40		50		ns	6,12
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	73		85		95		ns	6
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		60		ns	6
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	53		60		65		ns	6
$\overline{\text{CAS}}$ set-up time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	5		5		5		ns	14
$\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		15		ns	15
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time (CBR counter test cycle)	tCPT	20		20		25		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35		40	ns	3
Fast Page mode cycle time	tPC	35		40		45		ns	
Fast Page read-modify-write cycle time	tPRWC	76		80		95		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page cycle)	tCP	10		10		10		ns	11
$\overline{\text{RAS}}$ pulse width (Fast Page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		40		ns	
$\overline{\text{OE}}$ access time	tOEA		13		15		20	ns	3
$\overline{\text{OE}}$ to data delay	tOED	13		15		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	13	0	15	0	20	ns	
$\overline{\text{OE}}$ command hold time	tOEH	13		15		20		ns	
$\overline{\text{RAS}}$ pulse width (C-B-R self refresh)	tRASS	100		100		100		us	17
$\overline{\text{RAS}}$ precharge time (C-B-R self refresh)	tRPS	90		110		130		ns	17
$\overline{\text{CAS}}$ hold time (C-B-R self refresh)	tCHS	-50		-50		-50		ns	17

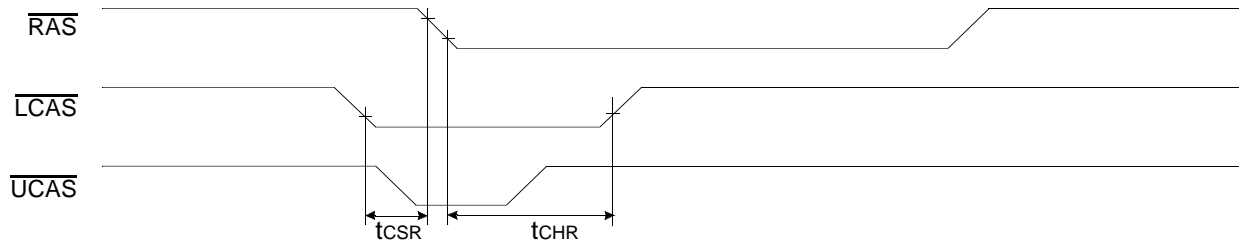
**NOTES**

1. An initial pause of 200us is required after power-up followed by any 8 ROR or  $\overline{\text{CBR}}$  cycles before proper device operation is achieved.
2. Input voltage levels are  $V_{ih}/V_{il}$ .  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1TTL(3.3V) loads and 100pF.
4. Operation within the  $t_{\text{RCD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RCD}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{oh}$  or  $V_{ol}$ .
6.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CPWD}}$  are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ ,  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$  and  $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min})$ , then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycle.
8. These parameters are referenced to the  $\overline{\text{CAS}}$  leading edge in ealy write cycles and to the  $\overline{\text{W}}$  falling edge in  $\overline{\text{OE}}$  controlled write cycle and read-modify-write cycles.
9. Operation within the  $t_{\text{RAD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RAD}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit, then access time is controlled by  $t_{\text{AA}}$ .

**KM416C/V10(2)00B/BL Truth Table**

$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	DQ0 - DQ7	DQ8-DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

10.  $t_{ASC}$ ,  $t_{CAH}$  are referenced to the earlier  $\overline{CAS}$  rising edge.
11.  $t_{CP}$  is specified from the last  $\overline{CAS}$  rising edge in the previous cycle to the first  $\overline{CAS}$  falling edge in the next cycle.
12.  $t_{CWD}$  is referenced to the later  $\overline{CAS}$  falling edge at word read-modify-write cycle.
13.  $t_{CWL}$  is specified from  $\overline{W}$  falling edge to the earlier  $\overline{CAS}$  rising edge.
14.  $t_{CSR}$  is referenced to earlier  $\overline{CAS}$  falling low before  $\overline{RAS}$  transition low.
15.  $t_{CHR}$  is referenced to the later  $\overline{CAS}$  rising high after  $\overline{RAS}$  transition low.



16.  $t_{DS}$ ,  $t_{DH}$  is independently specified for lower byte  $DIN(0-7)$ , upper byte  $DIN(8-15)$
17. 4096(4K Ref.)/1024(1K Ref.) of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification (L-version).