HD-LINX™ GS1510
HDTV Serial Digital Deformatter

PRELIMINARY DATA SHEET

GS1510

FEATURES

- **SMPTE 292M compliant**
- **standards detection/indication for SMPTE 292M levels A/B,C,D/E,F,G/H,I,J/K,L/M**
- **NRZI decoding and SMPTE descrambling with BYPASS option**
- **line CRC calculation, comparison**
- **selectable line based CRC re-Insertion**
- **H, V, F timing reference signal (TRS) extraction**
- **selectable flywheel for noise immune H, V, F extraction**
- **selectable automatic switch line handling**
- **selectable TRS and line number re-insertion**
- **selectable active picture illegal code re-mapping**
- **configurable FIFO LOAD pulse**
- **20 bit 3.3V CMOS input data bus**
- **optimized input interface to GS1545 or GS1540**
- **single +3.3V power supply**
- **5V tolerant I/O**

APPLICATIONS

SMPTE 292M Serial Digital Interfaces.

DESCRIPTION

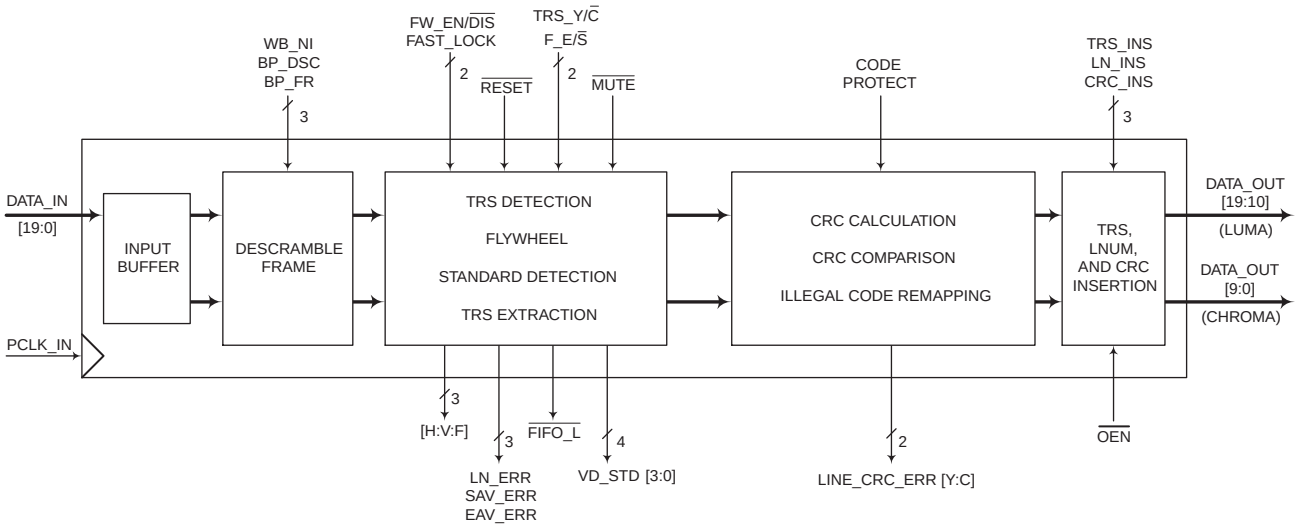
When interfaced to the Gennum GS1545 HDTV Equalizing Receiver or GS1540 Non-Equalizing Receiver, the GS1510 performs the final conversion to word aligned data. The device performs NRZI decoding and de-scrambling as per SMPTE 292M and word-aligns to the incoming data stream. Line based CRCs are calculated on the incoming data stream and are compared against the CRCs embedded within the data stream.

HVF timing information is extracted from the data stream. A selectable internal HVF flywheel provides superior noise immunity against TRS signal errors. The device also detects and indicates the input video signal standard.

The GS1510 can detect and re-map illegal code words contained within the active portion of the video signal. Prior to exiting the device, TRS, Line Numbers and CRCs based on internal calculations may be re-inserted into the data stream.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE
GS1510-CQR	128 pin MQFP	0°C to 70°C



BLOCK DIAGRAM

GENNUM CORPORATION P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946 E-mail: info@gennum.com
www.gennum.com

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage	-0.5V to +4.6V
Input Voltage Range (any input)	-0.5V < V_{IN} < 5.5V
Operating Temperature Range	0°C ≤ T_A ≤ 70°C
Storage Temperature Range	-40°C ≤ T_S ≤ 125°C
Lead Temperature (soldering 10 seconds)	260°C

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.0 to 3.6V, T_A = 0°C to 70°C, unless otherwise shown

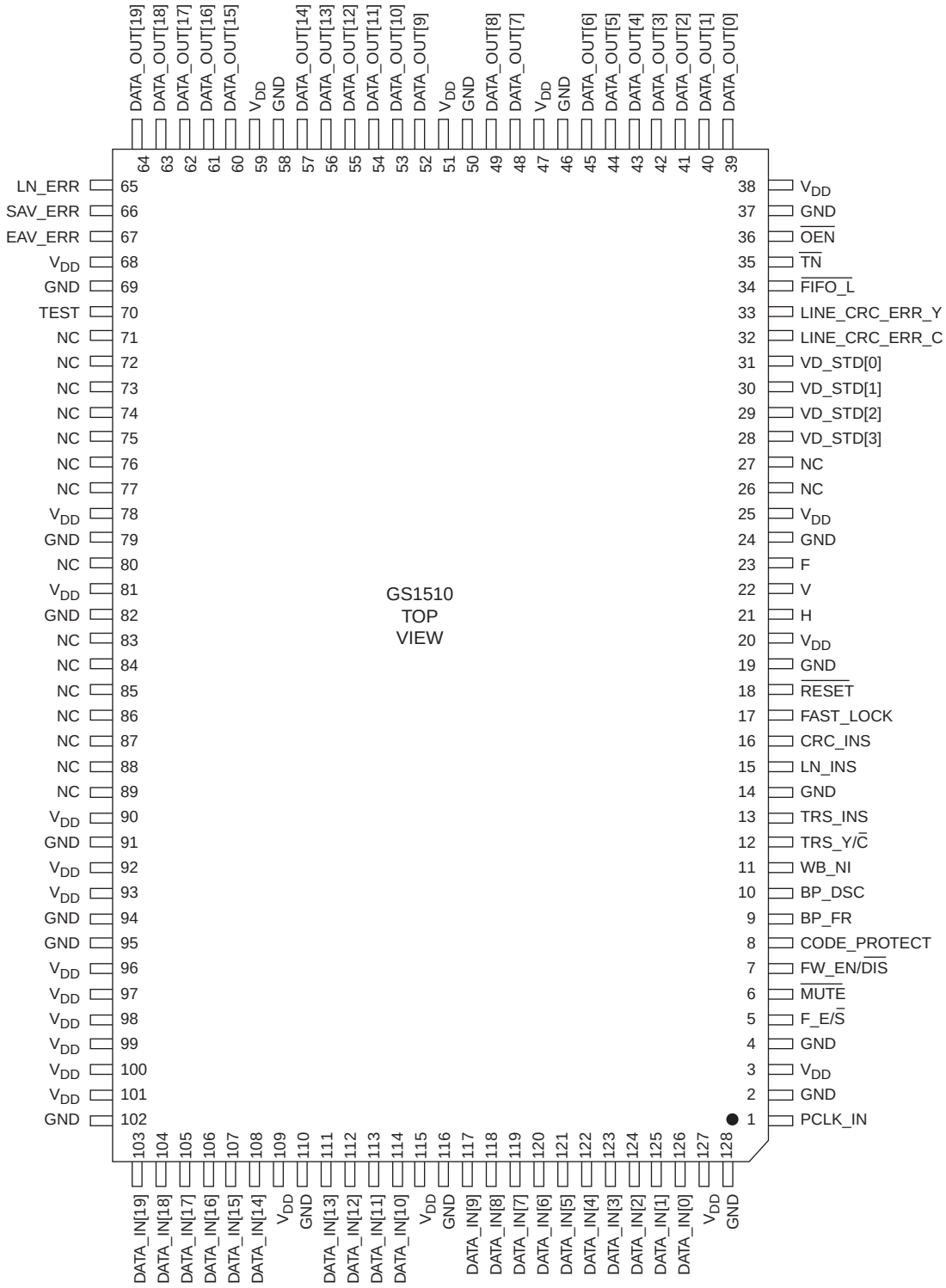
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Positive Supply Voltage	V_{DD}		3.0	3.3	3.6	V	
Supply Current	I_{DD}	f = 74.25MHz, T_A = 25°C	-	402	480	mA	
Input Logic LOW Voltage	V_{IL}	$I_{LEAKAGE}$ < 10µA	-	-	0.8	V	
Input Logic HIGH Voltage	V_{IH}	$I_{LEAKAGE}$ < 10µA	2.1	3.3	5.0	V	
Output Logic LOW Voltage	V_{OL}	V_{DD} = 3.0 to 3.6V, I_{OL} = 4mA	-	0.2	0.4	V	
Output Logic HIGH Voltage	V_{OH}	V_{DD} = 3.0 to 3.6V, I_{OH} = -4mA	2.6	-	-	V	

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.0 to 3.6V, T_A = 0°C to 70°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Clock Input Frequency	F_{HSCI}		-	74.25	80	MHz	Also supports 74.25/1.001MHz
Input Data Setup Time	t_{SU}		2.5	-	-	ns	50% levels
Input Data Hold Time	t_{IH}		1.5	-	-	ns	50% levels
Input Clock Duty Cycle			40	-	60	%	
Output Data Hold Time	t_{OH}	With 15pF load	2.0	-	-	ns	
Output Enable Time	t_{OEN}	With 15pF load	-	-	8	ns	
Output Disable Time	t_{ODIS}	With 15pF load	-	-	9	ns	
Output Data Delay Time	t_{OD}	With 15pF load	-	-	10	ns	
Output Data Rise/Fall Time	t_{ROD}/t_{FOD}	With 15pF load	-	-	2.5	ns	20% to 80% levels

PIN CONNECTIONS



PIN DESCRIPTIONS

NUMBER	SYMBOL	TIMING	TYPE	DESCRIPTION
1	PCLK_IN	Synchronous wrt PCLK_IN	Input	**Input Clock.** The device uses PCLK_IN for clocking the input data stream into DATA_IN[19:0]. This clock is generated by the GS1545 or GS1540
2, 4, 14, 19, 24, 37, 46, 50, 58, 69, 79, 82, 91, 94, 110, 116, 128	GND		Gnd	Ground power supply connections.
3, 20, 25, 38, 47, 51, 59, 68, 78, 81, 90, 93, 109, 115, 127	V_{DD}		Power	Positive power supply connections.
5	F_E/$\overline{S}$	Non-synchronous	Input	**Control Signal Input.** Used to control where the $\overline{FIFO\_L}$ signal is generated. When F_E/$\overline{S}$ is high, the GS1510 generates $\overline{FIFO\_L}$ signal at EAV. When F_E/$\overline{S}$ is low, the GS1510 generates $\overline{FIFO\_L}$ signal at SAV. See Fig. 4 for timing information.
6	$\overline{MUTE}$	Synchronous wrt PCLK_IN	Input	**Control Signal Input.** Used to enable or disable blanking of the LUMA (DATA_OUT[19:10]) and CHROMA (DATA_OUT[9:0]). When $\overline{MUTE}$ is low, the device sets the accompanying LUMA and CHROMA data to their appropriate blanking levels. When $\overline{MUTE}$ is high, the LUMA and CHROMA data streams pass through this stage of the device unaltered.
7	FW_EN/$\overline{DIS}$	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable the internal flywheel. When FW_EN/$\overline{DIS}$ is high, the internal flywheel is enabled. When FW_EN/$\overline{DIS}$ is low, the internal fly-wheel is disabled.
8	CODE_PROTECT	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable re-mapping of out-of-range words contained in the active portion of the video signal. When this signal is high, the device re-maps out-of-range words contained within the active portion of the video signal into CCIR-601 compliant words. Values between 000-003 are re-mapped to 004. Values between 3FC and 3FF are re-mapped to 3FB. When this signal is low, out-of-range words in the active video region pass through the device unaltered.
9	BP_FR	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable word boundary framing. When BP_FR is low internal framing is enabled. When BP_FR is high internal framing is bypassed.
10	BP_DSC	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable the SMPTE 292M descrambler. When BP_DSC is low, the internal SMPTE 292M descrambler is enabled. When BP_DSC is high, the internal SMPTE 292M de-scrambler is bypassed.
11	WB_NI	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable noise immune operation of the word boundary framer. When WB_NI is high, noise-immune word boundary alignment is enabled. The device switches to a new word boundary only when it has detected two consecutive identical new TRS positions. When WB_NI is low, the device re-aligns the word boundary position at every instance of a TRS.
12	TRS_Y/$\overline{C}$	Non-synchronous	Input	**Control Signal Input.** Used to control whether LUMA or CHROMA TRS IDs are detected and used. When TRS_Y/$\overline{C}$ is high, the device detects and uses TRS signals embedded in the LUMA channel. When TRS_Y/$\overline{C}$ is low, the device detects and uses TRS signals embedded in the CHROMA channel.

PIN DESCRIPTIONS

NUMBER	SYMBOL	TIMING	TYPE	DESCRIPTION
13	TRS_INS	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable re-insertion of the TRS into the data stream. When TRS_INS is high, the device re-inserts TRS into the incoming data stream based on the internal calculation. The original TRS packets are set to the blanking levels. If the flywheel is enabled, TRS calculated by the flywheel is used for insertion. When TRS_INS is low, the device will not re-insert TRS even if errors in TRS signals are detected.
15	LN_INS	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable re-insertion of the line number into the data stream. When LN_INS is high, the device re-inserts the line number into the incoming data stream based on the internal calculation. The original line number packets are set to the blanking levels. If the flywheel is enabled, the line number calculated by the flywheel is used for insertion. When LN_INS is low, the device will not re-insert the line number.
16	CRC_INS	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable re-insertion of the CRC into the data stream. When CRC_INS is high, the device is enabled to re-insert line CRCs based on the internal calculation. When CRC_INS is low, the device will not re-insert the CRCs.
17	FAST_LOCK	Synchronous wrt PCLK_IN	Input	**Control Signal Input.** Used to control the flywheel synchronization when a switch line occurs. When a low to high transition occurs on the FAST_LOCK signal, the internal flywheel will immediately re-synchronize to the next valid EAV or SAV TRS in the incoming data stream. See Fig. 5 for timing information.
18	$\overline{\text{RESET}}$	Non-synchronous	Input	**Control Signal Input.** Used to reset the system state registers to their default 720p parameters. When $\overline{\text{RESET}}$ is high, the fly wheel, TRS Detection, and ANC Detection operate normally. When $\overline{\text{RESET}}$ is low, the flywheel, TRS Detection, and ANC Detection are reset to the 720p parameters after a rising edge on PCLK_IN. The read and write counters are not affected.
21	H	Synchronous wrt PCLK_IN	Output	**Control Signal Input.** This signal indicates the Horizontal blanking period of the video signal. Refer to Fig. 2 for timing information of H relative to DATA_OUT[19:10] and DATA_OUT[9:0], LUMA and CHROMA respectively.
22	V	Synchronous wrt PCLK_IN	Output	**Control Signal Input.** This signal indicates the Vertical blanking period of the video signal. Refer to Fig. 2 for timing information of V relative to DATA_OUT[19:10] and DATA_OUT[9:0], LUMA and CHROMA respectively.
23	F	Synchronous wrt PCLK_IN	Output	**Control Signal Input.** This signal indicates the ODD/EVEN field of the video signal. Refer to Fig. 2 for timing information of F relative to DATA_OUT[19:10] and DATA_OUT[9:0], LUMA and CHROMA respectively. When locked and the input signal is of a progressive scan nature, F stays low at all times.
26,27,71-77,80, 83-89	NC	N/A	N/A	**No Connect.** Do not connect these pins.
28, 29, 30, 31	VD_STD[3:0]	Synchronous wrt PCLK_IN	Output	**Control Signal Output.** VD_STD[3:0] indicates which input video standard the device has detected. The GS1510 will indicate all of the formats in SMPTE292M (see Table 1) plus it will indicate an unknown interlace or progressive scan format.

PIN DESCRIPTIONS

NUMBER	SYMBOL	TIMING	TYPE	DESCRIPTION
32	LINE_CRC_ERR_C	Synchronous wrt PCLK_IN	Output	**Status Signal Output.** Indicates a difference in the calculated versus embedded CRC in the CHROMA channel. When LINE_CRC_ERR_C is high, it indicates that the GS1510 has detected a difference between the line based CRCs it calculates for the CHROMA channel and the line based CRCs embedded within the CHROMA channel. When LINE_CRC_ERR_C is low, the embedded and calculated CRCs match. Refer to Fig. 6 for timing information of LINE_CRC_ERR_C.
33	LINE_CRC_ERR_Y	Synchronous wrt PCLK_IN	Output	**Status Signal Output.** Indicates a difference in the calculated versus embedded CRC in the LUMA channel. When LINE_CRC_ERR_Y is high, it indicates that the GS1510 has detected a difference between the line based CRCs it calculates for the LUMA channel and the line based CRCs embedded within the LUMA channel. When LINE_CRC_ERR_Y is low, the embedded and calculated CRCs match. Refer to Fig. 6 for timing information of LINE_CRC_ERR_Y.
34	$\overline{\text{FIFO\_L}}$	Synchronous wrt PCLK_IN	Output	**Status Signal Output.** Used to control an external FIFO(s). $\overline{\text{FIFO\_L}}$ is normally high, but is set low for the EAV or SAV word depending on the state of F_E/$\overline{\text{S}}$. Refer to Fig. 4 for timing information of $\overline{\text{FIFO\_L}}$ relative to LUMA (DATA_OUT[19:10]) and CHROMA (DATA_OUT[9:0]).
35	$\overline{\text{TN}}$		TEST	**Test Pin.** Used for test purposes only. This pin must be connected to V_{DD} for normal operation
36	$\overline{\text{OEN}}$	Non-synchronous	Input	**Control Signal Input.** Used to enable the DATA_OUT[19:0] output bus or set it to a high Z state. When $\overline{\text{OEN}}$ is low, the LUMA (DATA_OUT[19:10]) and CHROMA (DATA_OUT [9:0]) busses are enabled. When $\overline{\text{OEN}}$ is high, these busses are in a high Z state.
39, 40, 41, 42, 43, 44, 45, 48, 49, 52	DATA_OUT[9:0] (CHROMA channel)	Synchronous wrt PCLK_IN	Output	**CHROMA Output Data Bus.** DATA_OUT [9] is CHROMA_OUT[9] which is the MSB of the CHROMA output signal (pin 52). DATA_OUT [0] is CHROMA_OUT[0] which is the LSB of the CHROMA output signal (pin 39).
53, 54, 55, 56, 57, 60, 61, 62, 63, 64	DATA_OUT[19:10] (LUMA channel)	Synchronous wrt PCLK_IN	Output	**LUMA Output Data Bus.** DATA_OUT [19] is LUMA_OUT[9] which is the MSB of the LUMA output signal (pin 64). DATA_OUT [10] is LUMA_OUT[0] which is the LSB of the LUMA output signal (pin 53).
65	LN_ERR	Synchronous wrt PCLK_IN	Output	**Status Signal Output.** Used to indicate a Line Number error or a mismatch between the embedded line number and the flywheel line number when the flywheel is enabled. When LN_ERR is high, a line number error is detected or the internal flywheel indicates mismatching line numbers. Refer to Fig. 3 for timing information of LN_ERR relative to LUMA (DATA_OUT[19:10]) and CHROMA (DATA_OUT [9:0]) Since LN_ERR depends on the sequence of line numbers, a line number error will actually cause LN_ERR to go high for two lines.
66	SAV_ERR	Synchronous wrt PCLK_IN	Output	**Status Signal Output.** Indicates a TRS error or a mismatch between the embedded TRS and the flywheel TRS when the flywheel is enabled. This signal is set high when an error in the SAV TRS is detected or when the internal flywheel indicates there is a mismatching SAV TRS. Refer to Fig. 3 for timing information of SAV_ERR relative to LUMA (DATA_OUT[19:10]) and CHROMA (DATA_OUT [9:0]).

PIN DESCRIPTIONS

NUMBER	SYMBOL	TIMING	TYPE	DESCRIPTION
67	EAV_ERR	Synchronous wrt PCLK_IN	Output	**Status signal output.** Indicates a TRS error or a mismatch between the embedded TRS and the flywheel TRS when the flywheel is enabled. This signal is set high when an error in the EAV TRS is detected or when the internal flywheel indicates there is a mismatching EAV TRS. Refer to Fig. 3 for timing information of EAV_ERR relative to LUMA (DATA_OUT[19:10]) and CHROMA (DATA_OUT [9:0]).
70	TEST		TEST	**Test pin.** Used for test purposes only. This pin must be connected to GND for normal operation.
92, 96, 97, 98, 99,100,101	V_{DD}	N/A	N/A	Must be connected to V_{DD} for normal operation.
95, 102	GND	N/A	N/A	Must be connected to GND for normal operation.
103,104,105, 106, 107, 108, 111, 112, 113, 114, 117, 118, 119,120, 121, 122, 123, 124, 125, 126	DATA_IN [19:0]	Synchronous wrt PCLK_IN	Input	**Input data bus.** DATA_IN [19] is the MSB of the signal (pin 103). DATA_IN [0] is the LSB of the signal (pin 126). This data is typically scrambled and not word aligned.

DETAILED DESCRIPTION

1. DATA INPUT AND OUTPUTS

Data enters and exits the device on the rising edge of PCLK_IN as shown in Figures 1 and 2. This data can be scrambled or unscrambled and framed or unframed.

2. DESCRAMBLER AND FRAMER

Both the descrambler and framer can be enabled or disabled independently of each other to allow the input to remain scrambled or unscrambled. If the data is unscrambled, it can be word aligned (framed) or passed through unaltered.

3. STANDARDS INDICATION

VD_STD[3:0] indicates the standard that the device has detected. The states of VD_STD[3:0] are shown in the following standards indication tables.

Interlaced Standards Indication
(VD_STD[3]=1)

VD_STD[3:0]	DESCRIPTION
1000	1080i (30 & 30/1.001Hz → D/E) [SMPTE274M]
1001	Reserved
1010	1080i (25Hz → F) [SMPTE274M]
1011	Reserved
1100	1080i (25Hz → C) [SMPTE295M]
1101	Reserved
1110	1035i (30 & 30/1.001Hz → A/B) [SMPTE260M]
1111	Unknown Interlaced with F switching 0/1

Progressive Scan Standards Indication
(VD_STD[3]=0)

VD_STD[3:0]	DESCRIPTION
0000	720p (60 & 60/1.001Hz → L/M) [SMPTE296M]
0001	Reserved
0010	1080p (30 & 30/1.001Hz → G/H) [SMPTE274M]
0011	Reserved
0100	1080p (25Hz → I) [SMPTE274M]
0101	Reserved
0110	1080p (24 & 24/1.001Hz → J/K) [SMPTE274M]
0111	Unknown Progressive with F = 0 always.

Note the following in the above tables:

SMPTE260M is 1125 lines/frame

SMPTE274M is 1125 lines/frame

SMPTE295M is 1250 lines/frame

SMPTE296M is 750 lines/frame

See Table 1 for more specific details on the source format parameters.

4. FLY WHEEL OPERATION

The flywheel logic will check the incoming video data for valid video lines. If the incoming data represents a valid line, the flywheel remains in sync with the incoming data. If the incoming data represents an invalid line, the flywheel will use the stored timing information for the past valid line to generate the output HVF timing signals until three (3) consecutive lines having identical timing are detected. In this case, the new timing information will be saved and the flywheel operation is updated to this new timing. Mismatches between the HVF information decoded from the data stream and that indicated by the flywheel will trigger the EAV_ERR and SAV_ERR signals as shown in Figure 3. HVF output timing is shown in Figure 2.

5. AUTOMATIC SWITCH LINE LOCK HANDLING

The automatic switch line lock is based on the assumption that the switching of video sources will only cause the H signal to be out of alignment whereas V and F signals remain in sync; i.e. switching between video sources of the same format. Therefore, when in the automatic switch line lock mode (FAST_LOCK transitions for low to high), the flywheel positive H signal transition will align with the detected positive H signal transition. Timing for the FAST_LOCK signal is shown in Figure 5.

TABLE 1: Source Format Parameters

Reference SMPTE Standard	260m	260m	295m	274m	274m	274m	274m	274m	274m	274m	274m	296m	296m
Format ID	A	B	C	D	E	F	G	H	I	J	K	L	M
Lines/Frame	1125	1125	1250	1125	1125	1125	1125	1125	1125	1125	1125	750	750
Words/Active Line (each channel Y, Cb/Cr)	1920	1920	1920	1920	1920	1920	1920	1920	1920	1920	1920	1280	1280
Total Active Lines	1035	1035	1080	1080	1080	1080	1080	1080	1080	1080	1080	720	720
Words/Total Line (each channel Y, Cb/Cr)	2200	2200	2376	2200	2200	2640	2200	2200	2640	2750	2750	1650	1650
Frame Rate (Hz)	30	30/M	25	30	30/M	25	30	30/M	25	24	24/M	60	60/M
Fields /Frame	2	2	2	2	2	2	1	1	1	1	1	1	1
Data Rate Divisor	1	M	1	1	M	1	1	M	1	1	M	1	M

NOTE: M=1.001 in the above table.

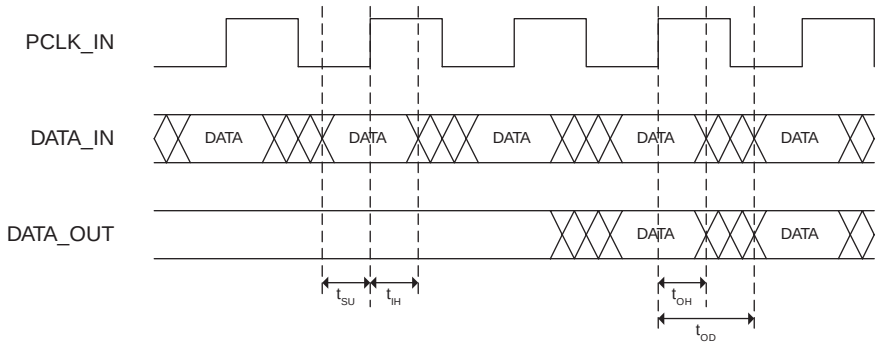


Fig. 1 Synchronous I/O Timing

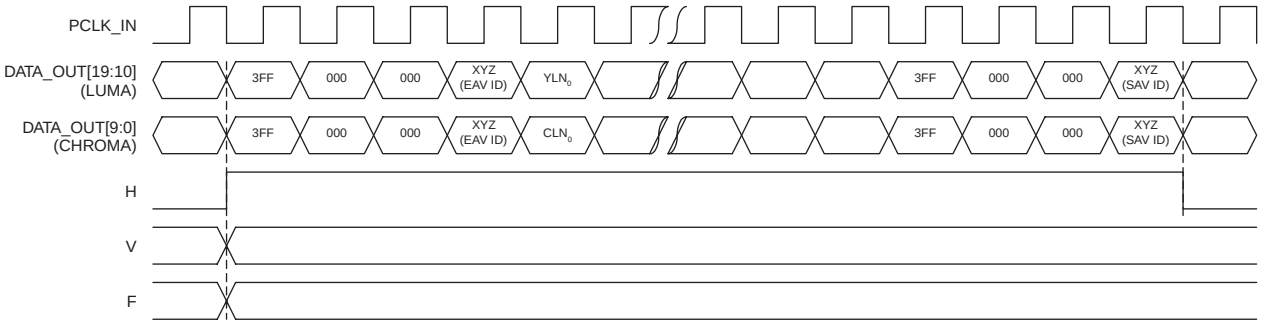


Fig. 2 HVF Timing

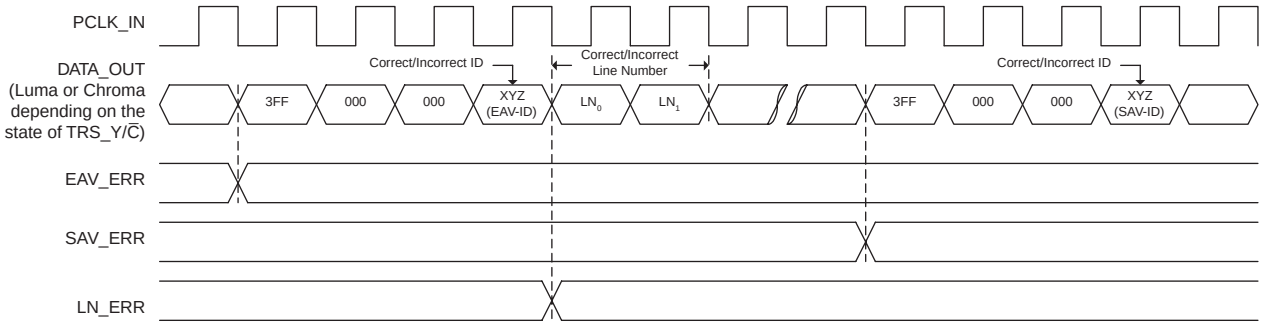


Fig. 3 EAV_ERR, SAV_ERR and LN_ERR Timing

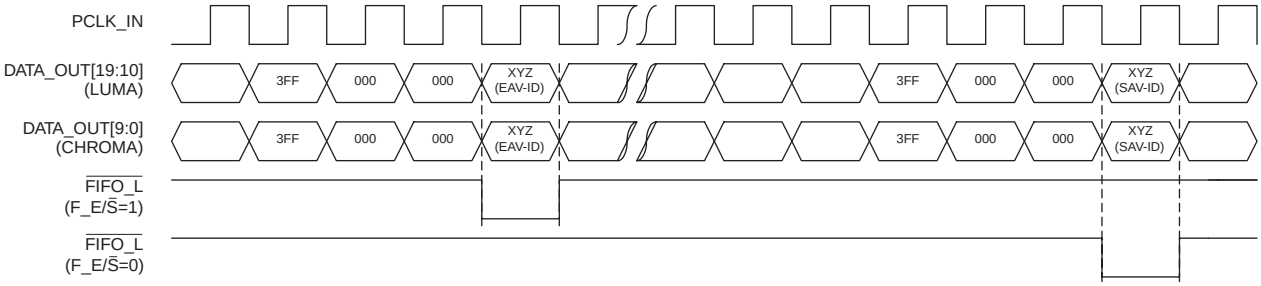


Fig. 4 FIFO_L Timing

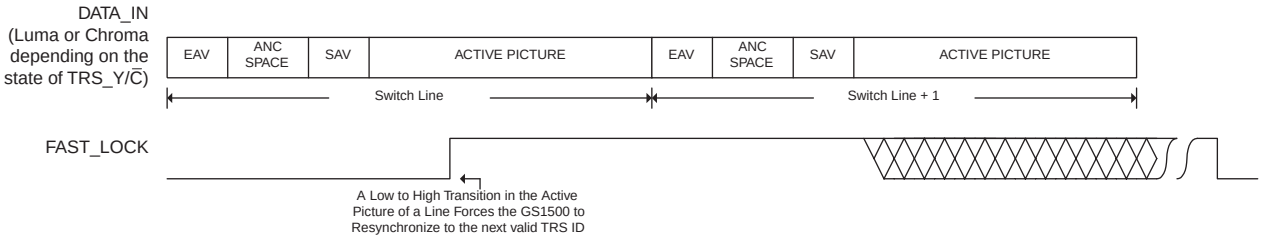


Fig. 5 FAST_LOCK Timing

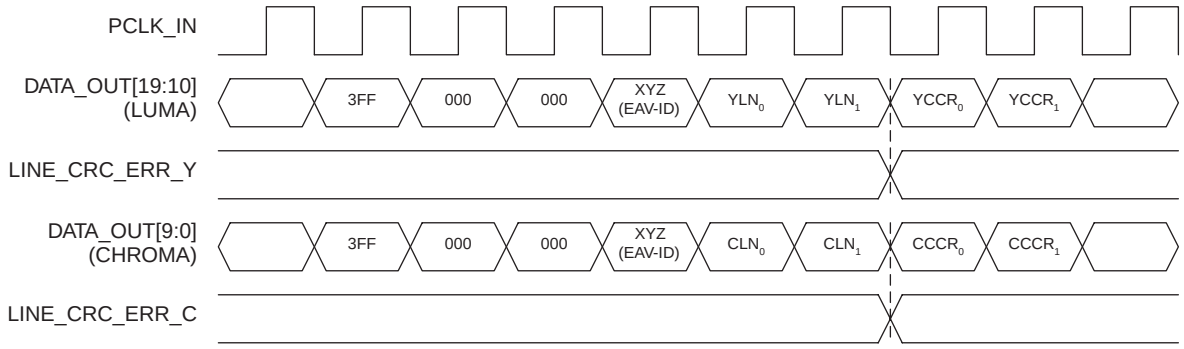
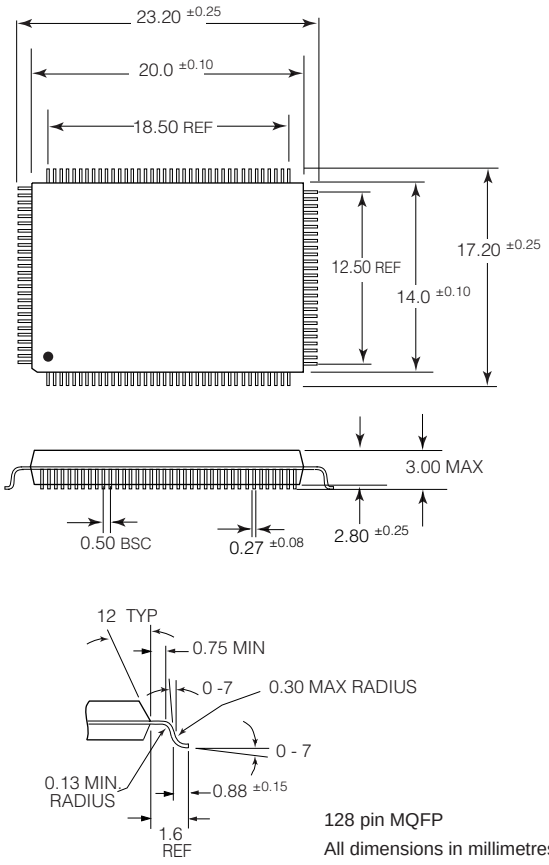


Fig. 6 Luma and Chroma LINE_CRC_ERR Timing

PACKAGE DIMENSIONS



128 pin MQFP

All dimensions in millimetres

CAUTION

ELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION

PRELIMINARY DATA SHEET

The product is in a preproduction phase and specifications are subject to change.

REVISION NOTES:

Updated Absolute Maximum Ratings; Updated AC and DC Electrical Characteristics Tables; Updated Figure 4.

For latest product information, visit www.gennum.com

GENNUM CORPORATION

MAILING ADDRESS:
P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946

SHIPPING ADDRESS:
970 Fraser Drive, Burlington, Ontario, Canada L7L 5P5

GENNUM JAPAN CORPORATION
C-101, Miyamae Village, 2-10-42 Miyamae, Suginami-ku
Tokyo 168-0081, Japan
Tel. +81 (03) 3334-7700 Fax. +81 (03) 3247-8839

GENNUM UK LIMITED
25 Long Garden Walk, Farnham, Surrey, England GU9 7HX
Tel. +44 (0)1252 747 000 Fax +44 (0)1252 726 523