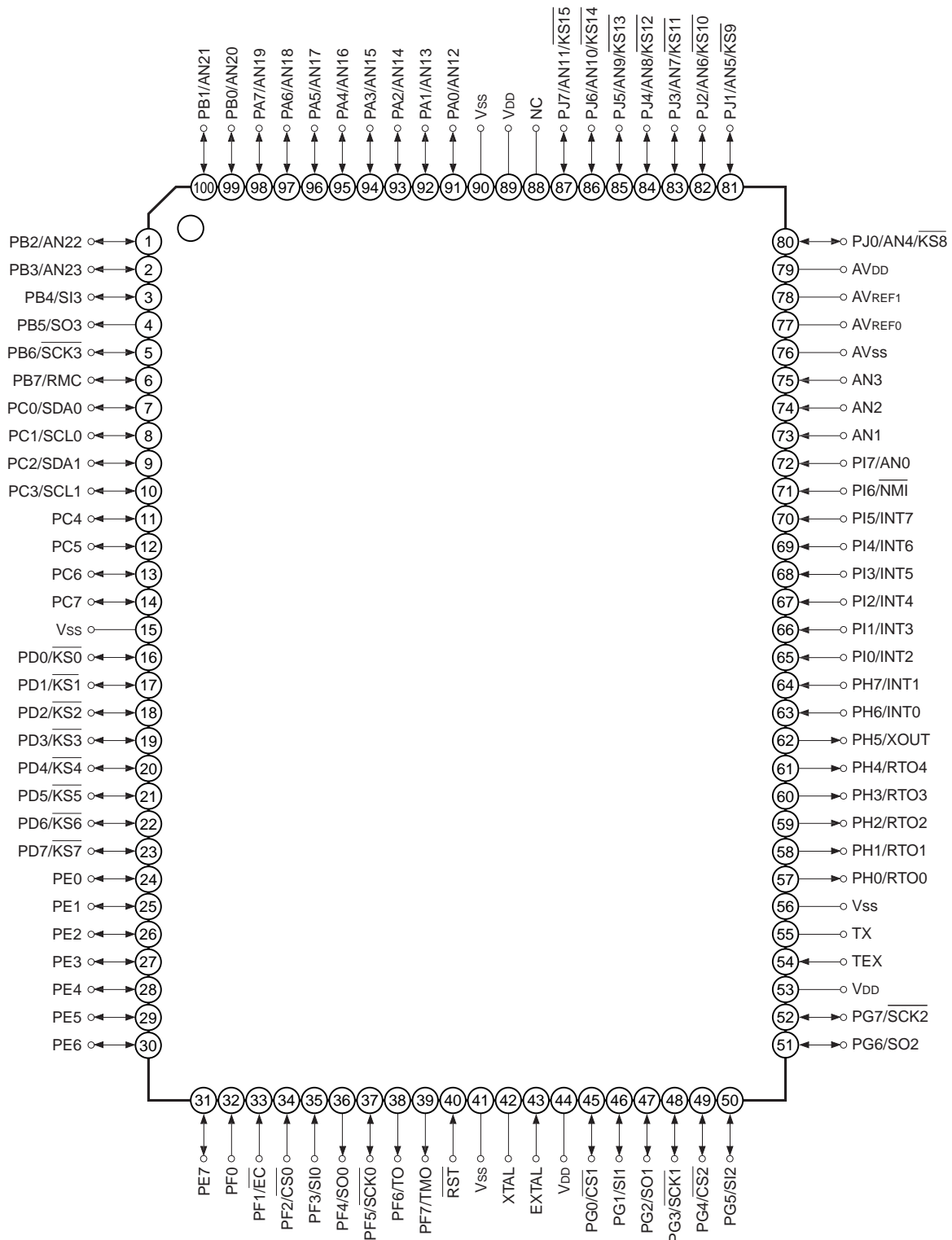
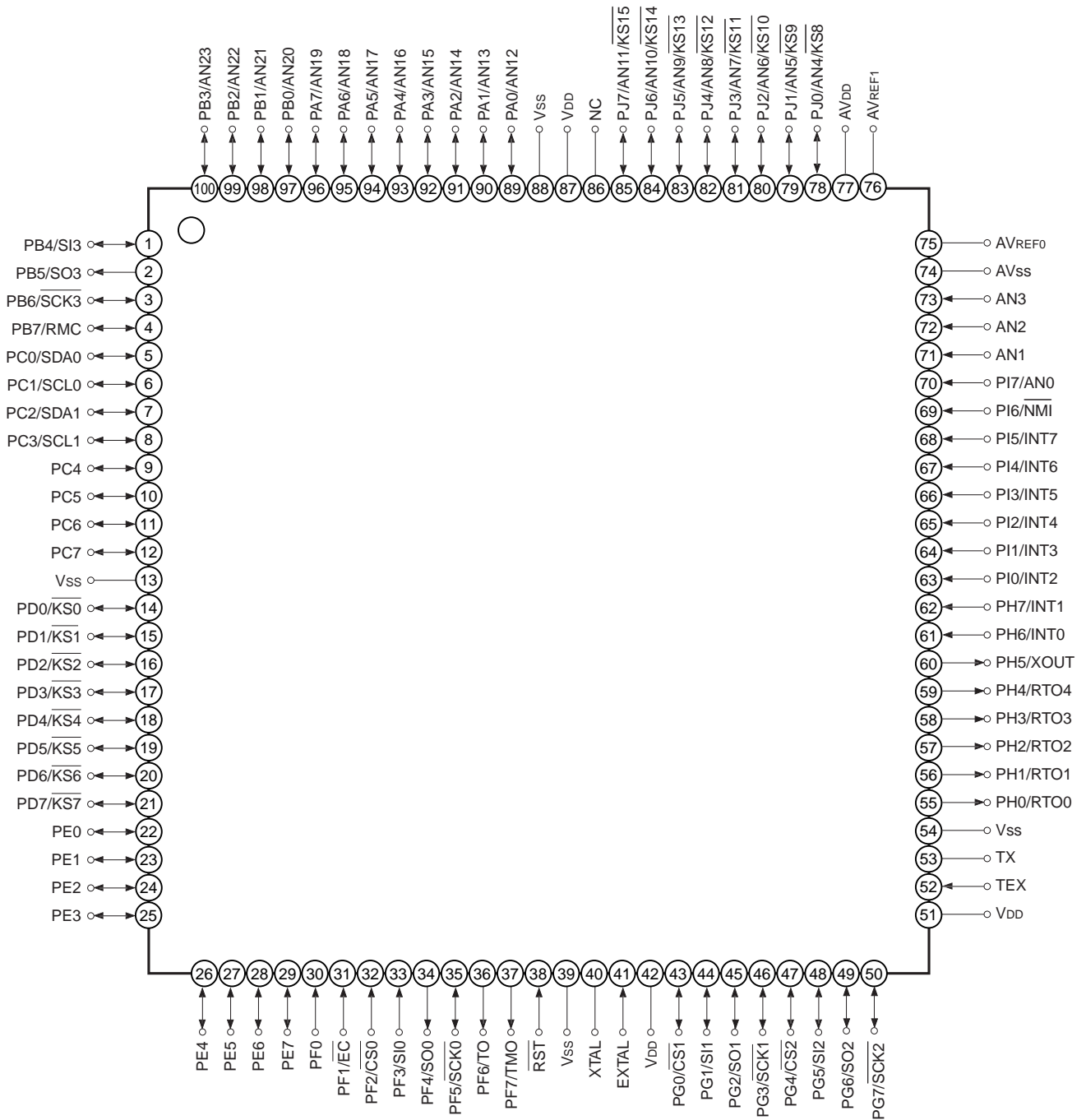


Pin Assignment 1 (Top View) 100-pin QFP package



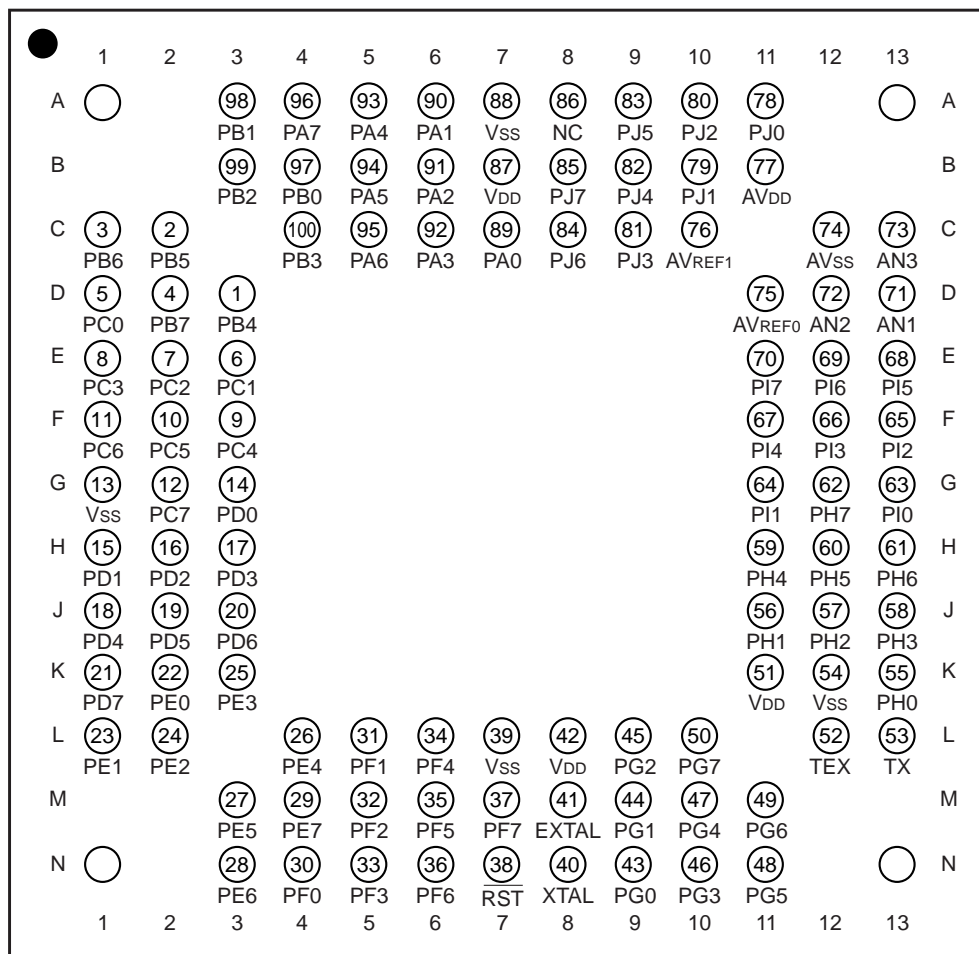
- Note** 1. NC (Pin 88) must be left open. However, use this pin for FLASH EEPROM incorporated version.
 2. Vss (Pins 15, 41, 56 and 90) must be connected to GND.
 3. VDD (Pins 44, 53 and 89) must be connected to VDD.

Pin Assignment 2 (Top View) 100-pin LQFP package



- Note** 1. NC (Pin 86) must be left open. However, use this pin for FLASH EEPROM incorporated version.
2. Vss (Pins 13, 39, 54 and 88) must be connected to GND.
3. VDD (Pins 42, 51 and 87) must be connected to VDD.

Pin Assignment 3 (Top View) 104-pin LFLGA package



- Note)** 1. NC (Pin 86) must be left open. However, use this pin for FLASH EEPROM incorporated version.
 2. V_{SS} (Pins 13, 39, 54 and 88) must be connected to GND.
 3. V_{DD} (Pins 42, 51 and 87) must be connected to V_{DD}.

Pin Functions

Symbol	I/O	Functions	
PA0/AN12 to PA7/AN19	Output / Input	(Port A) 8-bit output port. (8 pins)	Analog input for A/D converter. (12 pins)
PB0/AN20 to PB3/AN23	Output / Input	(Port B) 8-bit output port. (8 pins)	
PB4/SI3	Output / Input		Serial data (CH3) input.
PB5/SO3	Output / Output		Serial data (CH3) output.
PB6/SCK3	Output / I/O		Serial clock (CH3) I/O.
PB7/RMC	Output / Input		Remote control receive circuit input.
PC0/SDA0	I/O / I/O	(Port C) 8-bit I/O port. I/O can be specified in 1-bit units. Pull-up resistor is present or not through program in 1-bit units. (8 pins)	Data I/O of I ² C bus interface (CH0).
PC1/SCL0	I/O / I/O		Clock I/O of I ² C bus interface (CH0).
PC2/SDA1	I/O / I/O		Data I/O of I ² C bus interface (CH1).
PC3/SCL1	I/O / I/O		Clock I/O of I ² C bus interface (CH1).
PC4 to PC7	I/O		
PD0/KS0 to PD7/KS7	I/O / Input	(Port D) 8-bit I/O port. I/O can be specified in 1-bit units. Can drive 5mA sink current (V _{DD} = 2.7 to 3.3V). (8 pins)	Standby release input function can be specified in 1-bit units. (8 pins)
PE0 to PE7	I/O	(Port E) 8-bit I/O port. I/O can be specified in 1-bit units. (8 pins)	
PF0	Input	(Port F) 8-bit port. Lower 4 bits are for input; upper 4 bits are for output. (8 pins)	External event input for 8-bit timer/counter. Serial chip select (CH0) input. Serial data (CH0) input. Serial data (CH0) output. Serial clock (CH0) I/O. 8-bit timer/counter output. 16-bit timer (CH0) output.
PF1/EC	Input / Input		
PF2/CS0	Input / Input		
PF3/SI0	Input / Input		
PF4/SO0	Output / Output		
PF5/SCK0	Output / I/O		
PF6/TO	Output / Output		
PF7/TMO	Output / Output		

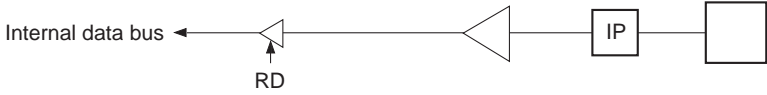
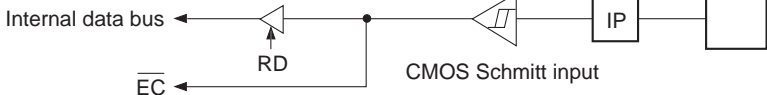
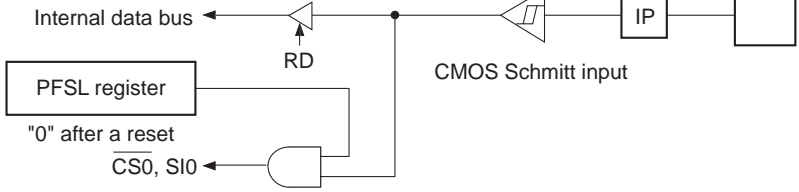
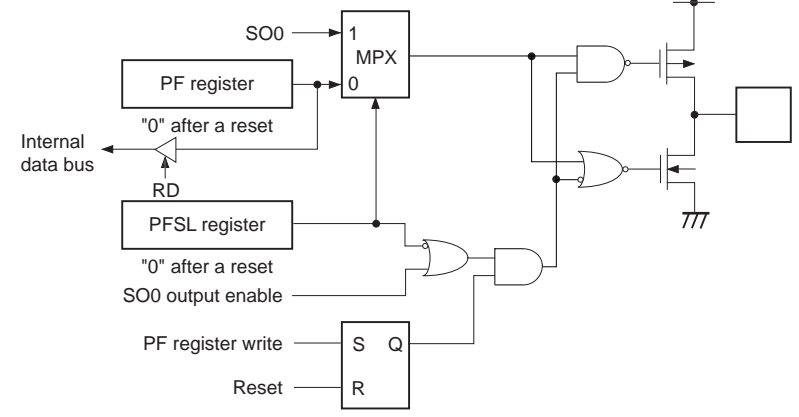
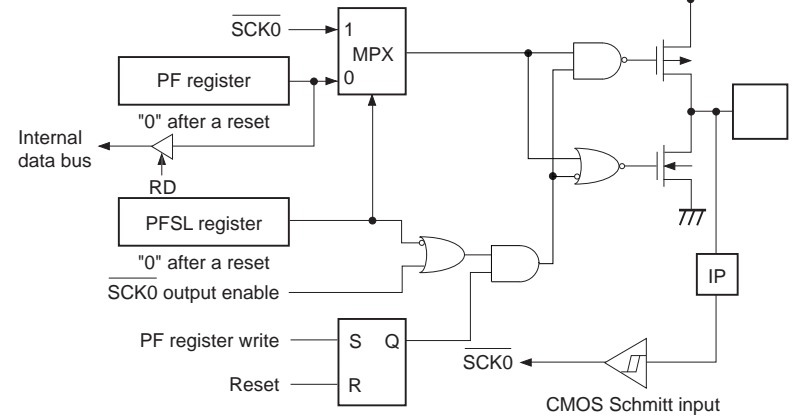
Symbol	I/O	Functions	
PG0/ $\overline{CS1}$	I/O / Input	(Port G) 8-bit I/O port. I/O can be specified in 1-bit units. (8 pins)	Serial chip select (CH1) input.
PG1/SI1	I/O / Input		Serial data (CH1) input.
PG2/SO1	I/O / Output		Serial data (CH1) output.
PG3/ $\overline{SCK1}$	I/O / I/O		Serial clock (CH1) I/O.
PG4/ $\overline{CS2}$	I/O / Input		Serial chip select (CH2) input.
PG5/SI2	I/O / Input		Serial data (CH2) input.
PG6/SO2	I/O / Output		Serial data (CH2) output.
PG7/ $\overline{SCK2}$	I/O / Output		Serial clock (CH2) output.
PH0/RTO0 to PH4/RTO4	Output / Output	(Port H) 8-bit port. Lower 6 bits are for output; upper 2 bits are for input. (8 pins)	Real-time pulse generator output. (5 pins)
PH5/XOUT	Output / Output		Clock output for clock prescaler buzzer.
PH6/INT0 to PH7/INT1	Input / Input		External interrupt input. (8 pins)
PI0/INT2 to PI5/INT7	Input / Input	(Port I) 8-bit input port. (8 pins)	Non-maskable external interrupt input.
PI6/ \overline{NMI}	Input / Input		
PI7/AN0	Input / Input		
AN1 to AN3	Input	Analog input for A/D converter. (12 pins)	
PJ0/AN4/ KS8 to PJ7/AN11/ KS15	I/O / Input / Input	(Port J) 8-bit I/O port. I/O can be specified in 1-bit units. (8 pins)	Standby release input function can be specified in 1-bit units. (8 pins)
EXTAL	Input	Connects a crystal for main clock oscillation. (When the clock is supplied externally, input it to EXTAL and input an opposite phase clock to XTAL.)	
XTAL			
TEX	Input	Connects a crystal for sub clock oscillation. (When the clock is supplied externally, input it to TEX and input an opposite phase clock to TX.)	
TX			
\overline{RST}	Input	System reset. Active at "L" level.	
AVDD		Positive power supply for A/D converter.	
AVREF0	Input	Reference voltage input for A/D converter (CH0).	
AVREF1	Input	Reference voltage input for A/D converter (CH1).	
AVSS		GND for A/D converter.	
VDD		Positive power supply. (Connect all three VDD pins to positive power supply.)	
VSS		GND (Connect all four VSS pins to GND.)	
NC		NC. (NC is used for FLASH EEPROM incorporated version.)	

I/O Circuit Format for Pins

Pin	Circuit format	After a reset
<p>PA0/AN12 to PA7/AN19</p>		<p>Hi-Z</p>
<p>PB0/AN20 to PB3/AN23</p>		<p>Hi-Z</p>
<p>PB4/SI3 PB7/RMC</p>		<p>Hi-Z</p>

Pin	Circuit format	After a reset
PB5/SO3		Hi-Z
PB6/ $\overline{\text{SCK3}}$		Hi-Z
PC0/SDA0 PC1/SCL0 PC2/SDA1 PC3/SCL1	<p>* Pull-up transistor approximately 15kΩ (V_{DD} = 2.7 to 3.3V)</p>	Hi-Z

Pin	Circuit format	After a reset
PC4 to PC7	<p>* Pull-up transistor approximately 15kΩ (V_{DD} = 2.7 to 3.3V)</p>	Hi-Z
PD0/ <u>KS0</u> to PD7/ <u>KS7</u>	<p>* Large current drive 5mA (V_{DD} = 2.7 to 3.3V)</p>	Hi-Z
PE0 to PE7		Hi-Z

Pin	Circuit format	After a reset
PF0		Hi-Z
PF1/ \overline{EC}		Hi-Z
PF2/ $\overline{CS0}$ PF3/SI0		Hi-Z
PF4/SO0		Hi-Z
PF5/ $\overline{SCK0}$		Hi-Z

Pin	Circuit format	After a reset
<p>PF6/TO PF7/TMO</p>	<p>PF register write — S Q Reset — R</p> <p>TO, TMO — 1 MPX 0</p> <p>PF register "0" after a reset</p> <p>Internal data bus RD</p> <p>PFSL register "0" after a reset</p> <p>* Pull-up transistor approximately 150kΩ (V_{DD} = 2.7 to 3.3V)</p>	<p>"H" level ("H" level at ON resistance of pull- up transistor during a reset.)</p>
<p>PG0/$\overline{\text{CS1}}$ PG1/$\overline{\text{S1}}$ PG4/$\overline{\text{CS2}}$ PG5/$\overline{\text{S2}}$</p>	<p>PG register Underfined after a reset</p> <p>PGD register "0" after a reset</p> <p>Internal data bus RD</p> <p>PGSL register "0" after a reset $\overline{\text{CS1}}$, $\overline{\text{S1}}$ $\overline{\text{CS2}}$, $\overline{\text{S2}}$</p> <p>CMOS Schmitt input</p> <p>IP</p>	<p>Hi-Z</p>
<p>PG2/$\overline{\text{SO1}}$ PG3/$\overline{\text{SCK1}}$ PG6/$\overline{\text{SO2}}$ PG7/$\overline{\text{SCK2}}$</p>	<p>$\overline{\text{SO1}}$, $\overline{\text{SCK1}}$ $\overline{\text{SO2}}$, $\overline{\text{SCK2}}$</p> <p>PG register Underfined after a reset</p> <p>PGSL register "0" after a reset</p> <p>Internal data bus RD</p> <p>PGD register "0" after a reset</p> <p>$\overline{\text{SO1}}$, $\overline{\text{SCK1}}$ $\overline{\text{SO2}}$, $\overline{\text{SCK2}}$ output enable</p> <p>$\overline{\text{SCK1}}$</p> <p>CMOS Schmitt input (PG3 only)</p> <p>IP</p>	<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PH0/RTO0 to PH4/RTO4</p>		<p>Hi-Z</p>
<p>PH5/XOUT</p>		<p>Hi-Z</p>
<p>PH6/INT0 to PH7/INT1</p>		<p>Hi-Z</p>
<p>PI0/INT2 to PI5/INT7</p>		<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PI6/$\overline{\text{NMI}}$</p>	<p>PISL register "0" after a reset</p> <p>Interrupt circuit ($\overline{\text{NMI}}$)</p> <p>Internal data bus</p> <p>RD</p> <p>CMOS Schmitt input</p> <p>IP</p>	<p>Hi-Z</p>
<p>PI7/$\overline{\text{AN0}}$</p>	<p>PISL register "0" after a reset</p> <p>Internal data bus</p> <p>RD</p> <p>A/D converter</p> <p>Input multiplexer</p> <p>IP</p>	<p>Hi-Z</p>
<p>AN1 to AN3</p>	<p>A/D converter</p> <p>Input multiplexer</p> <p>IP</p>	<p>Hi-Z</p>
<p>PJ0/$\overline{\text{AN4}}$/ KS8 to PJ7/$\overline{\text{AN11}}$/ KS15</p>	<p>PJ register Underfined after a reset</p> <p>PJD register "0" after a reset</p> <p>Internal data bus</p> <p>RD</p> <p>Standby release</p> <p>PJSL register "0" after a reset</p> <p>A/D converter</p> <p>Input multiplexer</p> <p>IP</p> <p>TTT</p>	<p>Hi-Z</p>

Pin	Circuit format	After a reset
EXTAL XTAL	<p>Timing generator</p> <ul style="list-style-type: none"> • Diagram shows circuit configuration during oscillation. • Feedback register is removed during stop mode, and XTAL is driven at "H" level. 	Oscillation
TEX TX	<p>Timing generator, clock prescaler</p> <ul style="list-style-type: none"> • TX is driver at Hi-Z during stop. 	Oscillation
$\overline{\text{RST}}$	<p>CMOS Schmitt input</p> <p>* Pull-up transistor approximately 30kΩ ($V_{DD} = 2.7$ to 3.3V)</p>	"L" level (during a reset)

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +4.6	V	
	AV _{DD}	AV _{SS} to +4.6* ¹	V	
	AV _{REF}	AV _{SS} to +4.6* ¹	V	
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +4.6* ²	V	
Output voltage	V _{OUT}	-0.3 to +4.6* ²	V	
High level output current	I _{OH}	-5	mA	Output (value per pin)
High level total output current	∑I _{OH}	-50	mA	Total for all output pins
Low level output current	I _{OL}	15	mA	All pins excluding large current output pins (value per pin)
	I _{OLC}	20	mA	Large current output pins* ³ (value per pin)
Low level total output current	∑I _{OL}	130	mA	Total for all output pins
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP-100P-L01
		380	mW	LQFP-100P-L01
		500	mW	LFLGA-104P-02

*1 AV_{DD} and AV_{REF} must be the same voltage with V_{DD}.

*2 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*3 The large current drive transistor is N-ch transistor of PD.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	2.7	3.3	V	
		2.2	3.3	V	Guaranteed operation range with TEX clock
		2.2	3.3	V	Guaranteed operation range for clock mode
		2.0	3.3	V	Guaranteed data hold range during stop mode
	AV _{DD}	2.7	3.3	V	*1
	AV _{REF}	2.7	3.3	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS Schmitt input*3
	V _{IHEX}	0.7V _{DD}	V _{DD} +0.3	V	EXTAL, TEX
Low level input voltage	V _{IL}	0	0.2V _{DD}	V	*2
	V _{ILS}	0	0.2V _{DD}	V	CMOS Schmitt input*3
	V _{ILEX}	-0.3	0.3V _{DD}	V	EXTAL, TEX
Operating temperature	T _{opr}	-20	+75	°C	

*1 AV_{DD} and AV_{REF} must be the same voltage with V_{DD}.

*2 PC4 to PC7, PD, PE, PF0, PG2, PG6, PI7, PJ for normal input port.

*3 PB4, PB6, PB7, PC0 to PC3, PF1 to PF3, PF5, PG0, PG1, PG3 to PG5, PG7, PH6, PH7, PI0 to PI6, $\overline{\text{RST}}$.

Electrical Characteristics

DC Characteristics

(Topr = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA, PB, PD, PE, PF4 to PF7, PG, PH0 to PH5, PJ	V _{DD} = 2.7V, I _{OH} = -0.15mA	2.4			V
			V _{DD} = 2.7V, I _{OH} = -0.5mA	2.0			V
		PC	V _{DD} = 2.7V, I _{OH} = -0.05mA	1.3			V
Low level output voltage	V _{OL}	PA, PB, PC4 to PC7, PE, PF4 to PF7, PG, PH0 to PH5, PJ	V _{DD} = 2.7V, I _{OL} = 1.2mA			0.3	V
			V _{DD} = 2.7V, I _{OL} = 1.6mA			0.5	V
		PC0 to PC3 (SCL0, SCL1, SDA0, SDA1)	V _{DD} = 2.7V, I _{OL} = 2.0mA			0.3	V
			V _{DD} = 2.7V, I _{OL} = 3.0mA			0.5	V
		PD	V _{DD} = 2.7V, I _{OL} = 5.0mA			1.0	V
Input current	I _{IHE}	EXTAL	V _{DD} = 3.3V, V _{IH} = 3.3V	0.3		20	μA
	I _{ILE}		V _{DD} = 3.3V, V _{IL} = 0.3V	-0.3		-20	μA
	I _{ILR}	$\overline{\text{RST}}^{*1}$	V _{DD} = 3.3V, V _{IL} = 0.3V	-0.9		-250	μA
	I _{IL}	PC ^{*2}				-250	μA
			V _{DD} = 2.7V, V _{IH} = 2.4V	-1.0			μA
I/O leakage current	I _{Iz}	PA, PB, PD to PG, PH6, PH7, PI, PJ, AN1 to AN3, $\overline{\text{TEX}}$, $\overline{\text{RST}}^{*1}$	V _{DD} = 3.3V, V _I = 0, 3.3V			±10	μA
Open drain output leakage current (N-ch Tr. off state)	I _{ILOH}	PC ^{*2}	V _{DD} = 3.3V, V _{IH} = 3.3V			10	μA
Supply current ^{*3}	I _{DD1} ^{*4}	V _{DD} , V _{SS}	V _{DD} = 3.0 ± 0.3V, 20MHz crystal oscillation, A/D off state (C1 = C2 = 10pF)		12	20	mA
	I _{DD2}		V _{DD} = 3.0 ± 0.3V, 32kHz crystal oscillation, 20MHz oscillation stop, A/D off state (C1 = C2 = 47pF)		25	50	μA
	I _{DDS1} ^{*4}		V _{DD} = 3.0 ± 0.3V, 20MHz crystal oscillation, A/D off state (C1 = C2 = 10pF), sleep mode		5	10	mA
	I _{DDS2}		V _{DD} = 3.0 ± 0.3V, 32kHz crystal oscillation, 20MHz oscillation stop, A/D off state (C1 = C2 = 47pF), sleep mode		10	25	μA
	I _{DDS3}		V _{DD} = 3.0V, 32kHz crystal oscillation, 20MHz oscillation stop (C1 = C2 = 47pF), clock mode		5	15	μA
	I _{DDS4}		V _{DD} = 3.0V, stop mode				10

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	PA, PB0 to PB4, PB6, PB7, PC to PE, PF0 to PF3, PF5, PG, PH6, PH7, PI, PJ, AN1 to AN3, EXTAL, TEX, $\overline{\text{RST}}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 $\overline{\text{RST}}$ specifies the input current when pull-up resistor has been selected; the leakage current when no resistor has been selected.

*2 PC specifies the input current when pull-up resistor has been selected; the leakage current when no resistor has been selected.

*3 When all output pins are open.

*4 When the upper two bits (PCK1, PCK0) of the clock control register (CLC: 0002FEh) are set to "00" and the LSI is operated in high-speed mode (2 frequency dividing clock).

AC Characteristics

(1) Clock timing

(Topr = -20 to +75°C, VDD = 2.7 to 3.3V, VSS = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit	
Main clock base oscillation frequency	fEX	EXTAL, XTAL	Fig.1	VDD = 3.0 ± 0.3V	15	20	20.5	MHz
Main clock base oscillation input pulse width	tXH	EXTAL	Fig.1, Fig.2 External clock drive	VDD = 3.0 ± 0.3V	20			ns
	tXL							
Main clock base oscillation input rise time, fall time	tXR	EXTAL	Fig.1, Fig.2 External clock drive	VDD = 3.0 ± 0.3V			14	ns
	tXF							
Sub clock base oscillation frequency	fTEX	TEX, TX	Fig.1	VDD = 2.2 to 3.3V	32.735	32.768	33.096	kHz
Sub clock base oscillation input pulse width	tTH	TEX	Fig.1, Fig.2 External clock drive	VDD = 3.3V	15.3			μs
	tTL			VDD = 2.2V	15.3			μs
Sub clock base oscillation input rise time, fall time	tTR	TEX	Fig.1, Fig.2 External clock drive	VDD = 3.3V			200	ns
	tTF			VDD = 2.2V			200	ns

Note) tsys indicates the four values below according to the upper two bits (PCK1,PCK0) of the clock control register (CLC: 0002FEh) during main mode and tsys = 2/fTEX = 61.04μs during sub mode.
 tsys [ns] = 2/fEX (PCK1, PCK0 = 00), 4/fEX (PCK1, PCK0 = 01), 8/fEX (PCK1, PCK0 = 10), 16/fEX (PCK1, PCK0 = 11)

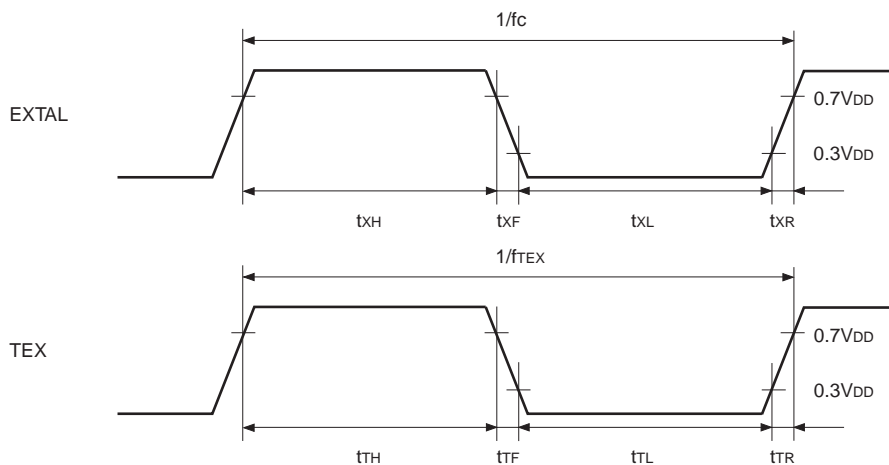


Fig.1. Clock timing

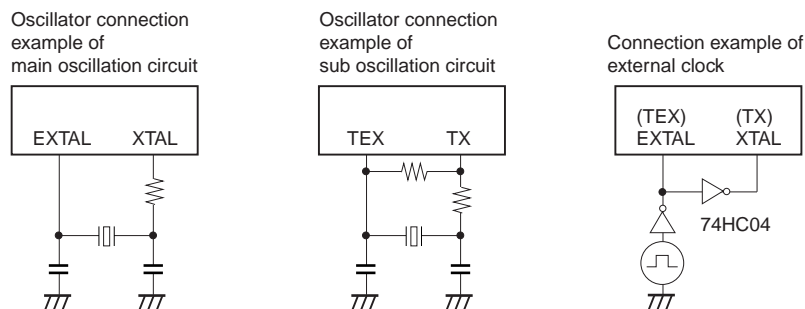


Fig.2. Oscillator connection and clock applied conditions

(2) Event count input

(Topr = -20 to +75°C, VDD = 2.7 to 3.3V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
Event count input clock pulse width	t_{EH} , t_{EL}	\overline{EC}	Fig.3	$t_{sys} + 100$		ns

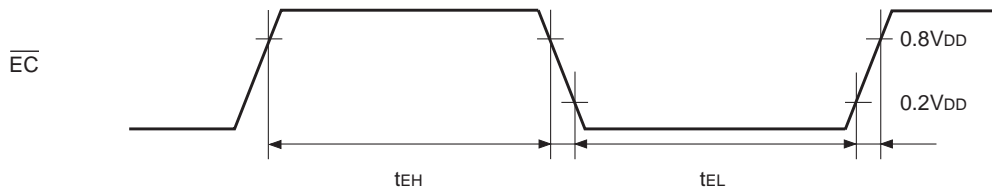


Fig.3. Event count input timing

(3) Interruption and reset input

(Topr = -20 to +75°C, VDD = 2.7 to 3.3V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit	
External interruption high, low level width	t_{IH} , t_{IL}	\overline{NMI} INT0 to INT7 KS0 to KS15	Main mode Sub mode Sleep mode	$t_{sys} + 100$		ns	
			Clock mode Stop mode	1		μs	
		INT4 to INT7	Noise filter selected	ϕ	$2t_{sys} + 100$		ns
				PS4	$32/f_{EX} + 100$		
	PS6	$128/f_{EX} + 100$					
Reset input low level width	t_{RST}	\overline{RST}	Fig.5	$3t_{sys} + 200$		ns	

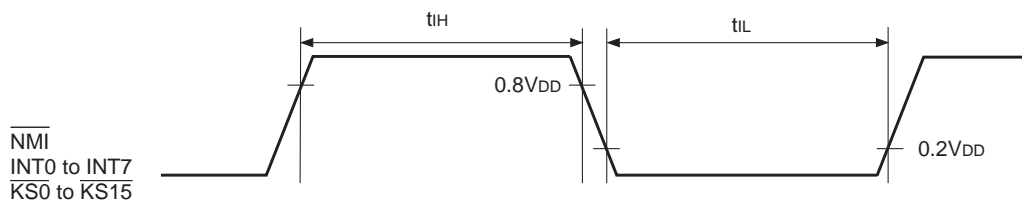


Fig.4. Interruption input timing

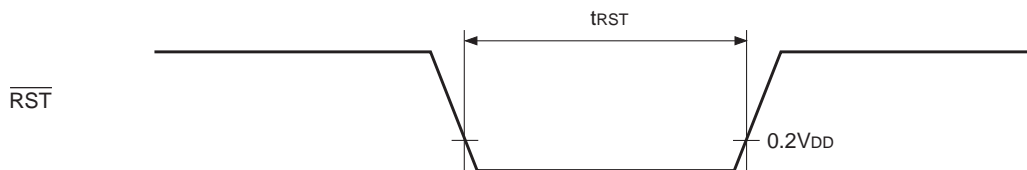


Fig.5. Reset input timing

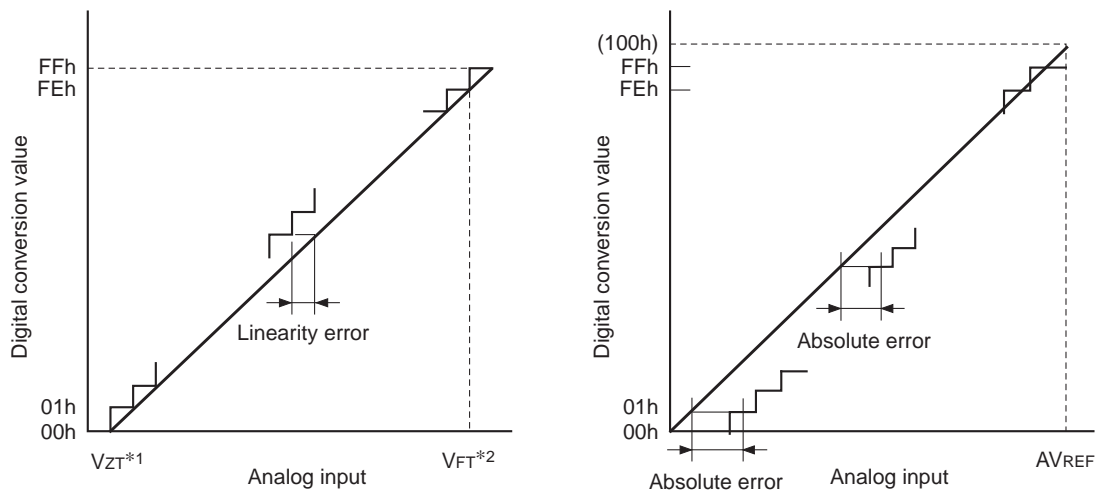
(4) A/D converter characteristics

(Topr = -20 to +75°C, V_{DD} = AV_{DD} = AV_{REF} = 2.7 to 3.3V, V_{SS} = AV_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			V _{DD} = AV _{DD} = AV _{REF} = 3.0V			±1	LSB
Absolute error						±3	LSB
Conversion time	t _{CONV}			34t _{sys}			µs
Sampling time	t _{SAMP}			9t _{sys}			µs
Reference input voltage	V _{REF}	AV _{REF}	V _{DD} = AV _{DD} = AV _{REF}	2.7		3.3	V
Analog input voltage	V _{IAN}	AN0 to AN23		0		AV _{REF}	V
AV _{REF} current	I _{REF}	AV _{REF0} AV _{REF1}	Main mode Sub mode		1.1	1.5	mA
	I _{REFS}		Clock mode Stop mode during ADC off state			10	µA

* When Bit 14 (ADOFF) of A/D control status register (ADCS0: 00013Ch,ADCS1: 00014Ch) is specified to "1".

Note) AV_{DD} and AV_{REF} must be the same voltage with V_{DD}.



*1 V_{ZT}: Value at which the digital conversion value changes from 00h to 01h and vice versa.
 *2 V_{FT}: Value at which the digital conversion value changes from FEh to FFh and vice versa.

Fig.6. Definition of A/D converter terms

(5) Serial transfer (CH0, CH1, CH2)

(Topr = -20 to +75°C, V_{DD} = 2.7 to 3.3V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t _{DCSK}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	External start transfer mode (SCK = output mode)		1.5t _{sys} + 200	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ float delay time	t _{DCSKF}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	External start transfer mode (SCK = output mode)		1.5t _{sys} + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t _{DCSO}	SO0 SO1 SO2	External start transfer mode		1.5t _{sys} + 200	ns
$\overline{CS} \uparrow \rightarrow SO$ float delay time	t _{DCSOF}	$\overline{CS0}$ $\overline{CS1}$ $\overline{CS2}$	External start transfer mode		1.5t _{sys} + 200	ns
\overline{CS} high level width	t _{WHCS}	$\overline{CS0}$ $\overline{CS1}$ $\overline{CS2}$	External start transfer mode	t _{sys} + 100		ns
\overline{SCK} cycle time	t _{KCY}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	Input mode	2t _{sys} + 200		ns
			Output mode	16/f _{EX}		ns
\overline{SCK} high, low pulse width	t _{KH} t _{KL}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	Input mode	t _{sys} + 100		ns
			Output mode	8/f _{EX} - 100		ns
SI input data setup time (for $\overline{SCK} \uparrow$)	t _{SIK}	SI0 SI1 SI2	\overline{SCK} input mode	100		ns
			\overline{SCK} output mode	200 - t _{sys}		ns
SI input data hold time (for $\overline{SCK} \uparrow$)	t _{KSI}	SI0 SI1 SI2	\overline{SCK} input mode	t _{sys} + 100		ns
			\overline{SCK} output mode	t _{sys} + 100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t _{KSO}	SO0 SO1 SO2	\overline{SCK} input mode		t _{sys} + 150	ns
			\overline{SCK} output mode		100	ns
Minimum interval time	t _{INT}	$\overline{SCK0}$ $\overline{SCK1}$ $\overline{SCK2}$	\overline{SCK} input mode	3t _{sys} + 100		ns
			\overline{SCK} output mode	8/f _{EX} - 100		ns

Note) The load condition for the \overline{SCK} output mode and SO output delay time is 100pF.

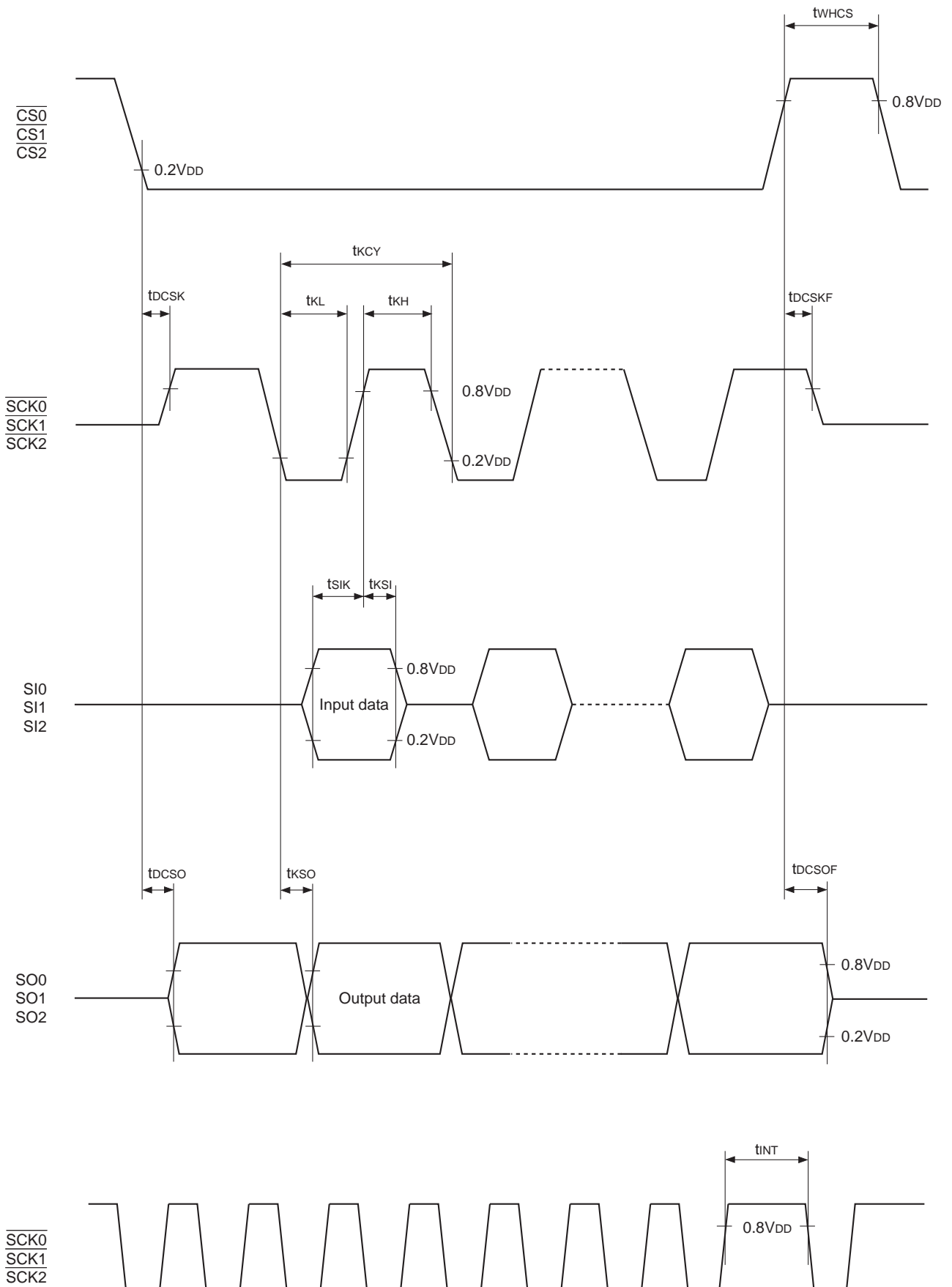


Fig.7. Serial transfer CH0, CH1, CH2 timing

(6) Serial transfer (CH3) [SIO mode]

(Topr = -20 to +75°C, V_{DD} = 2.7 to 3.3V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
SCK cycle time	t _{KCY}	SCK3	Input mode	2t _{sys} + 200		ns
			Output mode	16/f _{EX}		ns
SCK high, low pulse width	t _{KH} t _{KL}	SCK3	Input mode	t _{sys} + 100		ns
			Output mode	8/f _{EX} - 100		ns
SI input data setup time (for SCK ↑)	t _{SIK}	SI3	SCK input mode	100		ns
			SCK output mode	200		ns
SI input data hold time (for SCK ↑)	t _{KSI}	SI3	SCK input mode	t _{sys} + 100		ns
			SCK output mode	200		ns
SCK ↓ → SO delay time	t _{KSO}	SO3	SCK input mode		t _{sys} + 150	ns
			SCK output mode		100	ns

Note) The load condition for the SCK output mode and SO output delay time is 100pF.

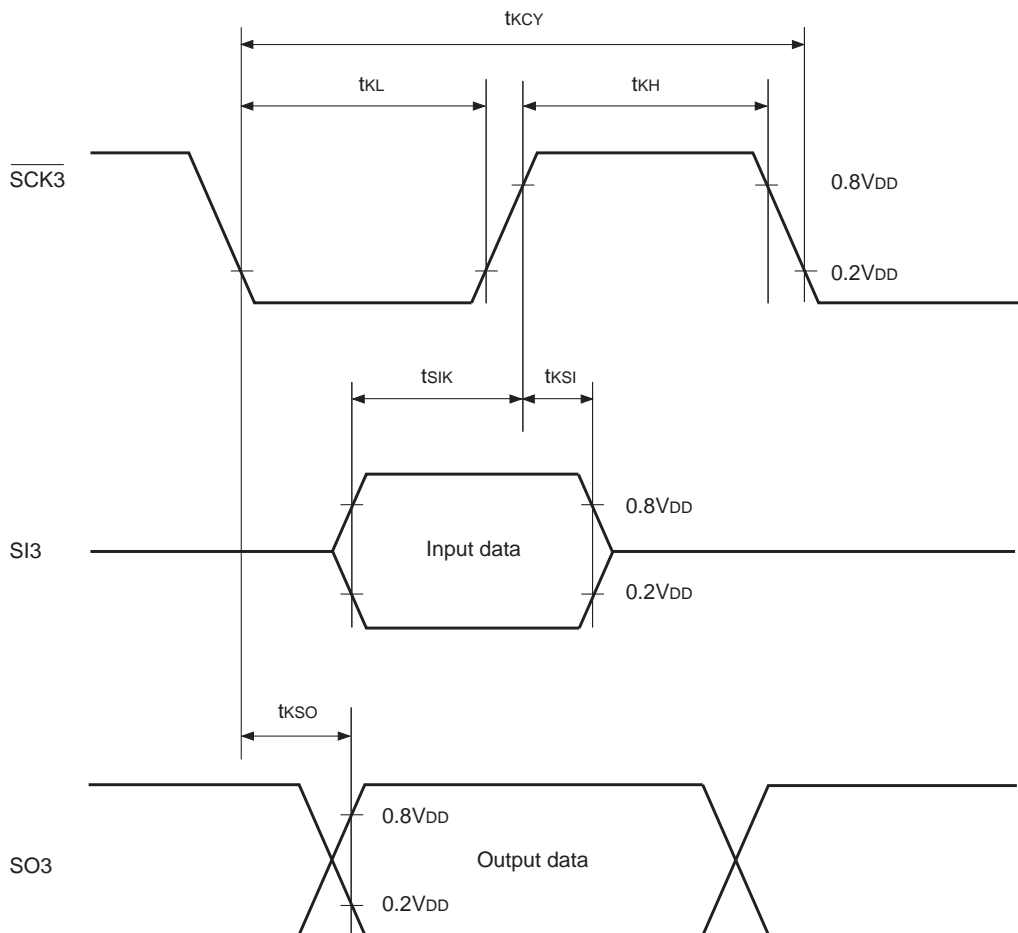


Fig.8. Serial transfer CH3 timing (SIO mode)

(7) Serial transfer (CH3) [Special mode]

(Topr = -20 to +75°C, V_{DD} = 2.7 to 3.3V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
SO cycle time*	t _{LCY}	SO3 SI3	f _{EX} = 20MHz		104		μs
SI input setup time	t _{LSU}	SI3		2			
SI input hold time	t _{LHD}	SI3		2			
Input start bit high level width	t _{LSBH}	SI3	Communication slave mode	1			
SI → SO delay time	t _{LIO}	SO3				1	

* When lower 2 bits (SCK1, SCK0) of serial mode register (SIOM3: 0001A4h) is specified to "00".

Note) The load condition for the SO output delay time is 100pF.

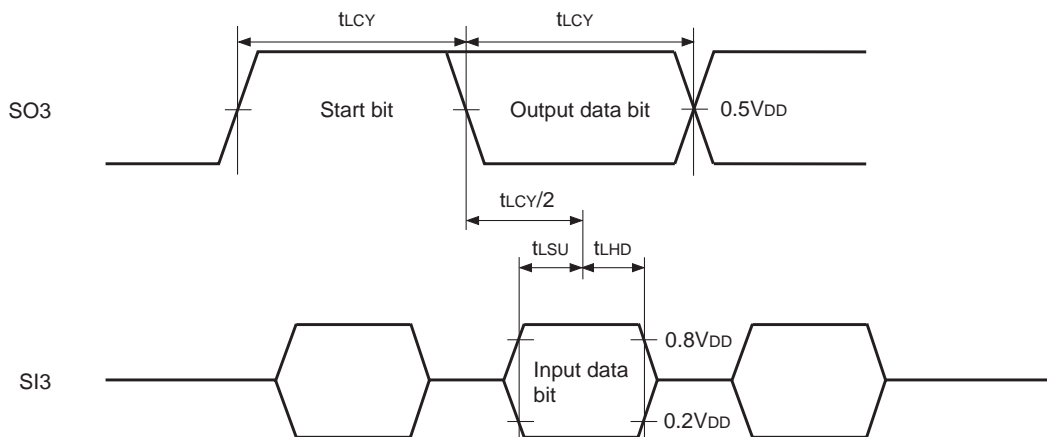


Fig.9. Serial transfer CH3 timing (Special mode)

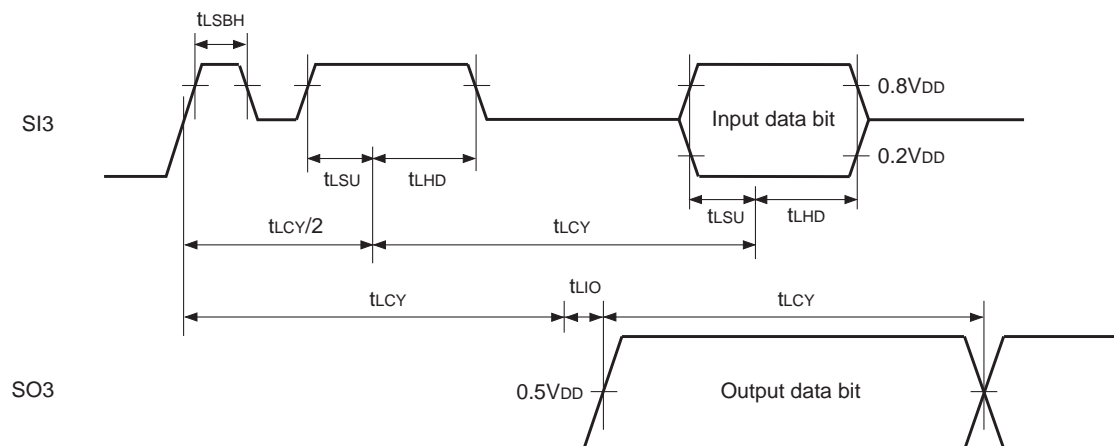


Fig.10. Serial transfer CH3 timing (Special mode)

(8) I²C bus (CH0, CH1)

(Topr = -20 to +75°C, V_{DD} = 2.7 to 3.3V, V_{SS} = 0V reference)

Item	Symbol	Pins	Standard mode		High-speed mode		Unit
			Min.	Max.	Min.	Max.	
SCK clock frequency	t _{SCL}	SCL0 SCL1	0	100	0	400	kHz
Bus free time between stop and start conditions	t _{BUF}	SDA0 SDA1	4.7		1.3		μs
Hold time under (resend) start condition	t _{HD;STA}	SDA0, SDA1 SCL0, SCL1	4.0		0.6		μs
Hold time in SCL clock low state	t _{Low}	SCL0 SCL1	4.7		1.3		μs
Hold time in SCL clock high state	t _{High}	SCL0 SCL1	4.0		0.6		μs
Setup time under (resend) start condition	t _{SU;STA}	SDA0, SDA1 SCL0, SCL1	4.7		0.6		μs
Data hold time	t _{HD;DAT}	SDA0, SDA1 SCL0, SCL1	0		0	0.9	μs
Data setup time	t _{SU;DAT}	SDA0, SDA1 SCL0, SCL1	250		100		ns
SCL, SDA signal output rise time	t _{Rd} t _{Rc}	SDA0, SDA1 SCL0, SCL1		1000	20 + α*	300	ns
SCL, SDA signal output fall time	t _{Fd} t _{Fc}	SDA0, SDA1 SCL0, SCL1		300	20 + α*	300	ns
Setup time under stop condition	t _{SU;STO}	SDA0, SDA1 SCL0, SCL1	4.0		0.6		μs

* Due to the total capacitance of the bus.

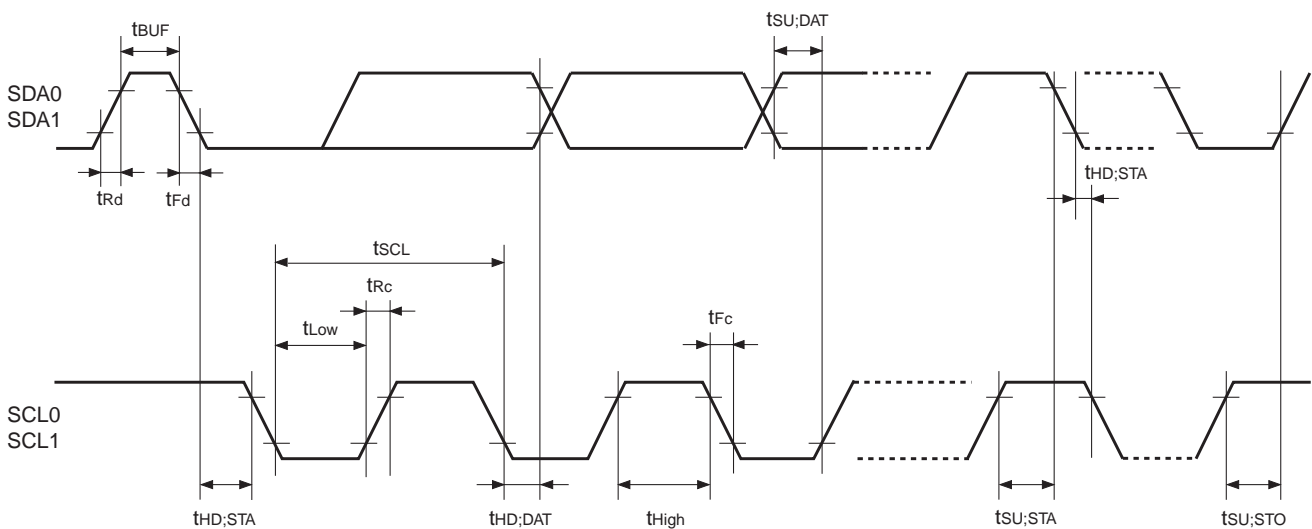


Fig.11. I²C bus timing

(9) Remote control reception

(Topr = -20 to +75°C, V_{DD} = 2.7 to 3.3V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit	
Remote control receive high, low level width	t _{RMC}	RMC	Main mode	PS5 selected	128/f _{EX} + 100		ns
				PS7 selected	512/f _{EX} + 100		
				PS9 selected	2048/f _{EX} + 100		
				32k selected	4/f _{TEX} + 100		
			Sub mode	8/f _{TEX} + 100			

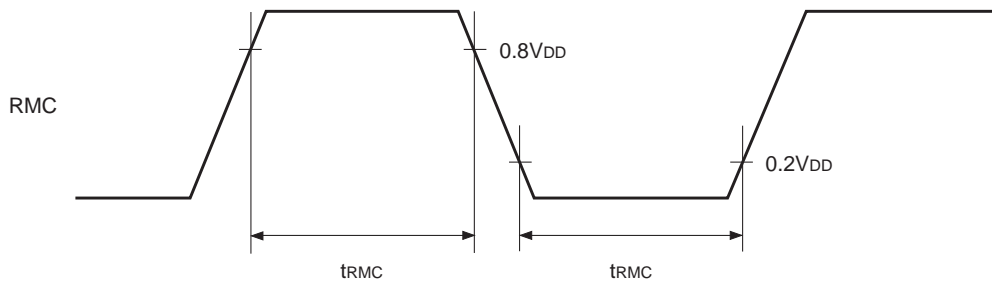


Fig.12. Remote control signal input timing

Appendix

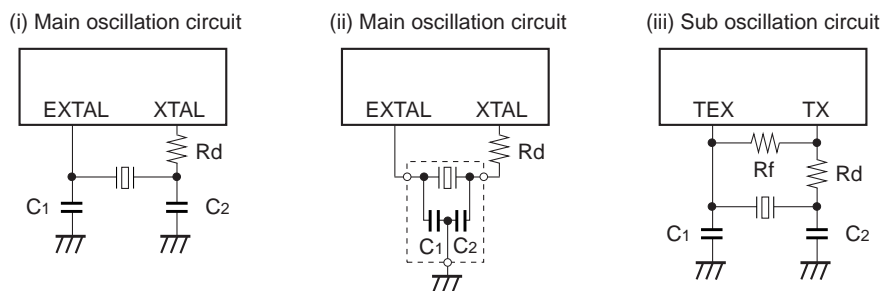


Fig.13. Recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C ₁ (pF)	C ₂ (pF)	R _d (Ω)	Circuit example	Remarks
MURATA MFG CO., LTD.	CSA12.0MG	12.0	30	30	0	(i)	
	CSA16.00MXZ040	16.0	15	15	0		
	CSA20.00MXZ040	20.00	10	10	0		
	CST12.0MTW*	12.0	30	30	0	(ii)	
	CST16.00MXW0C3*	16.0	15	15	0		
RIVER ELETEC CO., LTD.	HC-49/U03	12.00	10	10	220	(i)	CL = 10pF
KINSEKI LTD.	HC-49/U-S	12.0	12	12	1.0k	(i)	CL = 12pF
		16.0	12	12	470		
		20.0	12	12	390		
TDK Corporation	CCR12.0MSC5*	12.0	20 (±20%)	20 (±20%)	0	(ii)	
	CCR16.0MSC6*	16.0	10 (±20%)	10 (±20%)			
	CCR20.0MSC6*	20.0	10 (±20%)	10 (±20%)			
Seiko Instruments Inc.	VTC-200 SP-T	32.768kHz	20	18	150k	(iii)	R _f = 10MΩ CL = 12.5pF

* Indicates types with on-chip grounding capacitor (C₁, C₂). CCR***: Surface mounted type ceramic oscillator.
CL : Load capacitor

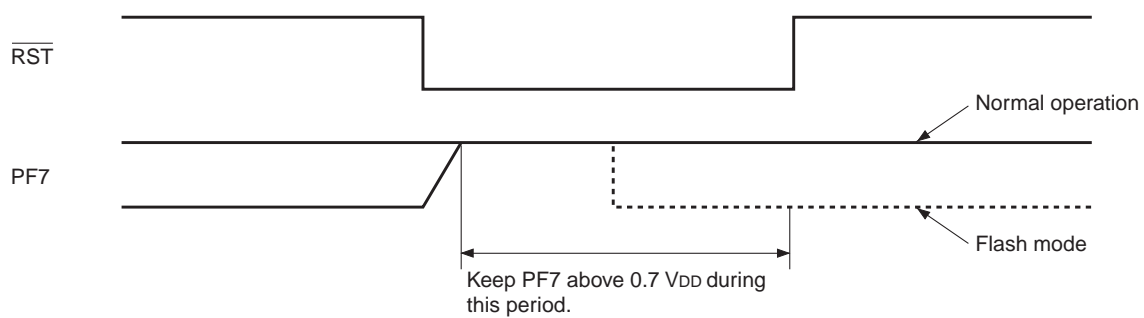
Mask option table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent

Notes on PF7 Usage

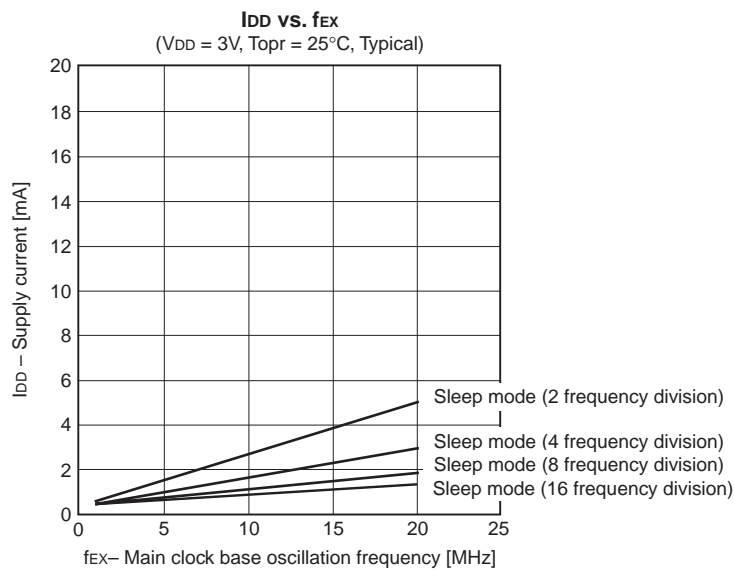
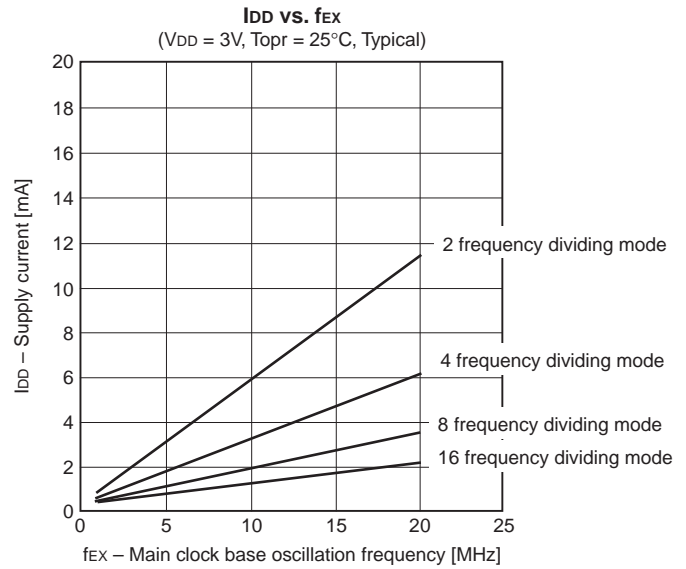
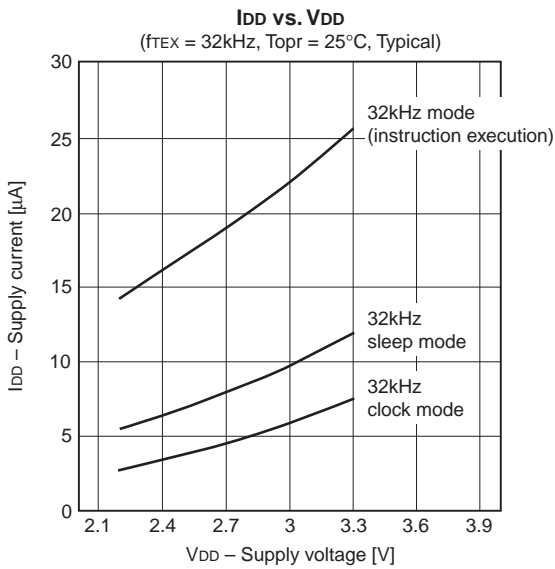
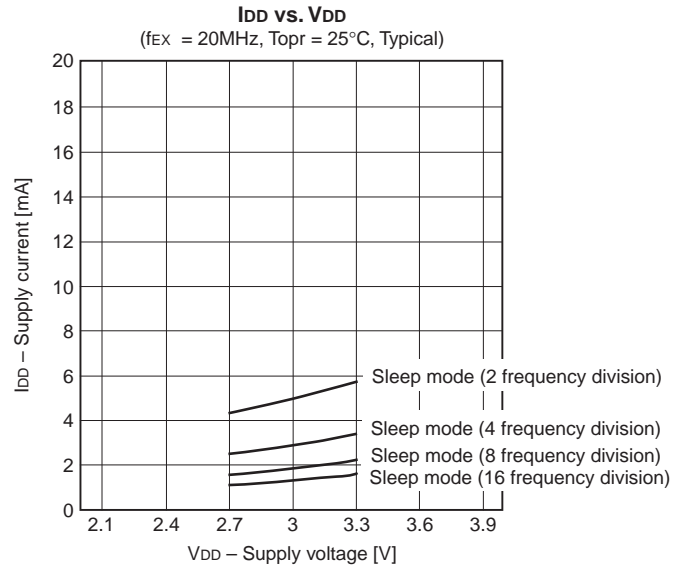
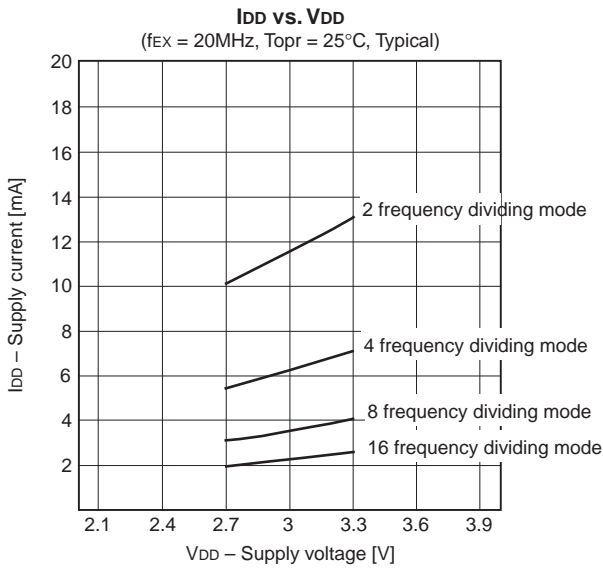
FLASH EEPROM incorporated PF7 is also used as flash mode setting function. Note the followings:

1. "H" is output to PF7 during a reset. That is driven at comparatively high impedance (approximately 150 k Ω), and take care that V_{OH} should not fall under 0.7 V_{DD} by the partial pressure with external circuit load impedance.
2. When using software reset functions, PF7 may not rise enough during a reset. Switching PF7 to "H" output prior to software reset execution or connecting pull-up resistor is recommended.



Mask ROM and piggy/evaluation chip do not have flash mode setting function. Considering that EEPROM incorporated type is used, above countermeasure should be performed.

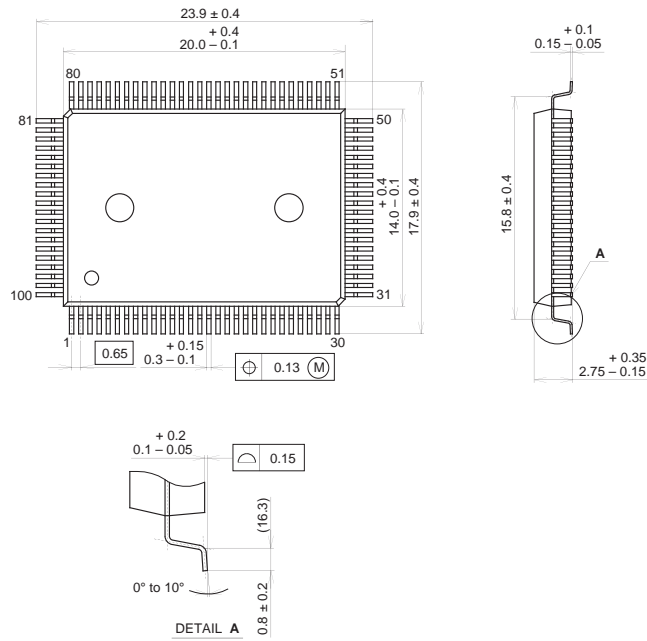
Characteristics Curve



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

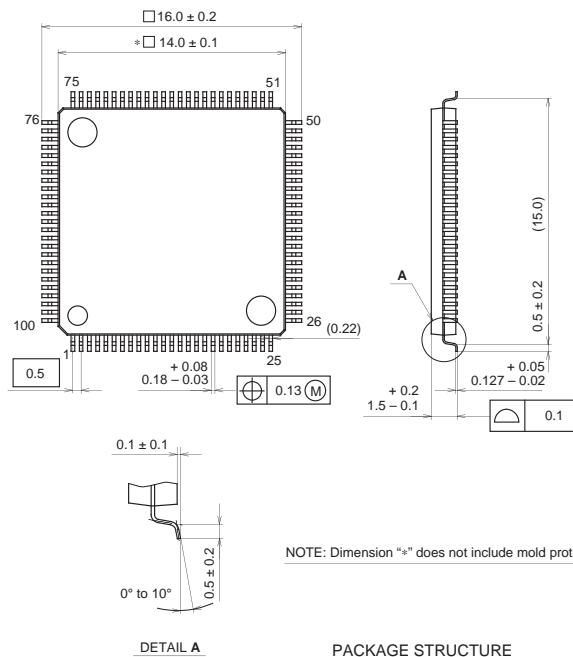


PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN LQFP (PLASTIC)



NOTE: Dimension "s" does not include mold protrusion.

PACKAGE STRUCTURE

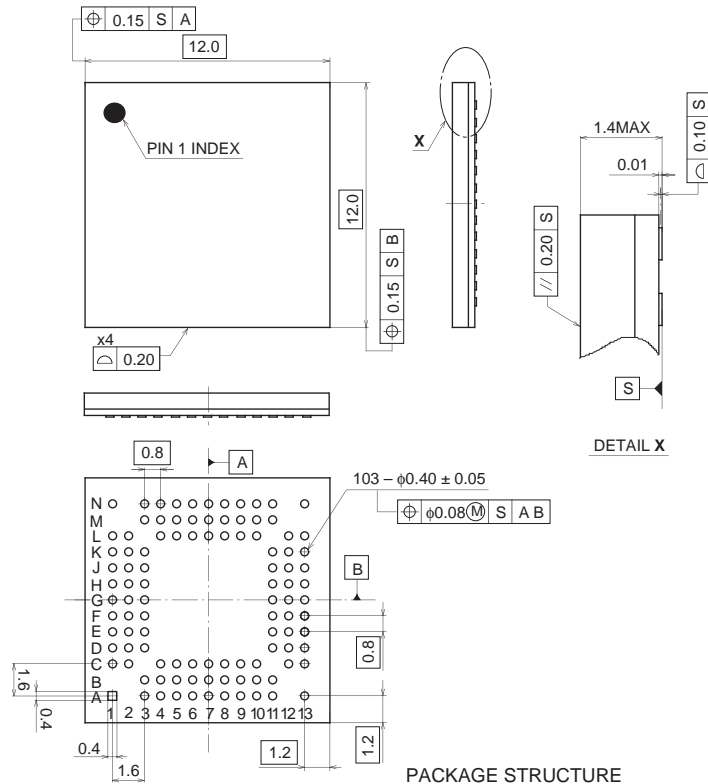
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EIAJ CODE	LQFP100-P-1414
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.8g

Package Outline

Unit: mm

104PIN LFLGA



PACKAGE STRUCTURE

SONY CODE	LFLGA-104P-02
EIAJ CODE	LFLGA104-P-1212
JEDEC CODE	

PACKAGE MATERIAL	ORGANIC SUBSTRATE
TERMINAL TREATMENT	GOLD PLATING
TERMINAL MATERIAL	NICKEL PLATING
PACKAGE MASS	0.4g