

## 74F114

### Dual JK Negative Edge-Triggered Flip-Flop with Common Clocks and Clears

#### General Description

The 74F114 contains two high-speed JK flip-flops with common Clock and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on  $\bar{S}_D$  or  $\bar{C}_D$  prevents clocking and forces Q or  $\bar{Q}$  HIGH, respectively.

Simultaneous LOW signals on  $\bar{S}_D$  and  $\bar{C}_D$  force both Q and  $\bar{Q}$  HIGH.

#### Asynchronous Inputs:

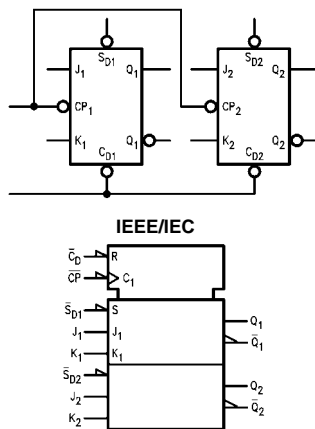
- LOW input to  $\bar{S}_D$  sets Q to HIGH level
- LOW input to  $\bar{C}_D$  sets Q to LOW level
- Clear and Set are independent of Clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

#### Ordering Code:

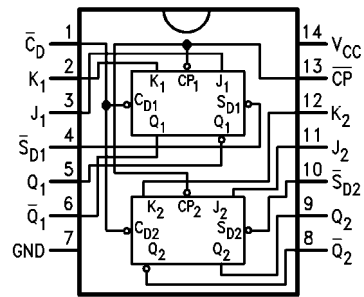
Order Number	Package Number	Package Description
74F114SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74F114PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Logic Symbols



#### Connection Diagram



### Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$J_1, J_2, K_1, K_2$	Data Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	1.0/8.0	20 $\mu$ A/-4.8 mA
$\overline{CD}$	Direct Clear Input (Active LOW)	1.0/10.0	20 $\mu$ A/-6.0 mA
$\overline{SD}_1, \overline{SD}_2$	Direct Set Inputs (Active LOW)	1.0/5.0	20 $\mu$ A/-3.0 mA
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs	50/33.3	-1 mA/20 mA

### Truth Table

Inputs					Outputs	
$\overline{SD}$	$\overline{CD}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	$\sim$	h	h	$\overline{Q}_0$	$Q_0$
H	H	$\sim$	l	h	L	H
H	H	$\sim$	h	l	H	L
H	H	$\sim$	l	l	$Q_0$	$\overline{Q}_0$

H (h) = HIGH Voltage Level

L (l) = LOW Voltage Level

X = Immaterial

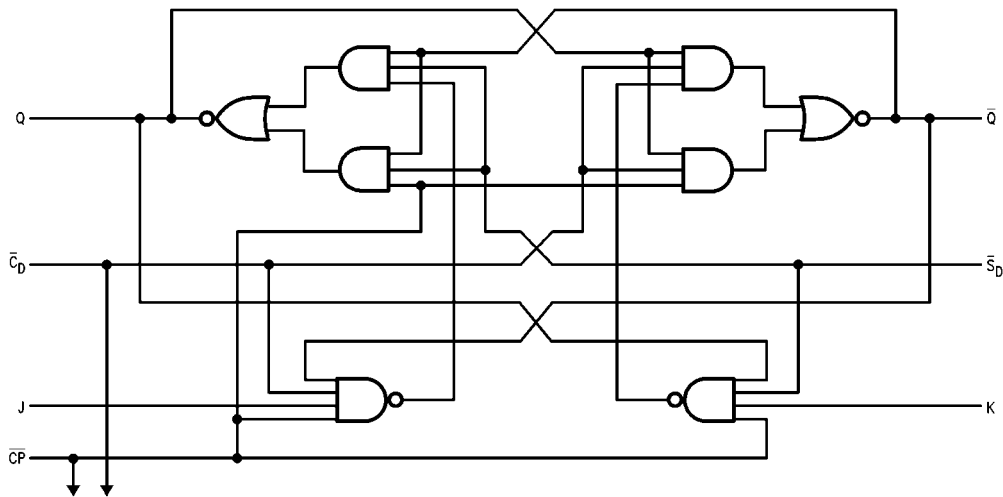
$\sim$  = HIGH-to-LOW Clock Transition

$Q_0$  ( $\overline{Q}_0$ ) = Before HIGH-to-LOW Transition of Clock

Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

### Logic Diagram

(one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

Voltage Applied to Output

in HIGH State (with V<sub>CC</sub> = 0V)Standard Output -0.5V to V<sub>CC</sub>

3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I<sub>OL</sub> (mA)**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

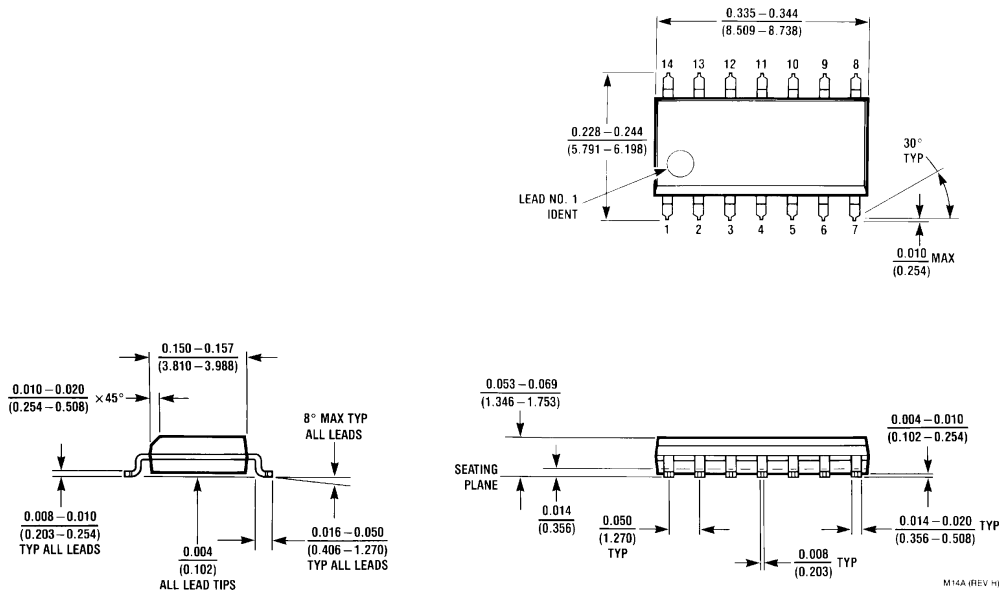
**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 5% V <sub>CC</sub>	2.5 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEx</sub>	Output High Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6 -3.0 -4.8 -6.0	mA	Max	V <sub>IN</sub> = 0.5V (J <sub>n</sub> , K <sub>n</sub> ) V <sub>IN</sub> = 0.5V ( $\bar{S}_{Dn}$ ) V <sub>IN</sub> = 0.5V (C $\bar{P}$ ) V <sub>IN</sub> = 0.5V ( $\bar{C}_{Dn}$ )
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		12.0	19.0	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		12.0	19.0	mA	Max	V <sub>O</sub> = LOW

AC Electrical Characteristics							
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	75	95		70		MHz
t <sub>PLH</sub>	Propagation Delay	3.0	5.0	6.5	3.0	7.5	ns
t <sub>PHL</sub>	$\overline{CP}$ to Q <sub>n</sub> or $\overline{Q}_n$	3.0	5.5	7.5	3.0	8.5	
t <sub>PLH</sub>	Propagation Delay	3.0	4.5	6.5	3.0	7.5	ns
t <sub>PHL</sub>	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q <sub>n</sub> or $\overline{Q}_n$	3.0	4.5	6.5	3.0	7.5	
AC Operating Requirements							
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V		Units	
		Min	Max	Min	Max		
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	4.0		5.0		ns	
t <sub>S</sub> (L)	J <sub>n</sub> or K <sub>n</sub> to $\overline{CP}$	3.0		3.5			
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	0		0		ns	
t <sub>H</sub> (L)	J <sub>n</sub> or K <sub>n</sub> to $\overline{CP}$	0		0			
t <sub>W</sub> (H)	$\overline{CP}$ Pulse Width	4.5		5.0		ns	
t <sub>W</sub> (L)	HIGH or LOW	4.5		5.0			
t <sub>W</sub> (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width, LOW	4.5		5.0		ns	
t <sub>REC</sub>	Recovery Time $\overline{S}_{Dn}$ , $\overline{C}_{Dn}$ , to $\overline{CP}$	4.0		5.0		ns	

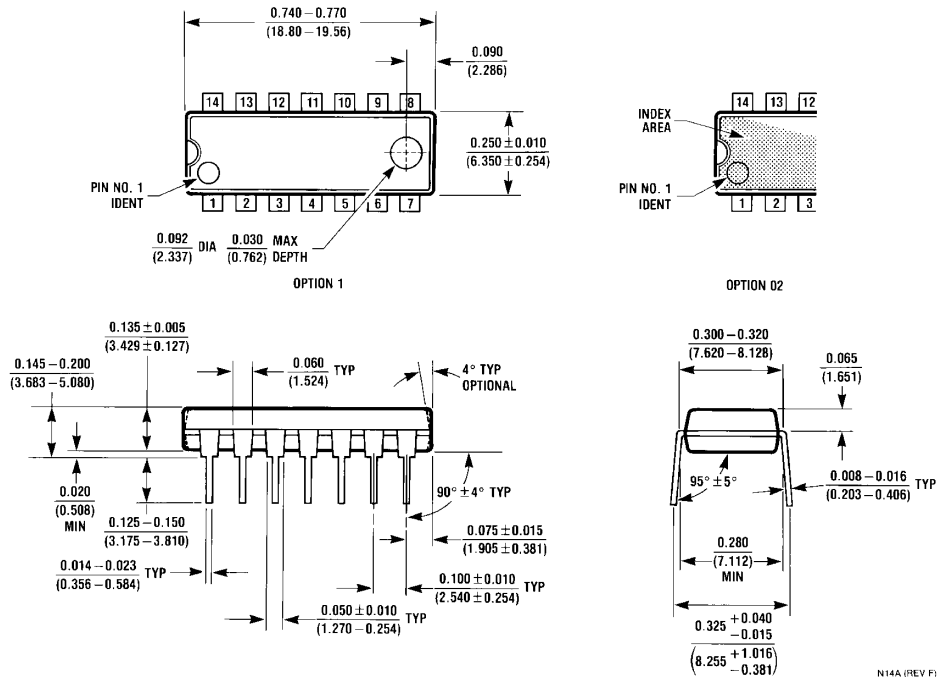
**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow  
Package Number M14A**

M14A (REV H)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A**

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