TDA2560

LUMINANCE AND CHROMINANCE CONTROL COMBINATION

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION: The TDA2560 is a monolithic integrated circuit for use in the luma and chroma sections of color television receivers. It contains the brightness, saturation and contrast control circuitry and is manufactured using the Fairchild Planar* process. It is designed to interface directly with the TDA2522 chroma demodulator. The TDA2530 may be added to provide an RGB drive to the picture tube. The TDA2560 may also be used in NTSC receivers.

LUMINANCE SECTION

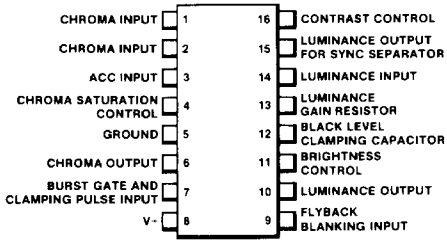
- LOW INPUT IMPEDANCE FOR EASE IN MATCHING DELAY LINE
- DC CONTRAST AND BRIGHTNESS CONTROL
- BLACK LEVEL CLAMP
- BLANKING
- ADDITIONAL VIDEO OUTPUT WITH POSITIVE SYNC

CHROMINANCE SECTION

- GAIN CONTROLLED AMPLIFIER
- CHROMA GAIN TRACKS WITH CONTRAST
- SEPARATE DC SATURATION CONTROL
- COMBINED CHROMA AND BURST OUTPUT
- BURST AMPLITUDE INDEPENDENT OF CONTRAST AND SATURATION CONTROL
- DIRECT DELAY LINE DRIVE FROM THE IC

*Planar is patented Fairchild process.

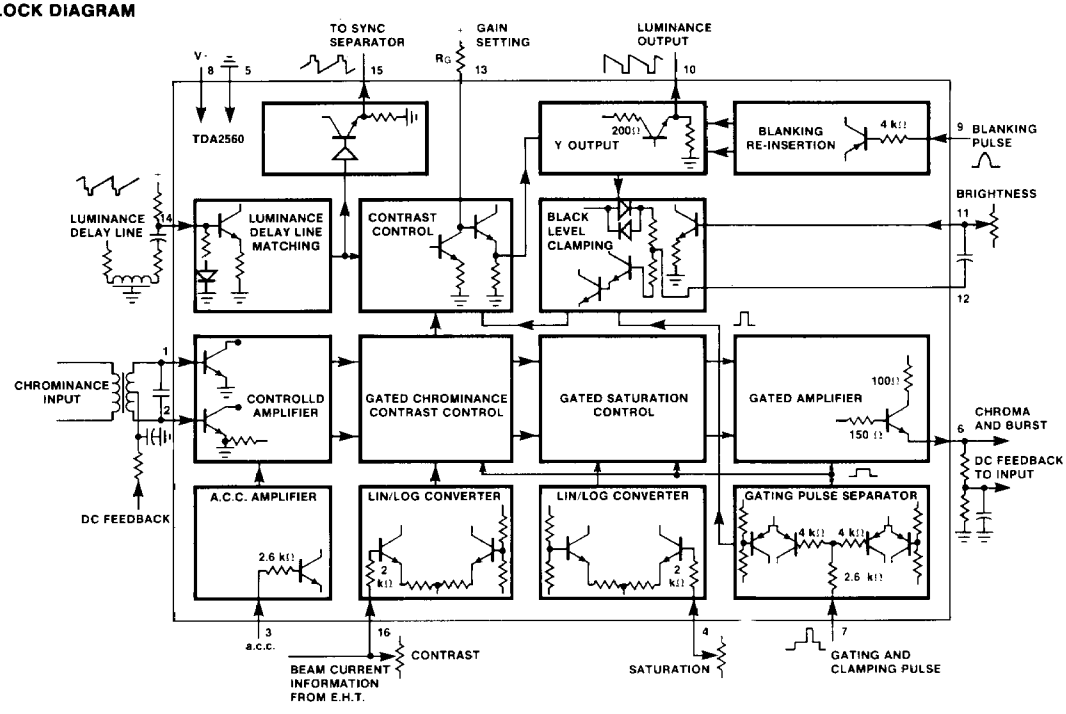
CONNECTION DIAGRAM
16-PIN DIP
PACKAGE OUTLINE 9B



ORDER INFORMATION

TYPE	PART NO.
2560	TDA2560

BLOCK DIAGRAM



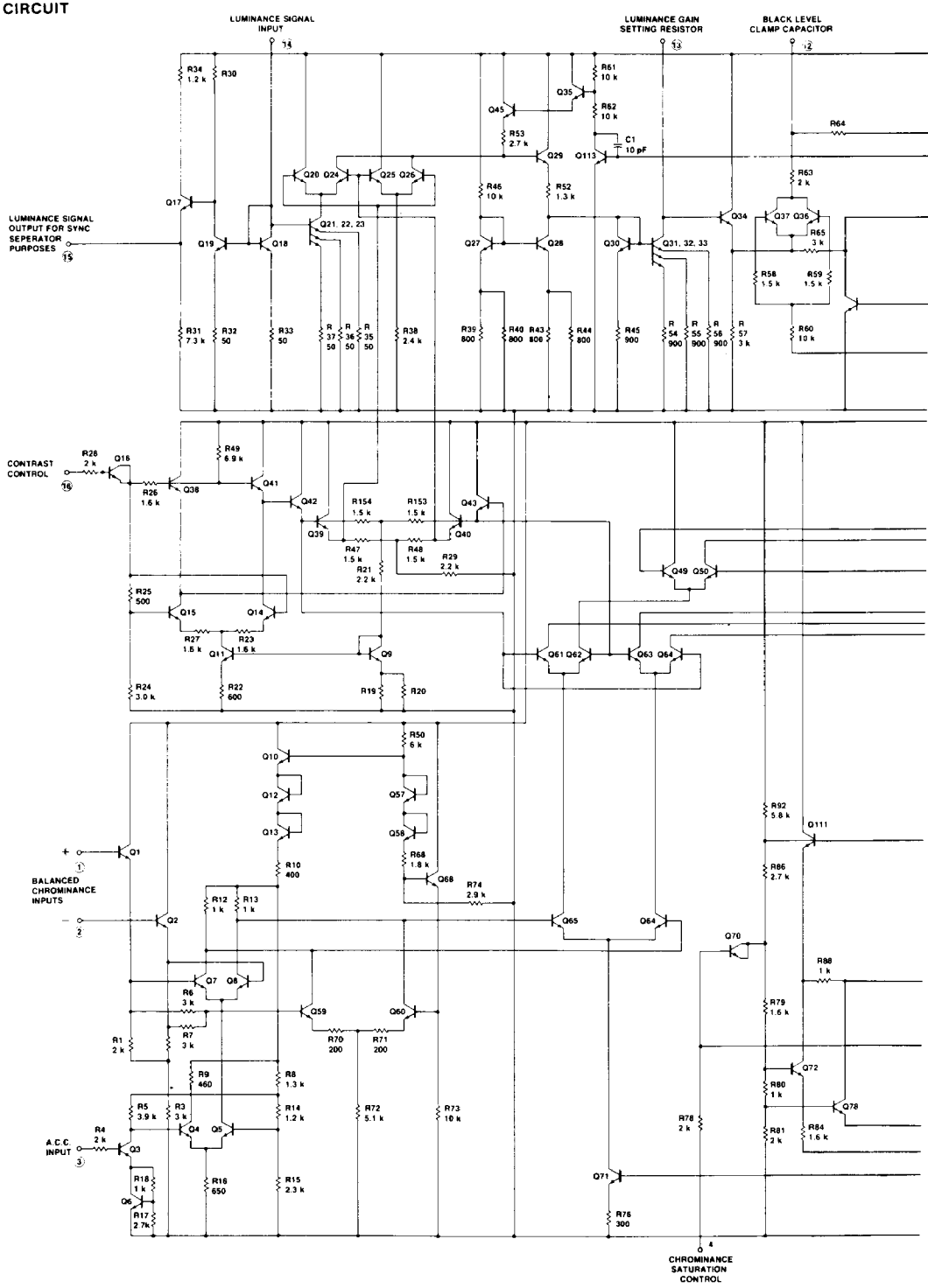
ABSOLUTE MAXIMUM RATINGS

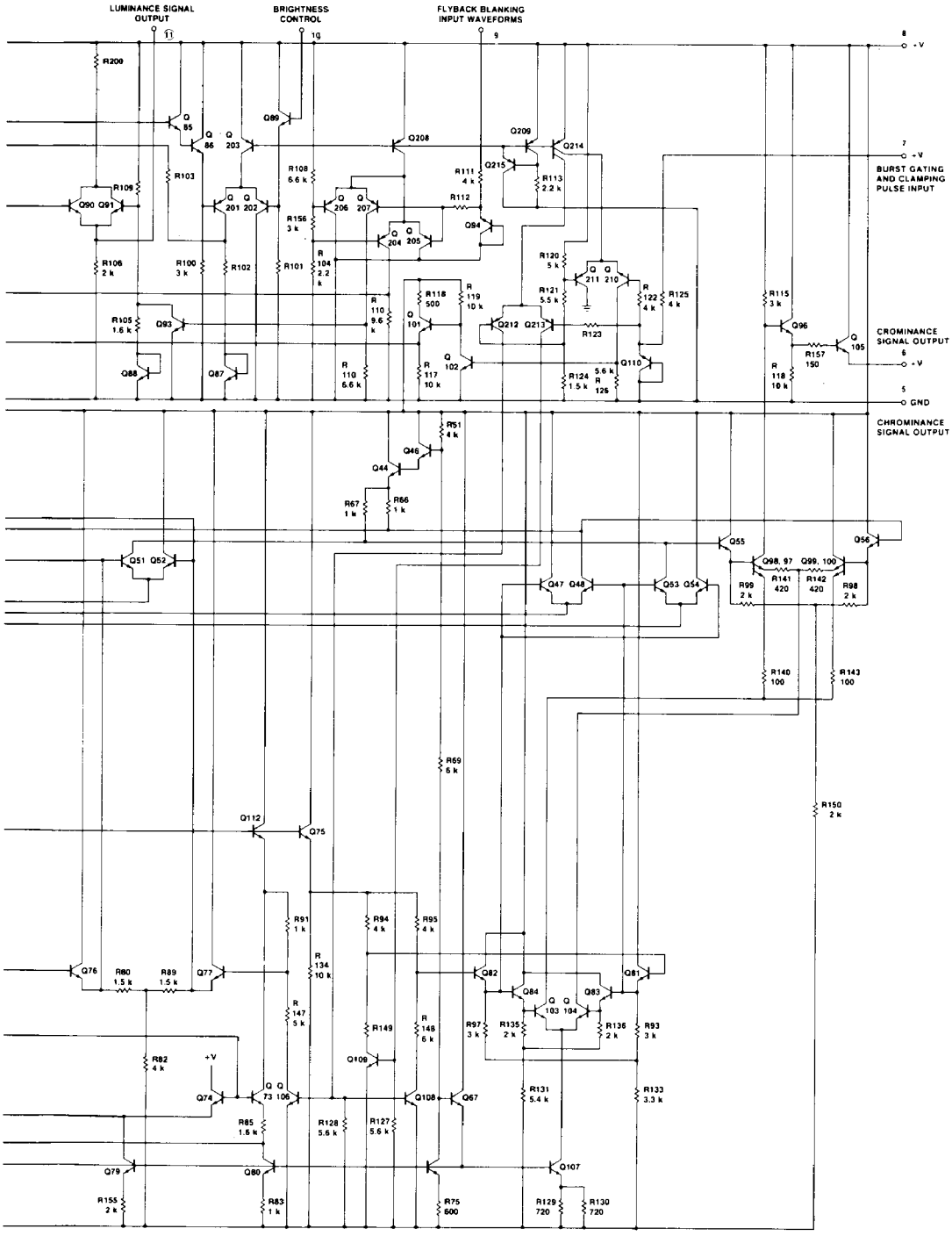
Supply Voltage	14 V
Power Dissipation	930 mW
Operating Temperature Range	0°C to +65°C
Storage Temperature Range	-55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

ELECTRICAL CHARACTERISTICS: T_A = 25°C, V+ = 12 V, R_G = 2.7 kΩ; (see test circuit unless otherwise specified).

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range (V_8)	Note 1	10	12	14	V
Supply Current (I_8)			45		mA
Allowable Hum on Supply Line				100	mV_{pk-pk}
LUMINANCE AMPLIFIER (Note 2)					
Input Signal Current (I_{14}) Black to White Value			0.2		mA
Input-Bias Current (I_{14})			0.25		mA
Input Impedance	I_{14} = 0.25 mA		150		Ω
Gain (Pin 13)	Notes 2, 5		40		dB
Contrast Control Range		20			dB
Contrast Control Voltage Range (V_{16})	See Figure 1		2-4		V
Contrast Control Current (I_{16})				8.0	μA
Black Level Range (V_{10})		1.0		3.0	V
Brightness Control Voltage Range (V_{11})			1 to 3		V
Brightness Control Current (I_{11})	$V_{11} \geq 4$ V			20	μA
Black Level Stability with Temperature			0.1		mV/°C
Black Level Stability with Contrast (V_{10}) See Applications section Pin 10	I_{14} = 0.25 mA			10	mV
Bandwidth (-3 dB)	Nominal Contrast	5.0			MHz
Output Voltage (V_{10}) (Black to White)	Max. Contrast, I_{14} = 0.2 mA		3.0		V
Output Voltage (V_{15}) (Black to White)	Sync Positive I_{14} = 0.2 mA (Black to White)		3.4		V_{pk-pk}
BLACK LEVEL CLAMP PULSE					
ON Level V_7	Note 3	7.0		V+	V
OFF Level V_7	See Figure 3			5.0	V
BLANKING PULSE	Note 4 (See Figure 4)				
ON Level V_9	V_{10} = 0 V	2.5		4.5	V
OFF Level V_9				1.5	V
ON Level V_9	V_{10} = 1.5 V	6.0		V+	V
OFF Level V_9				4.5	V
CHROMINANCE AMPLIFIER	Note 6				
Input Signal V_2		4.0		80	mV_{pk-pk}
Chroma Output Signal V_6	Nominal Contrast and Saturation V_{burst} = 1 V_{pk-pk}		2.0		V_{pk-pk}
Maximum Chroma Output V_6	V_{burst} = 1 V_{pk-pk}		4.6		V_{pk-pk}
Bandwidth (-3 dB)		6.0			MHz
Ratio of Burst to Chroma at Nominal Contrast and Saturation	See Note 2, 6, and 7		1:2		V/V
ACC Starting Voltage - V_3	Note 8		1.2		V
ACC Range		30			dB
Tracking between Luma and Chroma with Contrast Control	10 dB Contrast Control Adjustment		±1.0		dB
Saturation Control Range		20			dB
Saturation Control Voltage Range	See Figure 2		2-4		V
Gating Pulse					
ON Level V_7		2.3		5.0	V
OFF Level V_7	See Figure 3			1.0	V
Width		8.0			μs
Signal pulse Noise to Noise Ratio	Nominal Input Voltage	46			dB
Phase Shift between Burst and Chroma				5.0	°

EQUIVALENT CIRCUIT




LUMINANCE SIGNAL OUTPUT
BRIGHTNESS CONTROL
FLYBACK BLANKING INPUT WAVEFORMS
BURST GATING AND CLAMPING PULSE INPUT
CROMINANCE SIGNAL OUTPUT
CHROMINANCE SIGNAL OUTPUT
+V
GND

RELATIVE CONTRAST GAIN AS A FUNCTION OF CONTROL VOLTAGE

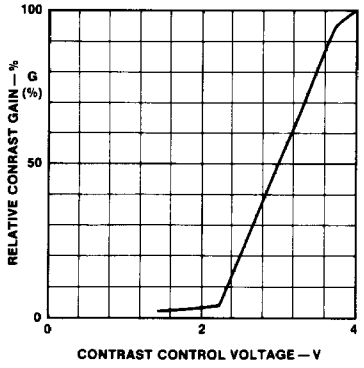


Fig. 1

RELATIVE SATURATION GAIN AS A FUNCTION OF CONTROL VOLTAGE

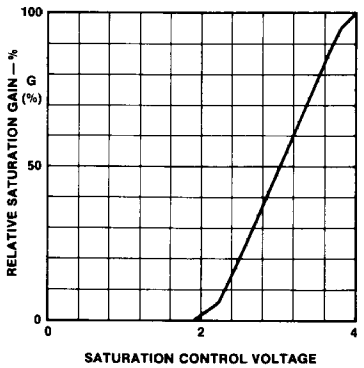


Fig. 2

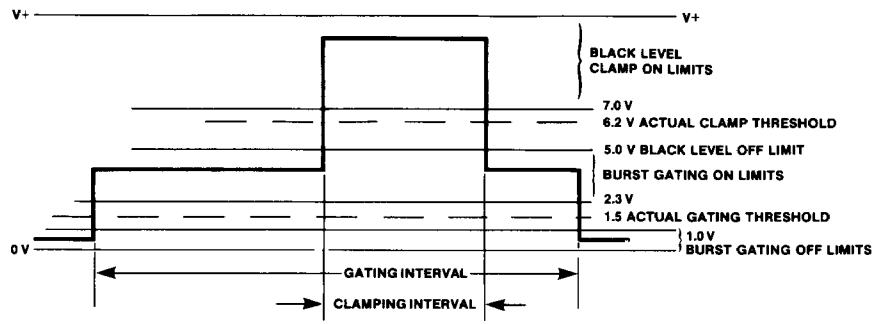


Fig. 3 PIN 7 INPUT VOLTAGE (SANDCASTLE PULSE)

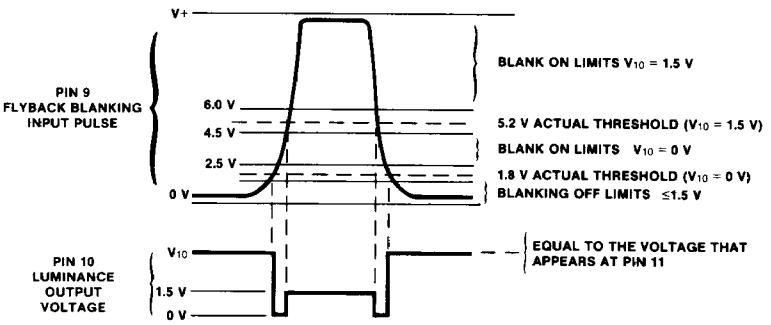


Fig. 4 DUAL THRESHOLD LUMINANCE BLANKING

NOTES:

1. Load on pin 6 is 1.5 kΩ. No load on pins 10 and 15.

2. Nominal contrast is defined as maximum contrast -3 dB
   Nominal Saturation is defined as maximum saturation -6 dB

3. This pulse (pin 7) is used for gating the chrominance amplifier and black level clamping. The latter function is actuated at +7 V. The input pulse must have an amplitude such that the clamping circuit is active only during the back porch of the blanking interval. The gating pulse switches the gain of the chroma amplifier to maximum during the flyback time, when the pulse rises above 2.3 V and switches it back to the normal setting when the pulse falls below 1 V.

4. This pulse (pin 9) is used for blanking the luminance amplifier. When the pulse exceeds +2.5 V, the output signal is blanked to a level of about 0 V. When the input exceeds +6 V, a fixed level of about +1.5 V is inserted in the output signal. This level can be used for clamping purposes.

5. The gain of the luminance amplifiers may be adjusted by varying R_G (see test circuit). R_G adjusts the gain of the contrast control circuit. This circuit configuration was chosen to keep the variation in gain to a minimum. With this design, the variation in gain is primarily a function of the ratio of the delay line matching resistors to R_G. At $R_G = 2.7\ k\Omega$, the output voltage at nominal contrast is 3 V black-to-white with an input current of 0.2 mA black-to-white. Under thse conditions the gain is;

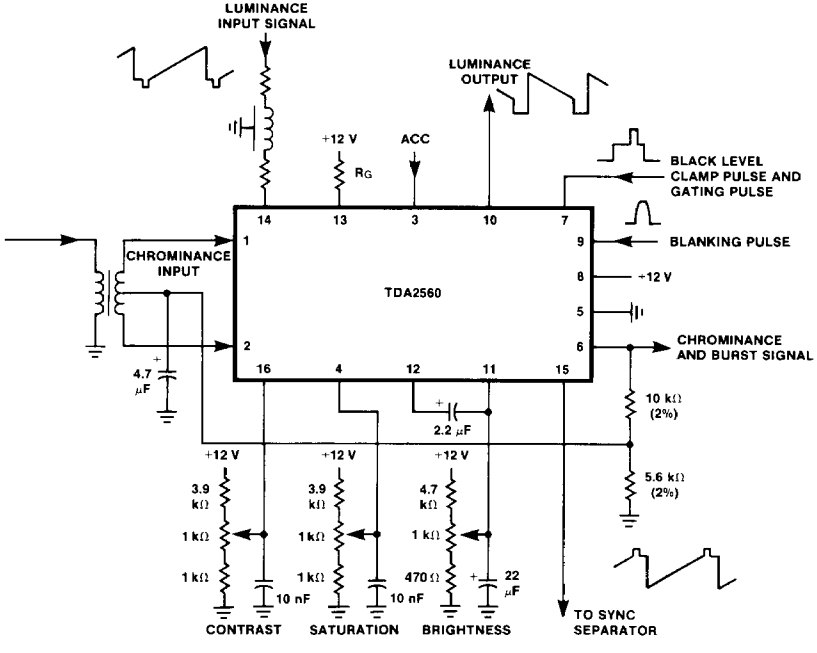
$$A\ V = 20 \log \frac{\Delta V_{OUT}}{\Delta I_{IN} \times R_{IN}} = 20 \log \left(\frac{3\ V}{(.2\ mA)\ (150\ \Omega)} \right) = 40\ dB$$

6. All measurements of the chrominance signal are based on a color bar signal with 75% saturation; i.e., the burst-to-chrominance ratio is 1:2.

7. The chrominance and burst signal are both available on this pin (6). The burst signal is not affected by the contrast and saturation control and is kept constant by the ACC circuit of the TDA2522. The output of the delay line matrix circuit, which is the input of the TDA2522, is thus automatically compensated for insertion losses. Therefore, the output signal of the TDA2560 is determined by the insertion losses of the delay line. At nominal contrast and saturation setting, the ratio of the burst to the chrominance signal at the output is typically identical to that at the input.

8. A negative-going control voltage decreases the gain.

TEST AND APPLICATION CIRCUIT



APPLICATIONS INFORMATION

A basic description of the conditions and signals at each pin is shown below:

1. **BALANCED CHROMINANCE INPUT SIGNAL (In conjunction with pin 2)**
The balanced input signal is derived from the chrominance bandpass filter, which is designed to provide a push-pull input. A signal amplitude of at least 4 mV peak-to-peak is required between pins 1 and 2. The chrominance amplifier is stabilized by an external feedback loop from the output (pin 6) to the input (pins 1 and 2). The required level at pins 1 and 2 is 3 V. All measurements of the chrominance signals are based on a color bar signal with 75% saturation: i.e., the burst-to-chrominance ratio of the input signal is 1 : 2.

2. **CHROMINANCE SIGNAL INPUT (see pin 1)**

3. **ACC INPUT**
A negative-going potential, starting at +1.2 V, gives a 40 db range of ACC. Maximum grain reduction is achieved at an input voltage of 500 mV.

4. **CHROMINANCE SATURATION CONTROL**
A control range of +6 dB to > -14 dB is provided over a range of dc potential on pin 4 from +2 to +4 V. The saturation control is a linear function of the control voltage.

5. **GROUND**

6. **CHROMINANCE SIGNAL OUTPUT**
For nominal settings of saturation and contrast controls (max. -6 dB for saturation, and max. -3 dB for contrast) both the chroma and burst are available at this pin, and in the same ratio as at the input pins 1 and 2. The burst signal is not affected by the saturation and contrast controls. The acc circuit of the TDA2522 will hold the color burst amplitude constant at the input of the TDA2522. As the PAL delay line is situated between the TDA2560 and TDA2522, there may be some variation of the nominal 1 V peak-to-peak burst output of the TDA2560, depending on the tolerances of the delay line. An external network is required from pin 6 of the TDA2560 to provide negative dc feedback in the chroma channel via pins 1 and 2.

7. **BURST GATING AND CLAMPING PULSE INPUT**
A two-level pulse is required at this pin to be used for burst gate and black level clamping. The black level clamp is activated when the pulse level is greater than 7 V. The timing of this interval should be such that no appreciable encroachment occurs into the sync pulse on picture line periods during normal operation of the receiver. The burst gate, which switches the gain of the chroma amplifier to maximum, requires that the input pulse at pin 7 should be sufficiently wide, at least 8 μs, at the actuating level of 2.3 V.

8. **V+**
Correct operation occurs within the range 10 to 14 V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design, this range may be restricted due to considerations of tracking between the power supply variations and picture contrast and chroma levels.

9. **FLYBACK BLANKING INPUT WAVEFORM**
This pin is used for blanking the luminance amplifier. When the input pulse exceeds +2.5 V, the output signal is blanked to a level of about 0 V. When the input exceeds +6 V, a fixed level of about 1.5 V is inserted in the output. This level can be used for clamping purposes.

10. **LUMINANCE SIGNAL OUTPUT**
An emitter follower provides a low impedance output signal of 3 V black-to-white amplitude at nominal contrast setting having a black level in the range 1 to 3 V. An external emitter load resistor is not required. The luminance amplitude available for nominal contrast may be modified according to the resistor value from pin 13 to the +12 V supply. At an input bias current of 0.25 mA during black level, the amplifier is compensated so that the black level shift does not exceed 10 mV as a function of contrast control setting. When the input current deviates from this value, the black level shift amounts to 100 mV/mA.

APPLICATIONS INFORMATION (continued)

11. **BRIGHTNESS CONTROL**

The black level at the luminance output (pin 10) is identical to the control voltage required at this pin. A range of black level from 1 to 3 V may be obtained.

12. **BLACK LEVEL CLAMP CAPACITOR**

13. **LUMINANCE GAIN SETTING RESISTOR**

The gain of the luminance amplifier may be adjusted by selection of the resistor value from pin 13 to +12 V. The nominal luminance output amplitude is 3 V black-to-white at pin 10 when this resistor is 2.7 kΩ, and the input current is 0.2 mA black-to-white. Maximum and minimum values of this resistor are 3.9 kΩ and 1.8 kΩ respectively.

14. **LUMINANCE SIGNAL INPUT**

A low input impedance in the form of a current sink is obtained at this pin. Nominal input current is 0.2 mA black-to-white. The luminance signal may be coupled to pin 14 using a dc blocking capacitor and, in addition, a resistor employed to give a dc current into pin 14 at black level of about 0.25 mA.

15. **LUMINANCE SIGNAL OUTPUT FOR SYNC SEPARATOR PURPOSES**

A luminance signal output with positive-going sync is available which is not affected by the contrast control or the value of resistor at pin 13. This voltage is intended for drive of sync separator circuits. The output amplitude is 3.4 V peak-to-peak when the luminance signal input is 0.2 mA black-to-white.

16. **CONTRAST CONTROL**

With 3 V on this pin, the gain of the luminance channel is such that 0.2 mA black-to-white at pin 14 gives a luminance output on pin 10 of 3 V black-to-white. The nominal value of 2.7 kΩ is then assumed for the resistor from pin 13 to the +12 V supply. The variation of control potential at pin 16 from 2 to 4 V gives -17 to +3 dB gain variation of the luminance channel. A similar variation in the chrominance channel occurs in order to provide correct tracking between the two signals.