FEATURES

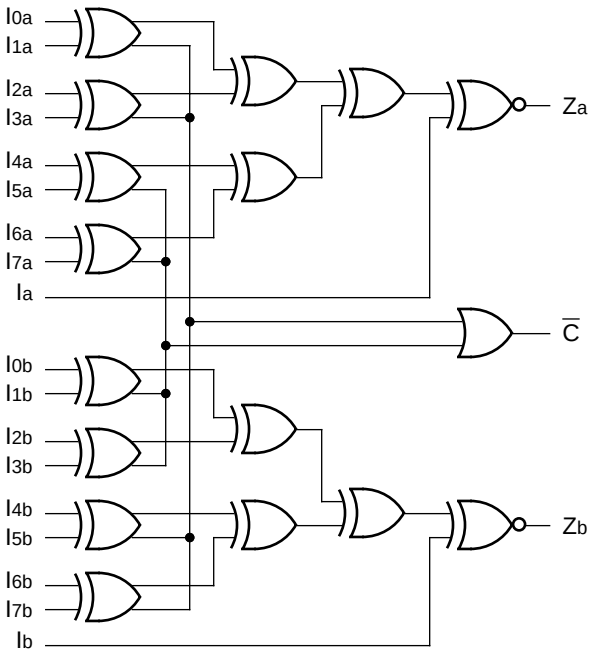
- **Max. propagation delay of 2200ps**
- **I_{EE} min. of –70mA**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option: V_{EE} = –4.2V to –5.5V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **15% faster than Fairchild 300K**
- **Approximately 30% lower power than Fairchild 300K**
- **Function and pinout compatible with Fairchild F100K**
- **Available in 24-pin CERPACK and 28-pin PLCC packages**

DESCRIPTION

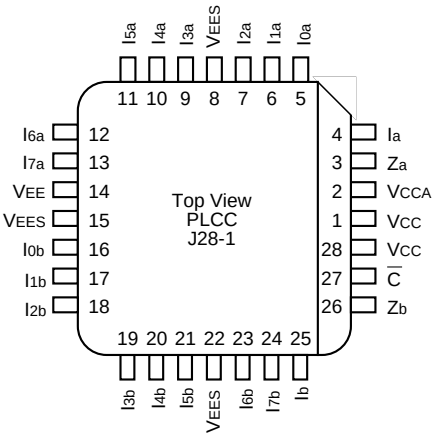
The SY100S360 is a dual parity checker/generator and is designed for use in high-performance ECL systems. The inputs are segmented into two groups of nine inputs each and the parity output is at a logic LOW when an even number of inputs are at a logic HIGH. In each group, one of the nine inputs (Ia, Ib) has a shorter propagation delay and, therefore, is ideal as the expansion input for parity generation of wider data.

A Compare output ($\overline{C}$) is also provided which allows comparison of two 8-bit words. A logic LOW on the $\overline{C}$ output indicates a match. The inputs on this device have 75KΩ pull-down resistors.

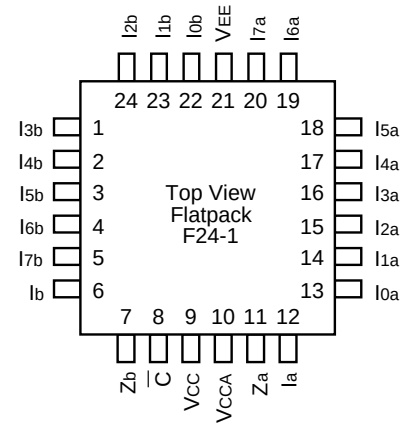
BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)



24-Pin Cerpack (F24-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S360FC	F24-1	Commercial	SY100S360FC	Sn-Pb
SY100S360FCTR[1]	F24-1	Commercial	SY100S360FC	Sn-Pb
SY100S360JC	J28-1	Commercial	SY100S360JC	Sn-Pb
SY100S360JCTR[1]	J28-1	Commercial	SY100S360JC	Sn-Pb
SY100S360JZ[2]	J28-1	Commercial	SY100S360JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S360JZTR[1, 2]	J28-1	Commercial	SY100S360JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

PIN NAMES

Pin	Function
I_a, I_b, I_{na}, I_{nb}	Data Inputs (n = 1...7)
Z_a – Z_b	Parity Odd Outputs
$\overline{C}$	Compare Output
V_{EES}	V_{EE} Substrate
V_{CCA}	V_{CCO} for ECL Outputs

TRUTH TABLE(1)

Sum of High Inputs	Output Z
Even	HIGH
Odd	LOW

Note:

1. Comparator Function:
$\overline{C} = (I_{0a} \oplus I_{1a}) + (I_{2a} \oplus I_{3a}) + (I_{4a} \oplus I_{5a}) + (I_{6a} \oplus I_{7a}) +$
$(I_{0b} \oplus I_{1b}) + (I_{2b} \oplus I_{3b}) + (I_{4b} \oplus I_{5b}) + (I_{6b} \oplus I_{7b})$

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current I_a, I_b I_{na}, I_{nb}	 — —	 — —	 300 200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–70	–45	–30	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

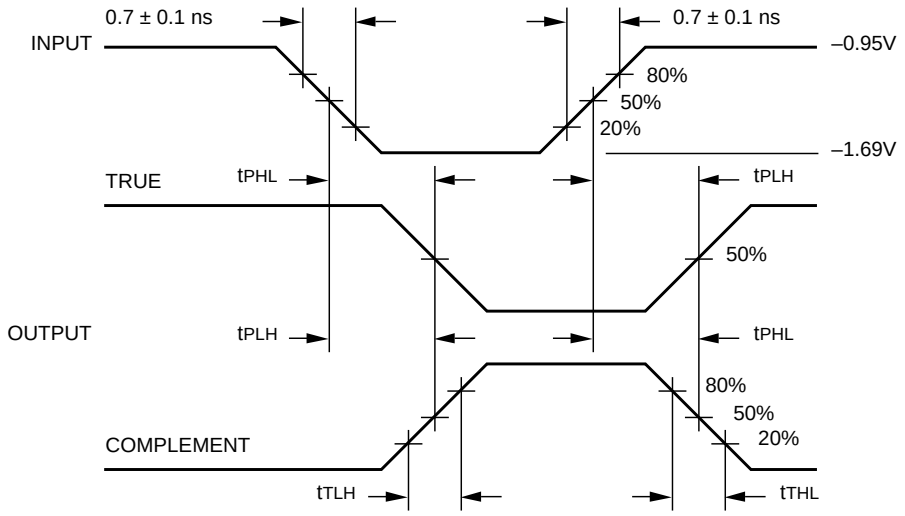
		T_A = 0°C		T_A = +25°C		T_A = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to Z_a, Z_b	500	2300	500	2300	500	2300	ps	
t_{PLH} t_{PHL}	Propagation Delay Ina, Inb to $\overline{C}$	500	1800	500	1800	500	1800	ps	
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Z_a, Z_b	300	1000	300	1000	300	1000	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

		T_A = 0°C		T_A = +25°C		T_A = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to Z_a, Z_b	500	2200	500	2200	500	2200	ps	
t_{PLH} t_{PHL}	Propagation Delay Ina, Inb to $\overline{C}$	500	1700	500	1700	500	1700	ps	
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Z_a, Z_b	300	900	300	900	300	900	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM

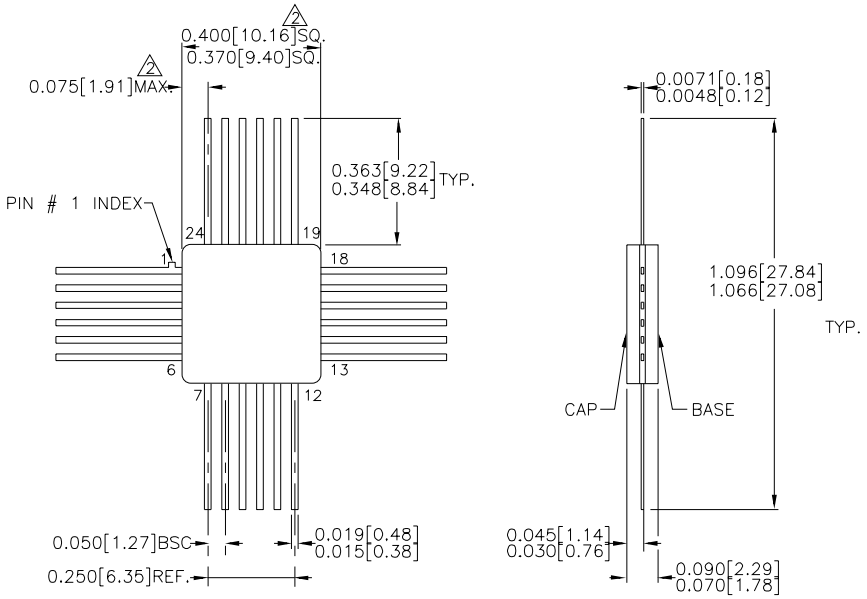


Propagation Delay and Transition Times

NOTE:

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

24-PIN CERPACK (F24-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

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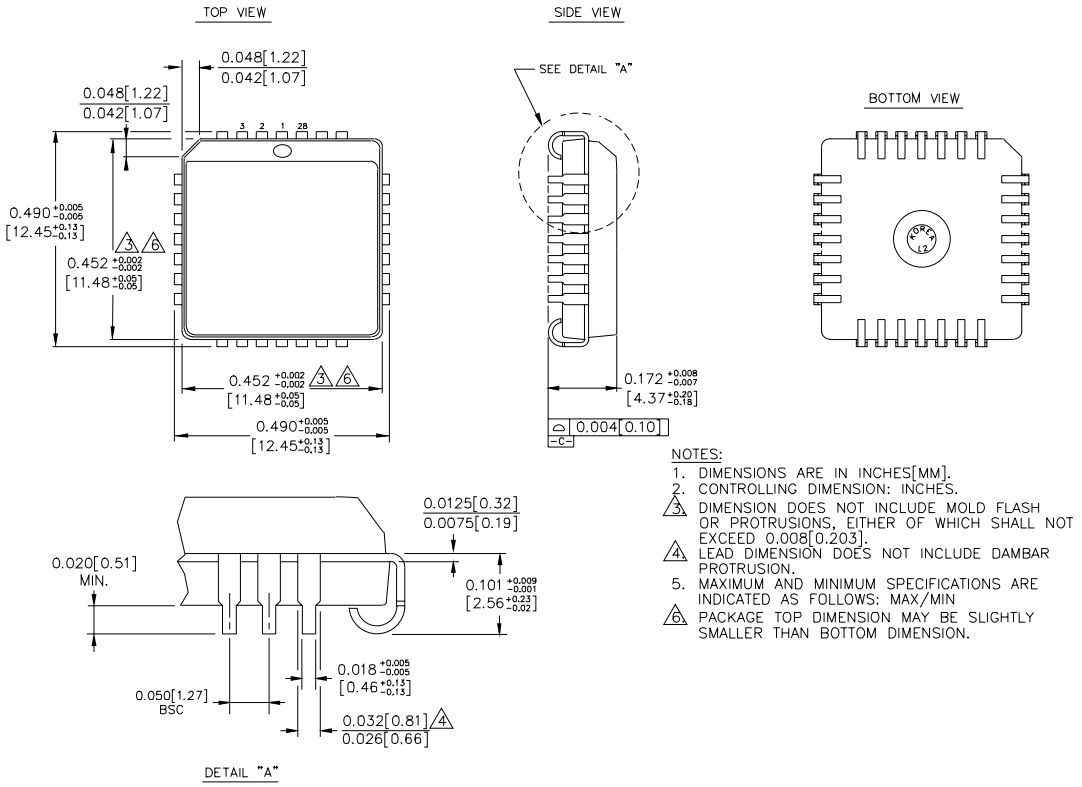
28-PIN PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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