

**FEATURES**

- Max. shift frequency of 700MHz
- Clock to Q delay max. of 1100ps
- IEE min. of -170mA
- Internal 75KΩ input pull-down resistors
- Industry standard 100K ECL levels
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- 50% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

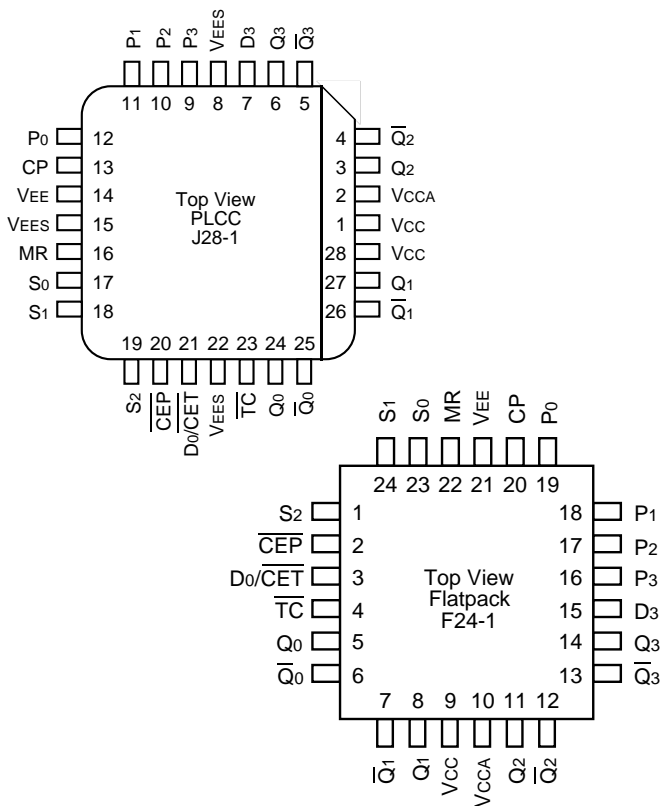
**DESCRIPTION**

The SY100S336 functions either as a modulo-16 up/down counter or as a 4-bit bidirectional shift register and is designed for use in high-performance ECL systems. Three Select inputs (Sn) are provided for determining the mode of operation. The Function Table lists the available modes of operation. In order to allow cascading for multistage counters, two Count Enable controls (CEP, CET) are provided. The CET input also functions as the Serial Data input (S0) for a shift-up operation, while the D3 input serves as the Serial Data input for the shift-down operation.

When the device is in the counting mode, the Terminal Count (TC) goes to a logical LOW when the count reaches 15 for count-up or reaches 0 for count-down. When in the shift mode, the TC output simply repeats the Q3 output.

The flexibility provided by the TC/Q3 output and the D0/CET input allows these signals to be interconnected from one stage to the next higher stage for multistage counting or shift-up operations. The individual Presets (Pn) allow initialization of the counter by entering data in parallel to preset the counter. A logic HIGH on the Master Reset (MR) overrides all other inputs and asynchronously clears the flip-flops. An additional synchronous Clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 75KΩ pull-down resistors.

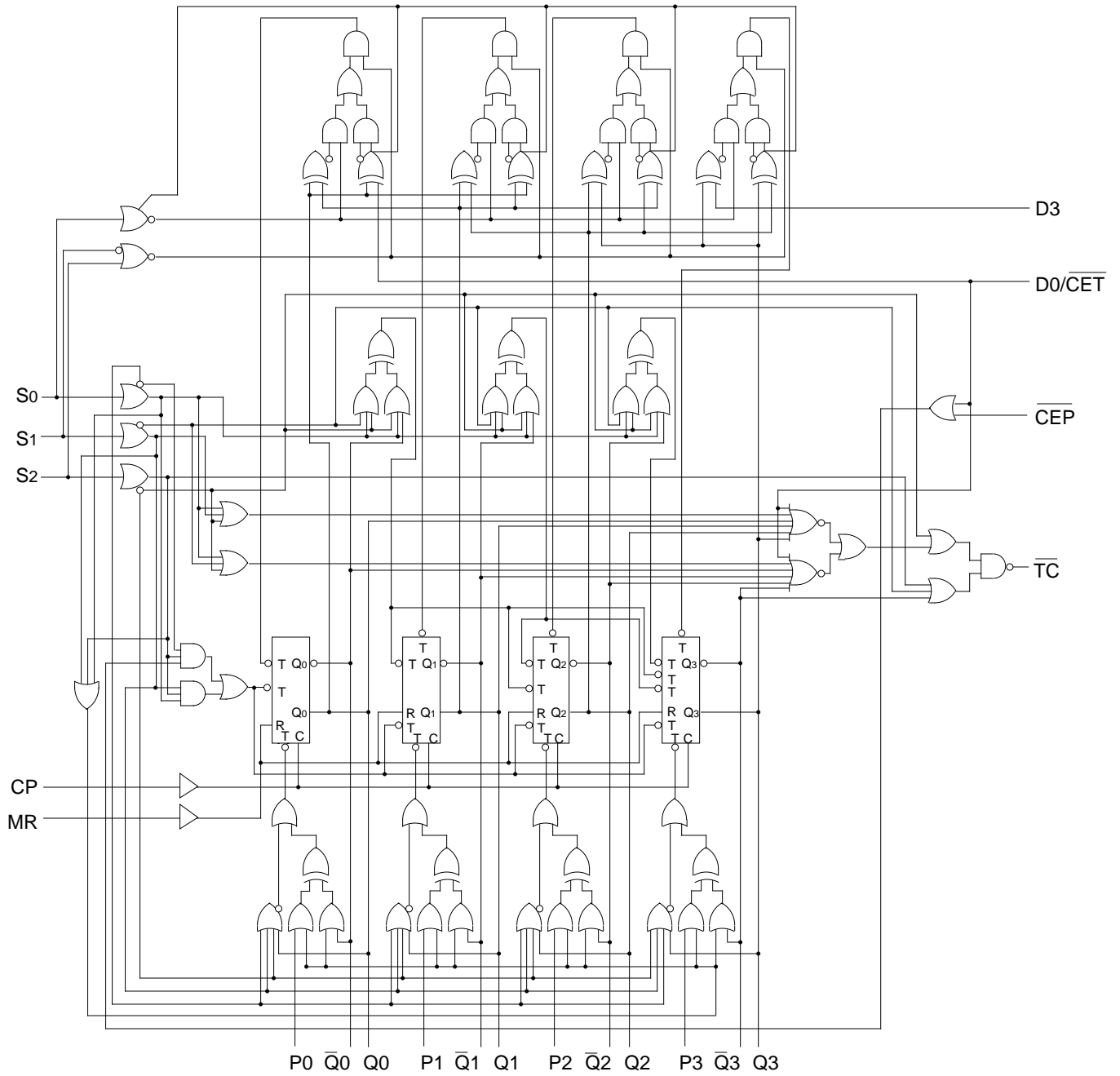
**PIN CONFIGURATIONS**



**PIN NAMES**

| Pin     | Function  |
|---------|---|
| CP      | Clock Pulse Input   |
| CEP     | Count Enable Parallel Input (Active LOW)                  |
| D0/CET  | Serial Data Input/Count Enable Trickle Input (Active LOW) |
| S0 — S2 | Select Inputs   |
| MR      | Master Reset Input  |
| VEES    | VEE Substrate   |
| VCCA    | VCCO for ECL Outputs                                      |
| P0 — P3 | Preset Inputs   |
| D3      | Serial Data Input   |
| TC      | Terminal Count Output                                     |
| Q0 — Q3 | Data Outputs  |
| Q0 — Q3 | Complementary Data Outputs                                |

**BLOCK DIAGRAM**



**TRUTH TABLE<sup>(1)</sup>**

| Inputs |                |                |                |                         |  |                |    | Outputs                     |                         |                         |                         |                        |   |
|--------|----------------|----------------|----------------|-------------------------|--|----------------|----|-----------------------------|-------------------------|-------------------------|-------------------------|------------------------|---|
| MR     | S <sub>2</sub> | S <sub>1</sub> | S <sub>0</sub> | $\overline{\text{CEP}}$ | D <sub>0</sub> / $\overline{\text{CET}}$ | D <sub>3</sub> | CP | Q <sub>0</sub>              | Q <sub>1</sub>          | Q <sub>2</sub>          | Q <sub>3</sub>          | $\overline{\text{TC}}$ | Mode  |
| L      | L              | L              | L              | X                       | X  | X              | u  | P <sub>0</sub>              | P <sub>1</sub>          | P <sub>2</sub>          | P <sub>3</sub>          | L                      | Preset (Parallel Load)                                |
| L      | L              | L              | H              | X                       | X  | X              | u  | $\overline{\text{Q}}_0$     | $\overline{\text{Q}}_1$ | $\overline{\text{Q}}_2$ | $\overline{\text{Q}}_3$ | L                      | Invert  |
| L      | L              | H              | L              | X                       | X  | X              | u  | Q <sub>1</sub>              | Q <sub>2</sub>          | Q <sub>3</sub>          | D <sub>3</sub>          | D <sub>3</sub>         | Shift Left  |
| L      | L              | H              | H              | X                       | X  | X              | u  | D <sub>0</sub>              | Q <sub>0</sub>          | Q <sub>1</sub>          | Q <sub>2</sub>          | Q <sub>3</sub> *       | Shift Right   |
| L      | H              | L              | L              | L                       | L  | X              | u  | (Q <sub>0-3</sub> ) minus 1 |                         |                         |                         | ①                      | Count Down  |
| L      | H              | L              | L              | H                       | L  | X              | X  | Q <sub>0</sub>              | Q <sub>1</sub>          | Q <sub>2</sub>          | Q <sub>3</sub>          | ①                      | Count Down with $\overline{\text{CEP}}$<br>Not Active |
| L      | H              | L              | L              | X                       | H  | X              | X  | Q <sub>0</sub>              | Q <sub>1</sub>          | Q <sub>2</sub>          | Q <sub>3</sub>          | H                      | Count Down with $\overline{\text{CET}}$<br>Not Active |
| L      | H              | L              | H              | X                       | X  | X              | u  | L                           | L                       | L                       | L                       | H                      | Clear   |
| L      | H              | H              | L              | L                       | L  | X              | u  | (Q <sub>0-3</sub> ) plus 1  |                         |                         |                         | ≠                      | Count Up  |
| L      | H              | H              | L              | H                       | L  | X              | X  | Q <sub>0</sub>              | Q <sub>1</sub>          | Q <sub>2</sub>          | Q <sub>3</sub>          | ≠                      | Count Up with $\overline{\text{CEP}}$<br>Not Active   |
| L      | H              | H              | L              | X                       | H  | X              | X  | Q <sub>0</sub>              | Q <sub>1</sub>          | Q <sub>2</sub>          | Q <sub>3</sub>          | H                      | Count Up with $\overline{\text{CET}}$<br>Not Active   |
| L      | H              | H              | H              | X                       | X  | X              | X  | Q <sub>0</sub>              | Q <sub>1</sub>          | Q <sub>2</sub>          | Q <sub>3</sub>          | H                      | Hold  |
| H      | L              | L              | L              | X                       | X  | X              | X  | L                           | L                       | L                       | L                       | L                      | Asynchronous Master<br>Reset                          |
| H      | L              | L              | H              | X                       | X  | X              | X  | L                           | L                       | L                       | L                       | L                      |   |
| H      | L              | H              | L              | X                       | X  | X              | X  | L                           | L                       | L                       | L                       | L                      |   |
| H      | L              | H              | H              | X                       | X  | X              | X  | L                           | L                       | L                       | L                       | L                      |   |
| H      | H              | L              | L              | X                       | L  | X              | X  | L                           | L                       | L                       | L                       | L                      |   |
| H      | H              | L              | H              | X                       | H  | X              | X  | L                           | L                       | L                       | L                       | H                      |   |
| H      | H              | L              | L              | X                       | X  | X              | X  | L                           | L                       | L                       | L                       | H                      |   |
| H      | H              | H              | L              | X                       | X  | X              | X  | L                           | L                       | L                       | L                       | H                      |   |

**NOTE:**

1. H = High Voltage Level

L = Low Voltage Level

X = Don't Care

u = LOW-to-HIGH Transition

① = L if Q<sub>0</sub> – Q<sub>3</sub> = LLLLH if Q<sub>0</sub> – Q<sub>3</sub> ≠ LLLL≠ = L if Q<sub>0</sub> – Q<sub>3</sub> = HHHHH if Q<sub>0</sub> – Q<sub>3</sub> ≠ HHHH\* Before the clock,  $\overline{\text{TC}}$  is Q<sub>3</sub>; after the clock,  $\overline{\text{TC}}$  is Q<sub>2</sub>**DC ELECTRICAL CHARACTERISTICS**V<sub>EE</sub> = -4.2V to -5.5V unless otherwise specified, V<sub>CC</sub> = V<sub>CCA</sub> = GND

| Symbol          | Parameter                      | Min. | Typ. | Max. | Unit | Condition                                |
|-----------------|--------------------------------|------|------|------|------|--|
| I <sub>IH</sub> | Input HIGH Current, All Inputs | —    | —    | 200  | μA   | V <sub>IN</sub> = V <sub>IH</sub> (Max.) |
| I <sub>EE</sub> | Power Supply Current           | -170 | -145 | -90  | mA   | Inputs Open                              |

## AC ELECTRICAL CHARACTERISTICS

### CERPACK

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

| Symbol       | Parameter  | TA = 0°C                         |                       | TA = +25°C                       |                       | TA = +85°C                       |                       | Unit | Condition |
|--------------|--|----------------------------------|-----------------------|----------------------------------|-----------------------|----------------------------------|-----------------------|------|-----------|
|              |  | Min.                             | Max.                  | Min.                             | Max.                  | Min.                             | Max.                  |      |           |
| fshift       | Shift Frequency  | —                                | 700                   | —                                | 700                   | —                                | —                     | MHz  |           |
| tPLH<br>tPHL | Propagation Delay<br>CP to Qn, $\bar{Q}_n$   | 450                              | 1200                  | 450                              | 1200                  | 450                              | 1200                  | ps   |           |
| tPLH<br>tPHL | Propagation Delay<br>CP to $\bar{TC}$  | 600                              | 1900                  | 600                              | 1900                  | 600                              | 1900                  | ps   |           |
| tPLH<br>tPHL | Propagation Delay<br>MR to Qn, $\bar{Q}_n$   | 500                              | 1400                  | 500                              | 1400                  | 500                              | 1400                  | ps   |           |
| tPLH<br>tPHL | Propagation Delay<br>MR to $\bar{TC}$  | 600                              | 1900                  | 600                              | 1900                  | 600                              | 1900                  | ps   |           |
| tPLH<br>tPHL | Propagation Delay<br>D0/ $\bar{CET}$ to $\bar{TC}$                                   | 400                              | 1200                  | 400                              | 1200                  | 400                              | 1200                  | ps   |           |
| tPLH<br>tPHL | Propagation Delay<br>Sn to $\bar{TC}$  | 1500                             | 2600                  | 1500                             | 2600                  | 1500                             | 2600                  | ps   |           |
| tTLH<br>tTHL | Transition Time<br>20% to 80%, 80% to 20%  | 900                              | 300                   | 900                              | 300                   | 900                              | 300                   | ps   |           |
| ts           | Set-up Time<br>D3<br>Pn<br>D0/ $\bar{CET}$ to $\bar{CEP}$<br>Sn<br>MR (Release Time) | 800<br>800<br>700<br>2000<br>900 | —<br>—<br>—<br>—<br>— | 800<br>800<br>700<br>2000<br>900 | —<br>—<br>—<br>—<br>— | 800<br>800<br>700<br>2000<br>900 | —<br>—<br>—<br>—<br>— | ps   |           |
| th           | Hold Time<br>D3<br>Pn<br>D0/ $\bar{CET}$ to $\bar{CEP}$<br>Sn                        | 200<br>200<br>200<br>-600        | —<br>—<br>—<br>—      | 200<br>200<br>200<br>-600        | —<br>—<br>—<br>—      | 200<br>200<br>200<br>-600        | —<br>—<br>—<br>—      | ps   |           |
| tpw (H)      | Pulse Width HIGH, CP, MR   | —                                | 800                   | —                                | 800                   | —                                | 800                   | ps   |           |

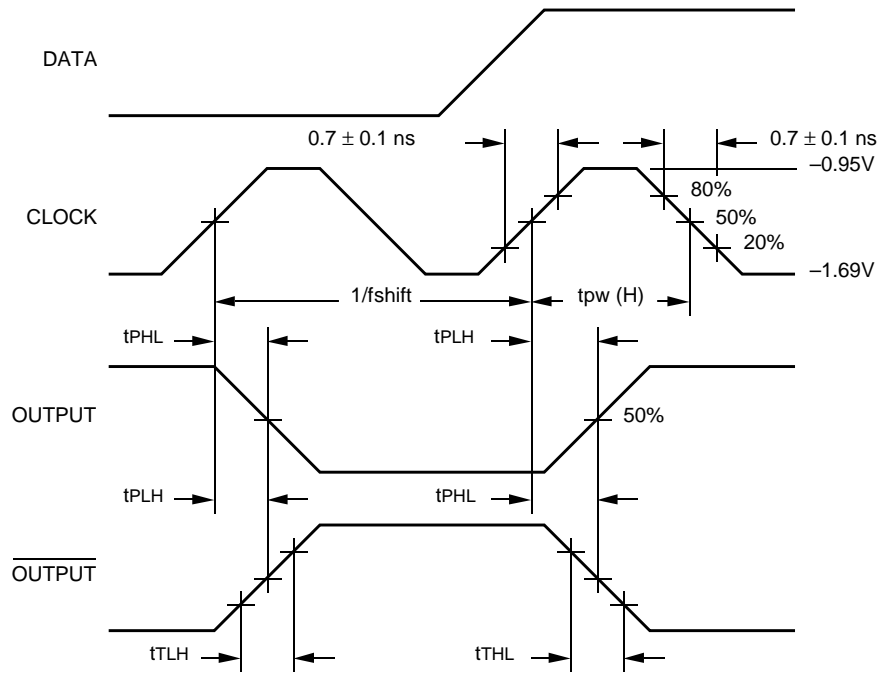
## AC ELECTRICAL CHARACTERISTICS

### PLCC

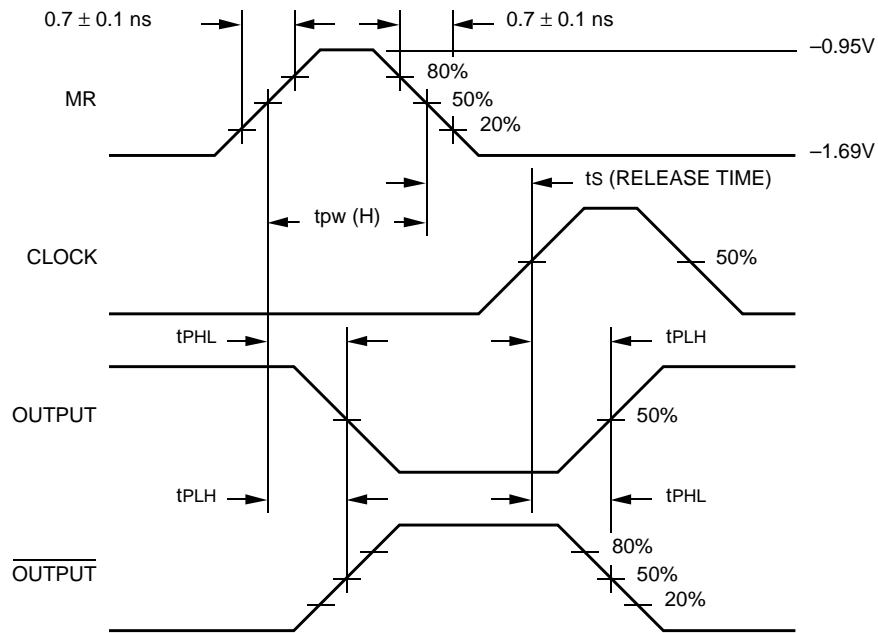
VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

| Symbol       | Parameter                                 | TA = 0°C |      | TA = +25°C |      | TA = +85°C |      | Unit | Condition |
|--------------|---|----------|------|------------|------|------------|------|------|-----------|
|              |   | Min.     | Max. | Min.       | Max. | Min.       | Max. |      |           |
| fshift       | Shift Frequency                           | —        | 700  | —          | 700  | —          | 700  | MHz  |           |
| tPLH<br>tPHL | Propagation Delay<br>CP to Qn, Qn         | 450      | 1100 | 450        | 1100 | 450        | 1100 | ps   |           |
| tPLH<br>tPHL | Propagation Delay<br>CP to TC             | 600      | 1800 | 600        | 1800 | 600        | 1800 | ps   |           |
| tPLH<br>tPHL | Propagation Delay<br>MR to Qn, Qn         | 500      | 1300 | 500        | 1300 | 500        | 1300 | ps   |           |
| tPLH<br>tPHL | Propagation Delay<br>MR to TC             | 600      | 1800 | 600        | 1800 | 600        | 1800 | ps   |           |
| tPLH<br>tPHL | Propagation Delay<br>Do/CET to TC         | 400      | 1100 | 400        | 1100 | 400        | 1100 | ps   |           |
| tPLH<br>tPHL | Propagation Delay<br>Sn to TC             | 1500     | 2500 | 1500       | 2500 | 1500       | 2500 | ps   |           |
| tTLH<br>tTHL | Transition Time<br>20% to 80%, 80% to 20% | 300      | 900  | 300        | 900  | 300        | 900  | ps   |           |
| ts           | Set-up Time                               |          |      |            |      |            |      | ps   |           |
|              | D3  | 800      | —    | 800        | —    | 800        | —    |      |           |
|              | Pn  | 800      | —    | 800        | —    | 800        | —    |      |           |
|              | Do/CET to CEP                             | 700      | —    | 700        | —    | 700        | —    |      |           |
|              | Sn  | 2000     | —    | 2000       | —    | 2000       | —    |      |           |
|              | MR (Release Time)                         | 900      | —    | 900        | —    | 900        | —    |      |           |
| th           | Hold Time                                 |          |      |            |      |            |      | ps   |           |
|              | D3  | 200      | —    | 200        | —    | 200        | —    |      |           |
|              | Pn  | 200      | —    | 200        | —    | 200        | —    |      |           |
|              | Do/CET to CEP                             | 200      | —    | 200        | —    | 200        | —    |      |           |
|              | Sn  | -600     | —    | -600       | —    | -600       | —    |      |           |
| tpw (H)      | Pulse Width HIGH, CP, MR                  | —        | 800  | —          | 800  | —          | 800  | ps   |           |

**TIMING DIAGRAMS**

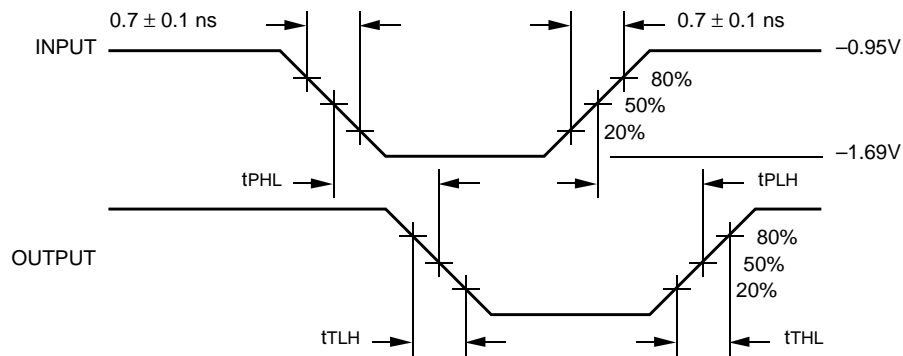


**Propagation Delay (Clock) and Transition Times**

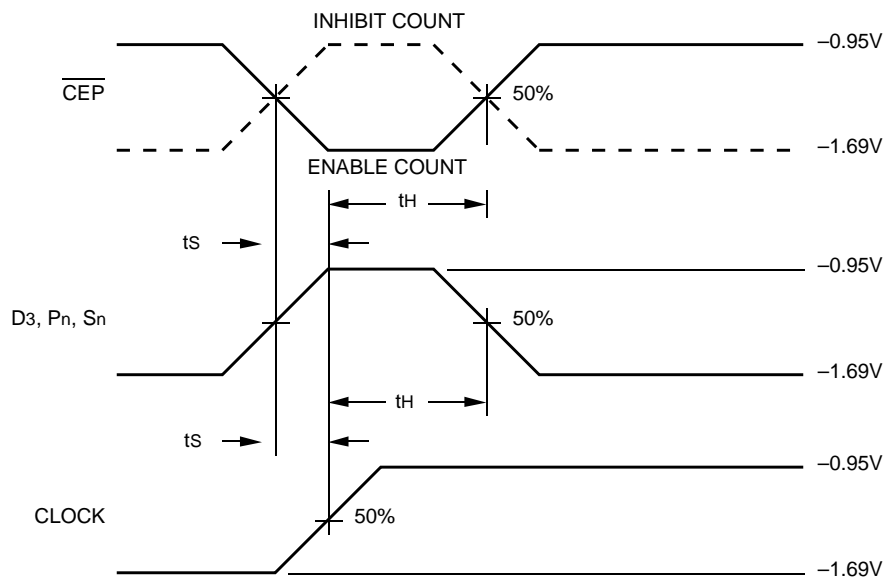


**Propagation Delay (Reset)**

**TIMING DIAGRAMS**



**Propagation Delay (Serial Data, Selects)**



**Set-up and Hold Time**

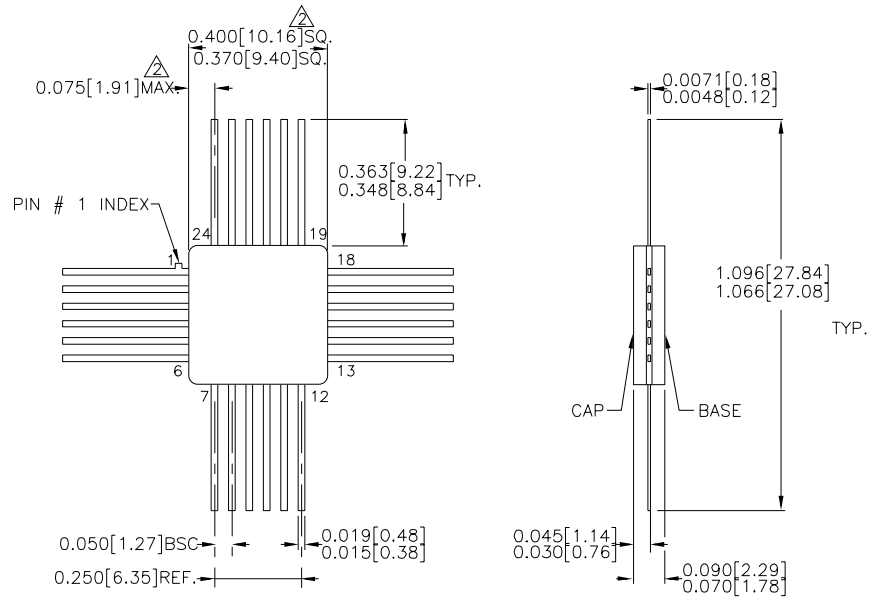
**NOTES:**

1.  $V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$ .
2.  $t_s$  is the minimum time before the transition of the clock that information must be present at the data input.
3.  $t_h$  is the minimum time after the transition of the clock that information must remain unchanged at the data input.

**PRODUCT ORDERING CODE**

| Ordering Code | Package Type | Operating Range |
|---------------|--------------|-----------------|
| SY100S336FC   | F24-1        | Commercial      |
| SY100S336JC   | J28-1        | Commercial      |
| SY100S336JCTR | J28-1        | Commercial      |

**24 LEAD CERPACK (F24-1)**

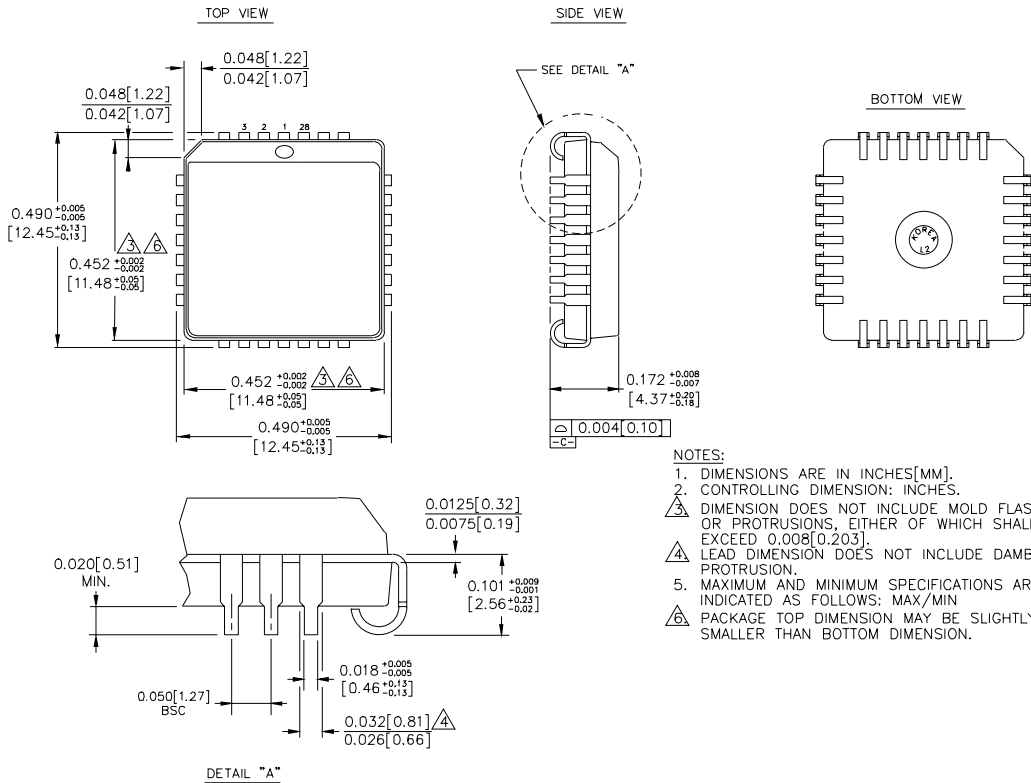


- NOTES:**
1. DIMENSIONS ARE IN INCHES[MM].
  2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
  3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03



**28 LEAD PLCC (J28-1)**



Rev. 03

**MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA**

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