PEREGRINE SEMICONDUCTOR

PRODUCT SPECIFICATION

# PE4246

## SPST High-Isolation, 50Ω Absorptive MOSFET RF Switch

### Features

- Non-reflective 50-ohm RF switch
- 50-ohm (0.25 watt) terminations
- High isolation: 55 dB at 1 GHz, 48 dB at 3 GHz, typical
- Low insertion loss: 0.8 dB at 1 GHz, 0.9 dB at 3 GHz
- High linearity: +33 dBm input 1dB compression point
- CMOS/TTL single-pin control
- Single +3-volt supply operation
- Extremely low bias: 33 µA @ 3V

## Product Description

*The PE4246 is a high-isolation MOSFET RF Switch designed to cover a broad range of applications from DC to 5.0 GHz, and is non-reflective at both RF1 and RF2 ports. This SPST switch integrates a single-pin CMOS control interface, and provides low insertion loss while operating with extremely low bias from a single +3-volt supply. In a typical application, the high isolation PE4246 can replace multiple RF switches of lesser isolation performance.*

*The PE4246 is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.*

**Figure 1. Functional Schematic Diagram**

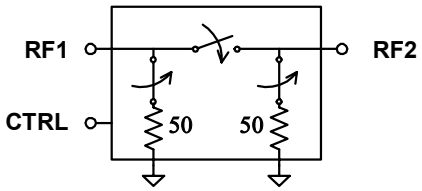



**Figure 2. Package Type**

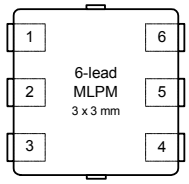
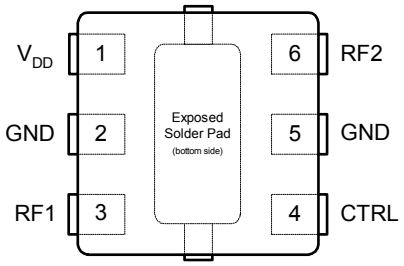



**Table 1. Electrical Specifications @ +25 °C** ($Z_S$ = $Z_L$ = 50 Ω)

| Parameter | Condition | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Operation Frequency[1] | | DC | | 5000 | MHz |
| Operating Power | CTRL=1/CTRL=0 | | | 30/24 | dBm |
| Insertion Loss | DC-2 GHz<br>2-3 GHz<br>3-4 GHz<br>4-5 GHz | | 0.8<br>0.9<br>1.0<br>1.3 | 1.0<br>1.1<br>1.3<br>1.8 | dB<br>dB<br>dB<br>dB |
| Isolation | DC-2 GHz<br>2-3 GHz<br>3-4 GHz<br>4-5 GHz | 49<br>45<br>43<br>40 | 55<br>48<br>46<br>44 | | dB<br>dB<br>dB<br>dB |
| Return Loss | DC-5 GHz | 11 | 20 | | dB |
| Input 1 dB Compression[3] | DC-5 GHz | 30 | 33 | | dBm |
| Input IP3 | DC-5 GHz | 50 | | | dBm |
| Video Feedthrough[2] | | | | 15 | $mV_{pp}$ |
| Switching Time | | | 2 | | µs |

Notes: 1. Device linearity will begin to degrade below 1 MHz.
2. The DC transient at the output of the switch when the control voltage is switched from Low to High or High to Low in a 50Ω test set-up, measured with 1ns risetime pulses and 500 MHz bandwidth.
3. Note Absolute Maximum ratings in Table 3.

## Figure 3. Pin Configuration (Top View)




## Table 2. Pin Descriptions

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | $V_{DD}$ | Nominal 3 V supply connection.[1] |
| 2 | GND | Ground connection. [3] |
| 3 | RF1 | RF port. [2] |
| 4 | CTRL | CMOS or TTL logic level:<br>High = RF1 to RF2 signal path<br>Low = RF1 isolated from RF2 |
| 5 | GND | Ground connection. [3] |
| 6 | RF2 | RF port. [2] |

Notes: 1. A bypass capacitor should be placed as close as possible to the pin.
2. Both RF pins must be DC blocked by an external capacitor or held at 0 $V_{DC}$.
3. The exposed pad must be soldered to the ground plane for proper switch performance.

## Table 3. Absolute Maximum Ratings

| Symbol | Parameter/Condition | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | -0.3 | 4.0 | V |
| $V_I$ | Voltage on CTRL input | -0.3 | 5.5 | V |
| $T_{ST}$ | Storage temperature | -65 | 150 | °C |
| $T_{OP}$ | Operating temperature | -40 | 85 | °C |
| $P_{IN}$ | Input power (50Ω), CTRL=1/CTRL=0 | | 33/24 | dBm |
| $V_{ESD}$ | ESD voltage (Human Body Model) | | 200 | V |

## Table 4. DC Electrical Specifications @ 25 °C

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ Power Supply | 2.7 | 3.0 | 3.3 | V |
| $I_{DD}$ Power Supply Current ($V_{DD}$ = 3V, $V_{CNTL}$ = 3V) | | 33 | 40 | µA |
| Control Voltage High | 0.7x$V_{DD}$ | | 5 | V |
| Control Voltage Low | 0 | | 0.3x$V_{DD}$ | V |

## Device Description

The PE4246 high-isolation SPST RF Switch is designed to support a variety of applications where high isolation performance is demanded and a non-reflective input and output is desired. This switch is able to replace multiple lesser performing switches in a very small 3x3 MLPM footprint.

## Table 5. Truth Table

| Control Voltage | Signal Path |
|---|---|
| CTRL = CMOS or TTL High | RF1 to RF2 |
| CTRL = CMOS or TTL Low | RF1 isolated from RF2 |

## Control Logic

The control logic input pin (CTRL) is typically driven by a 3-volt CMOS logic level signal, and has a threshold of 50% of $V_{DD}$. For flexibility to support systems that have 5-volt control logic drivers, the control logic input has been designed to handle a 5-volt logic HIGH signal. (A minimal current will be sourced out of the $V_{DD}$ pin when the control logic input voltage level exceeds $V_{DD}$.)

## Electrostatic Discharge (ESD) Precautions

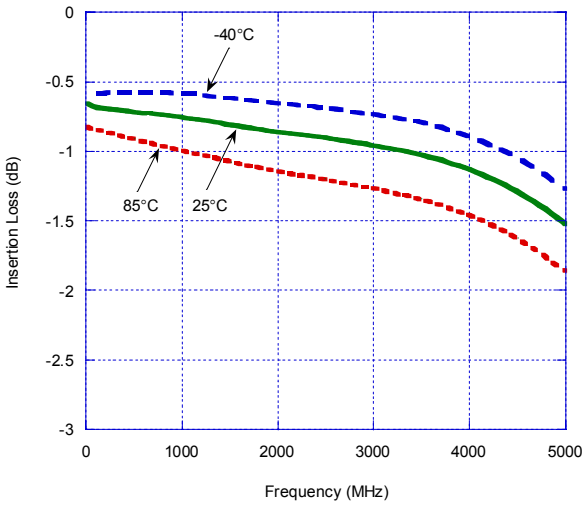
When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

## Latch-Up Avoidance

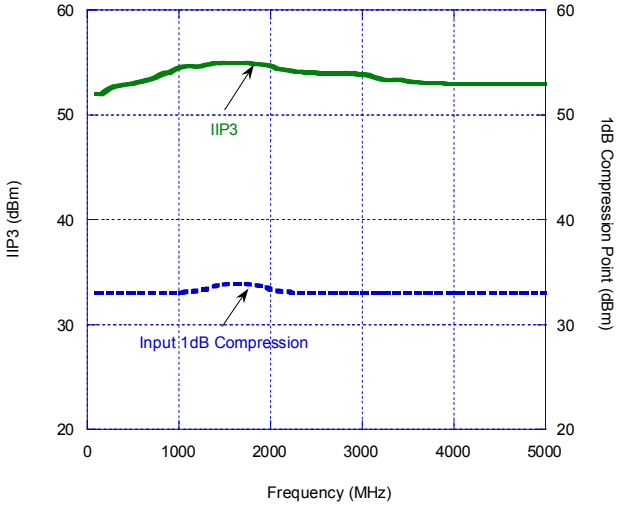
Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

## Typical Performance Data @ -40 °C to 85 °C (Unless Otherwise Noted)

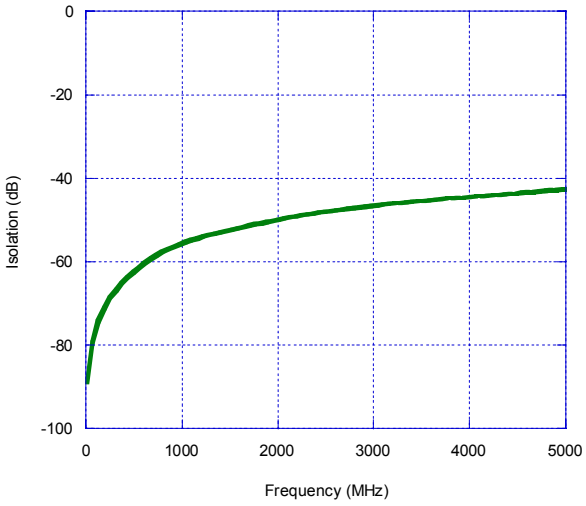
### Figure 4. Insertion Loss




### Figure 5. Input 1 dB Compression Point & IIP3

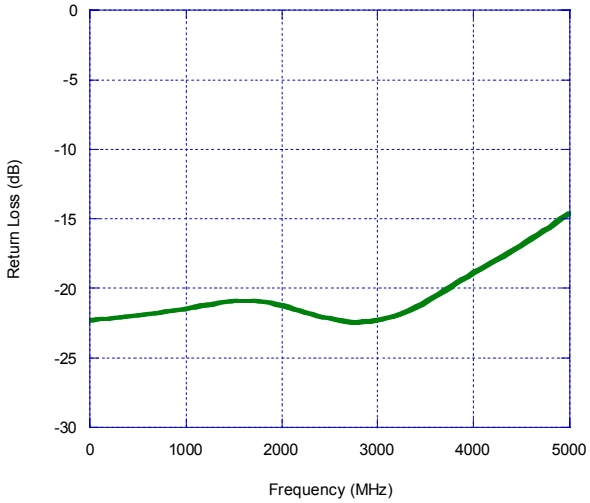



### Figure 6. Isolation

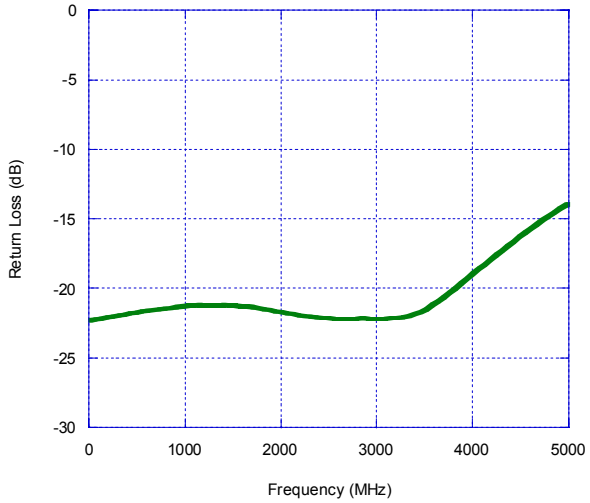


## Typical Performance Data @ +25 °C

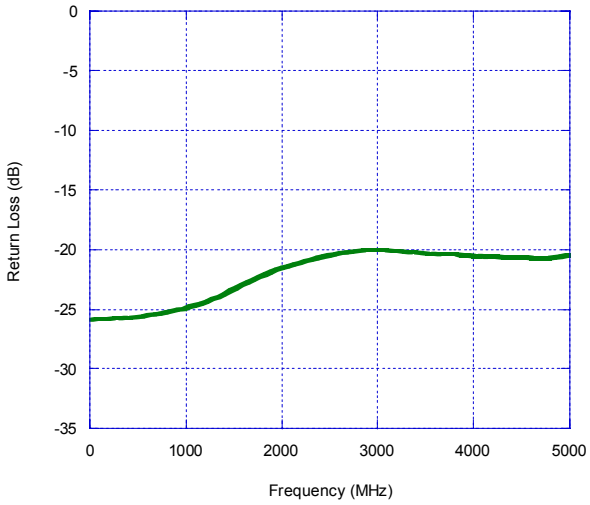
### Figure 7. RF1 Return Loss (CTRL = High)



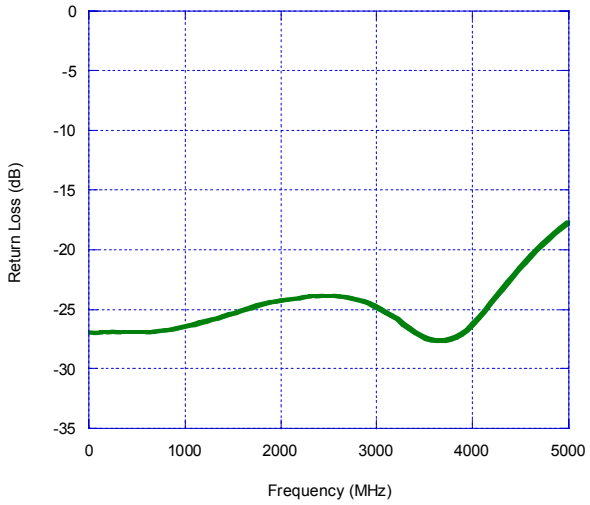

### Figure 8. RF2 Return Loss (CTRL = High)




### Figure 9. RF1 Return Loss (CTRL = Low)




### Figure 10. RF2 Return Loss (CTRL = Low)



## Evaluation Kit Information

### Evaluation Kit

The SPST Switch Evaluation Kit board was designed to ease customer evaluation of the PE4246 SPDT switch. The RF1 port is connected through a 50Ω transmission line to the top left SMA connector, J1. The RF2 port is connected through a 50Ω transmission line to the top right SMA connector, J2. A through transmission line connects SMA connectors J3 and J4. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide model with trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and εR of 4.3. Note that the predominate mode for these transmission lines is coplanar waveguide with a ground plane.

J5 and J6 provide a means for controlling DC and digital inputs to the device. J6-1 is connected to the device $V_{DD}$ input. J5-1 is connected to the device CNTL input. J5-2 and J6-2 are GND connections. A decoupling capacitor (100 pF) is provided on both CNTL and $V_{DD}$ traces. It is the responsibility of the customer to determine proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

**Figure 11. Evaluation Board Layouts**

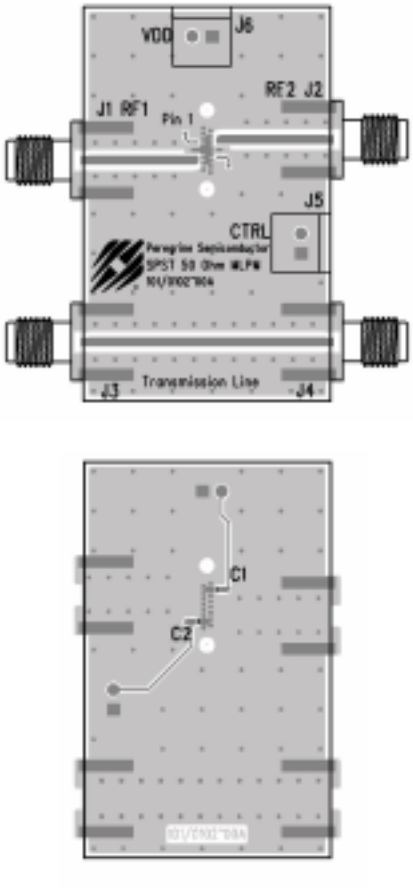
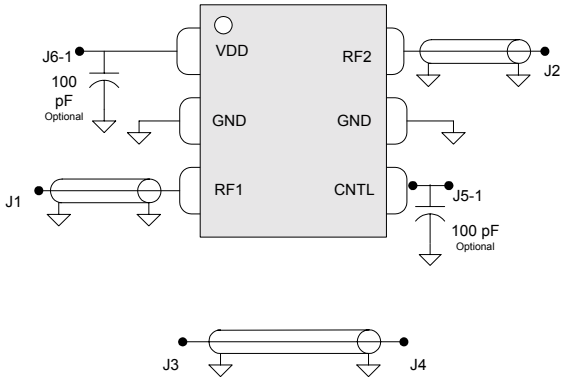
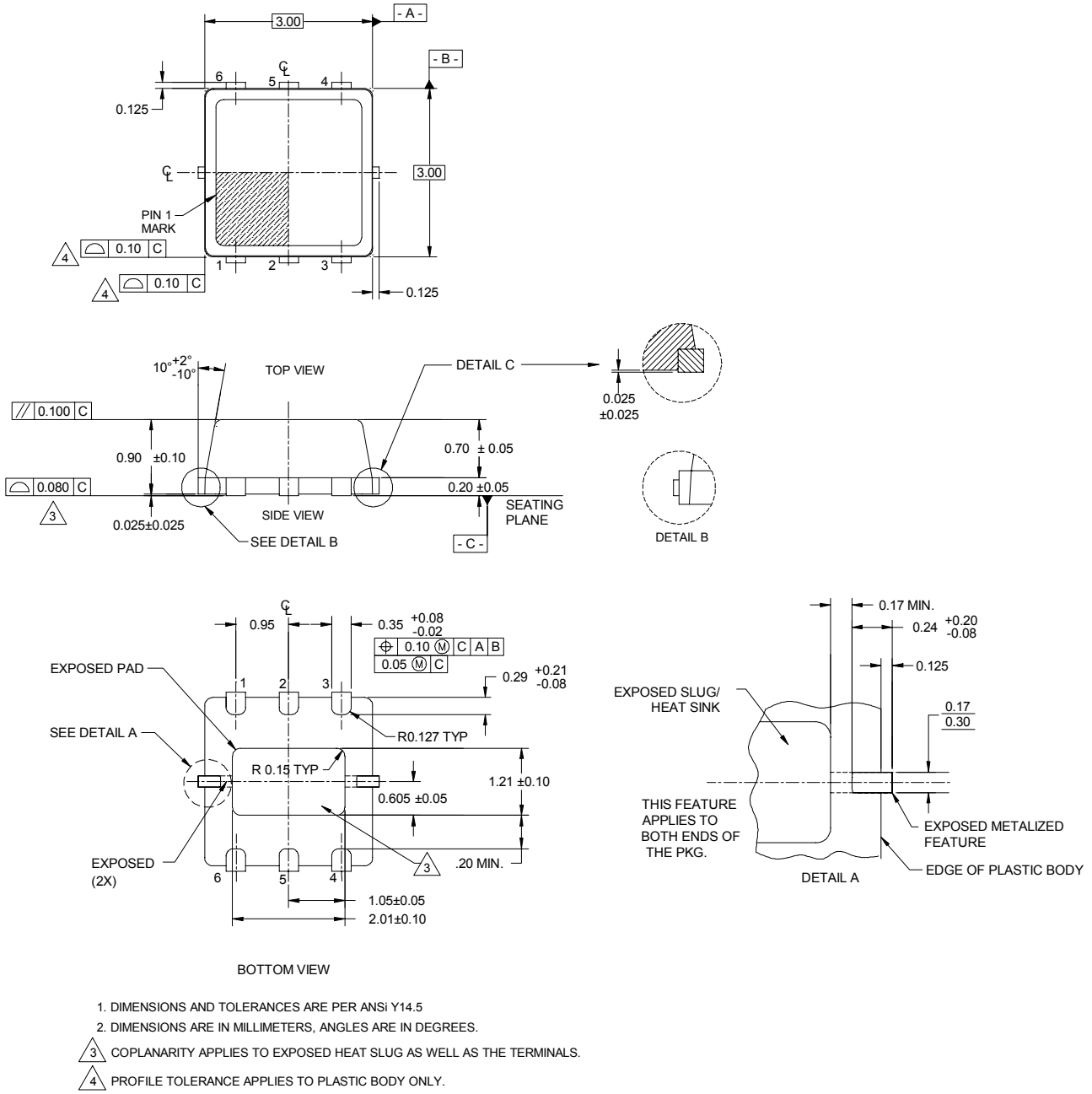



**Figure 12. Evaluation Board Schematic**



## Figure 13. Package Drawing

6-lead MLPM




1. DIMENSIONS AND TOLERANCES ARE PER ANSi Y14.5
2. DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
3. COPLANARITY APPLIES TO EXPOSED HEAT SLUG AS WELL AS THE TERMINALS.
4. PROFILE TOLERANCE APPLIES TO PLASTIC BODY ONLY.

## Table 6. Ordering Information

| Order Code | Part Marking | Description | Package | Shipping Method |
|---|---|---|---|---|
| 4246-01 | 4246 | PE4246-06MLP3x3-12800F | 6-lead 3x3mm MLPM | 12800 units / Canister |
| 4246-02 | 4246 | PE4246-06MLP3x3-3000C | 6-lead 3x3mm MLPM | 3000 units / T&R |
| 4246-00 | PE4246-EK | PE4246-06MLP3x3-EK | Evaluation Board | 1 / Box |

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The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

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