



FET INPUT HIGH SPEED VOLTAGE FOLLOWER/BUFFER AMPLIFIER

0033

M.S.KENNEDY CORP.

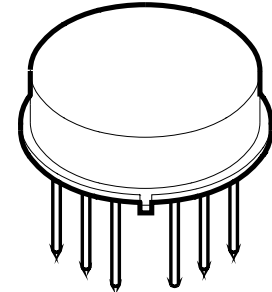
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FEATURES:

- Industry Wide LH0033/EL2005 Replacement
- Low Input Offset - 2mV
- Low Input Offset Drift - 25 μ V/ $^{\circ}$ C
- FET Input, Low Input Current - 50pA
- High Slew Rate - 1500V/ μ S
- Wide Bandwidth - 140MHz
- High Output Current - \pm 100mA
- Available to DSCC SMD 5962-80014

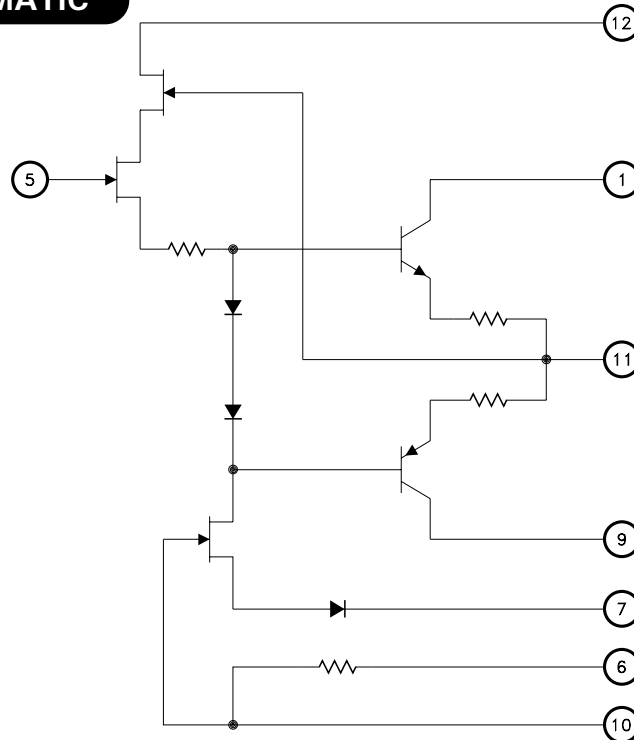
MIL-PRF-38534 CERTIFIED



DESCRIPTION:

The MSK 0033(B) is a high speed, wide bandwidth voltage follower/buffer amplifier that is pin compatible with all other 0033 designs. The FET input is cascaded to force the input characteristics to remain constant over the full input voltage range. Significantly improved performance in sample and hold circuits is achieved since the DC bias current remains constant with input voltage. The FET input also makes the MSK 0033 very accurate since it produces extremely low input bias current, input offset voltage and input offset voltage drift specifications. Transition times in the range of 2.5 nS make the MSK 0033 fast enough for most high speed voltage follower/buffer amplifier applications.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- Sample And Hold
- Impedance Buffers For A to D's
- High Speed Line Drivers
- CRT Deflection Driver

PIN-OUT INFORMATION

- | | |
|-------------------------|--------------------------------|
| 1 Positive Driver Power | 7 Offset Adjust |
| 2 Supply | 8 N/C |
| 3 N/C | 9 Negative Driver Power Supply |
| 4 N/C | 10 Negative Power Supply |
| 5 N/C | 11 Output |
| 6 Input | 12 Positive Power Supply |
| Offset Preset | |

ABSOLUTE MAXIMUM RATINGS

| | | | | | |
|--------------|---|-----------------------------------|----------|--------------------------------|--|
| $\pm V_{CC}$ | Supply Voltage | $\pm 20V$ | T_{ST} | Storage Temperature Range | $-65^{\circ}C$ to $+150^{\circ}C$ |
| I_{OUT} | Output Current | $\pm 120mA$ | T_{LD} | Lead Temperature Range | $300^{\circ}C$ (10 Seconds) |
| V_{IN} | Differential Input Voltage | $\pm 20V$ | T_J | Junction Temperature | $175^{\circ}C$ |
| T_C | Case Operating Temperature (MSK 0033B) | $-55^{\circ}C$ to $+125^{\circ}C$ | R_{TH} | Thermal Resistance | $65^{\circ}C/W$ Junction to Case Output Devices Only |
| | (MSK 0033) | $-40^{\circ}C$ to $+85^{\circ}C$ | | | |

ELECTRICAL SPECIFICATIONS

| Parameter | Test Conditions | Group A Subgroup | MSK 0033B | | | MSK 0033 | | | Units |
|---------------------------------|--|---------------------|----------------|------------|-----------|----------------|------------|-----------|-------------------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| STATIC | | | | | | | | | |
| Supply Voltage Range ③ ⑧ | | - | ± 10 | ± 15 | ± 18 | ± 10 | ± 15 | ± 18 | V |
| Quiescent Current | $V_{IN} = 0V$ | 1 | - | ± 19 | ± 22 | - | ± 19 | ± 25 | mA |
| INPUT | | | | | | | | | |
| Offset Voltage | Short Pin 6 to Pin 7 $V_{IN} = 0V$ | 1 | - | ± 2.0 | ± 10 | - | ± 5 | ± 15 | mV |
| Offset Voltage Drift | Short Pin 6 to Pin 7 $V_{IN} = 0V$ | 2,3 | - | ± 25 | ± 250 | - | - | - | $\mu V/^{\circ}C$ |
| Offset Adjust | Pin 6 = open $R_{POT} = 200\Omega$ From Pin 7 to Pin 9 | 1,2,3 | Adjust to Zero | | | Adjust to Zero | | | mV |
| Input Bias Current ⑨ | $V_{CM} = 0V$ Either Input | 1 | - | ± 50 | ± 100 | - | ± 50 | ± 500 | pA |
| | | 2,3 | - | ± 2 | ± 10 | - | ± 2 | - | nA |
| Input Impedance ③ | $F = DC$ | - | - | 10^{12} | - | - | 10^{12} | - | Ω |
| Power Supply Rejection Ratio ② | $\pm 10V \leq V_S \leq \pm 20V$ | - | 65 | 75 | - | 60 | 75 | - | dB |
| Input Noise Density ③ | $F = 10Hz$ to $1KHz$ | - | - | 1.5 | - | - | 1.5 | - | μV_{RMS} |
| Input Noise Voltage ③ | $F = 1KHz$ | - | - | 40 | - | - | 40 | - | nV/\sqrt{Hz} |
| OUTPUT | | | | | | | | | |
| Output Voltage Swing | $V_{IN} = \pm 14V$ $R_L = 1K\Omega$ | 4 | ± 12 | ± 12.5 | - | ± 12 | ± 12.5 | - | V |
| Output Current | $V_{IN} = \pm 10.5V$ $R_L = 100\Omega$ | 4 | ± 90 | ± 110 | - | ± 90 | ± 110 | - | mA |
| Settling Time to 1% ② ③ | 2V step | - | - | 25 | - | - | 25 | - | nS |
| Bandwidth (-3dB) ③ | $V_{IN} = 1V_{RMS}$ $R_L = 1K\Omega$ | - | - | 140 | - | - | 140 | - | MHz |
| TRANSFER CHARACTERISTICS | | | | | | | | | |
| Slew Rate | $V_{OUT} = \pm 10V$ | 4 | 1000 | 1500 | - | 1000 | 1500 | - | $V/\mu S$ |
| Voltage Gain | $R_S = 100\Omega$ $V_{IN} = 1V_{RMS}$ $F = 1KHz$ | 4 | 0.97 | 0.99 | - | 0.95 | 0.98 | - | V/V |

NOTES:

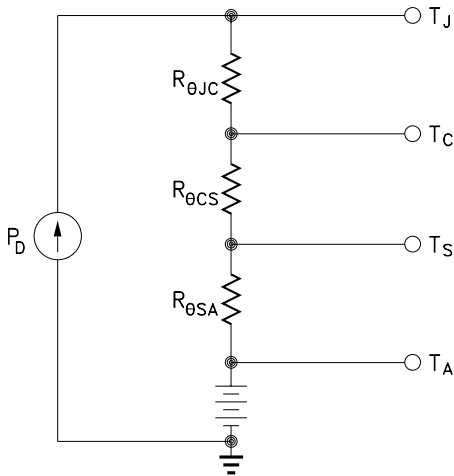
- ① Unless otherwise specified $\pm V_{CC} = \pm 15VDC$.
- ② Measured within a high speed amplifier feedback loop.
- ③ Devices shall be capable of meeting the parameter, but need not be tested. Typical parameters are for reference only.
- ④ Industrial grade devices shall be tested to subgroups 1 and 4 unless otherwise specified.
- ⑤ Military grade devices ('B' suffix) shall be 100% tested to subgroups 1,2,3 and 4.
- ⑥ Subgroup 5 and 6 testing available upon request.
- ⑦ Subgroup 1,4 $T_A = T_C = +25^{\circ}C$
Subgroup 2,5 $T_A = T_C = +125^{\circ}C$
Subgroup 3,6 $T_A = T_C = -55^{\circ}C$
- ⑧ Electrical specifications are derated for power supply voltages other than $\pm 15VDC$.
- ⑨ Measurement made 0.5 seconds after application of power. Actual DC continuous test limit is 2.5 nA at $25^{\circ}C$

APPLICATION NOTES

HEAT SINKING

To determine if a heat sink is necessary for your application and if so, what type, refer to the thermal model and governing equation below.

Thermal Model:



Governing Equation:

$$T_J = P_D \times (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A$$

Where

- T_J = Junction Temperature
- P_D = Total Power Dissipation
- $R_{\theta JC}$ = Junction to Case Thermal Resistance
- $R_{\theta CS}$ = Case to Heat Sink Thermal Resistance
- $R_{\theta SA}$ = Heat Sink to Ambient Thermal Resistance
- T_C = Case Temperature
- T_A = Ambient Temperature
- T_S = Sink Temperature

Example:

This example demonstrates a worst case analysis for the buffer output stage. This occurs when the output voltage is 1/2 the power supply voltage. Under this condition, maximum power transfer occurs and the output is under maximum stress.

Conditions:

- $V_{CC} = \pm 16VDC$
- $V_O = \pm 8Vp$ Sine Wave, Freq. = 1KHz
- $R_L = 100\Omega$

For a worst case analysis we will treat the $\pm 8Vp$ sine wave as an 8 VDC output voltage.

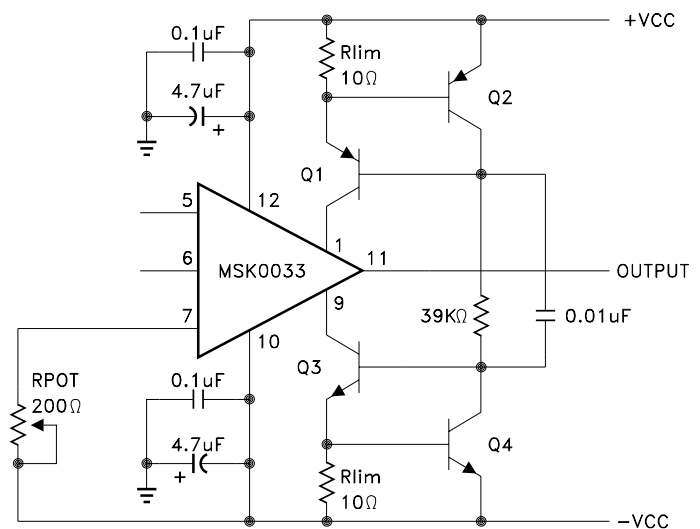
- 1.) Find Driver Power Dissipation
 - $P_D = (V_{CC} - V_O) (V_O / R_L)$
 - $= (16V - 8V) (8V / 100\Omega)$
 - $= 640mW$
- 2.) For conservative design, set $T_J = +125^\circ C$ Max.
- 3.) For this example, worst case $T_A = +80^\circ C$
- 4.) $R_{\theta JC} = 65^\circ C/W$ from MSK 0033B Data Sheet
- 5.) $R_{\theta CS} = 0.15^\circ C/W$ for most thermal greases
- 6.) Rearrange governing equation to solve for $R_{\theta SA}$

$$\begin{aligned} R_{\theta SA} &= ((T_J - T_A) / P_D) - (R_{\theta JC}) - (R_{\theta CS}) \\ &= ((125^\circ C - 80^\circ C) / .64W) - 65^\circ C/W - .15^\circ C/W \\ &= 70.3 - 65.15 \\ &= 5.2^\circ C/W \end{aligned}$$

The heat sink in this example must have a thermal resistance of no more than $5.2^\circ C/W$ to maintain a junction temperature of no more than $+125^\circ C$.

OFFSET VOLTAGE ADJUST

See Figure 1. To externally null the offset voltage, connect a 200Ω potentiometer between Pins 7 and 10 and leave Pin 6 open. If offset null is not necessary, short Pin 6 to Pin 7 and remove the 200Ω potentiometer. Do not connect Pin 7 to $-V_{CC}$.



Q1,Q2 = 2N2907
Q3,Q4 = 2N2222

FIGURE 1

CURRENT LIMITING

See Figure 1. If no current limit is required, short Pin 1 to Pin 12 and Pin 9 to Pin 10 and delete Q1 thru Q4 connections. Q1 through Q4 and the R_{lim} resistors form a current source current limit scheme and current limit resistor values can be calculated as follows:

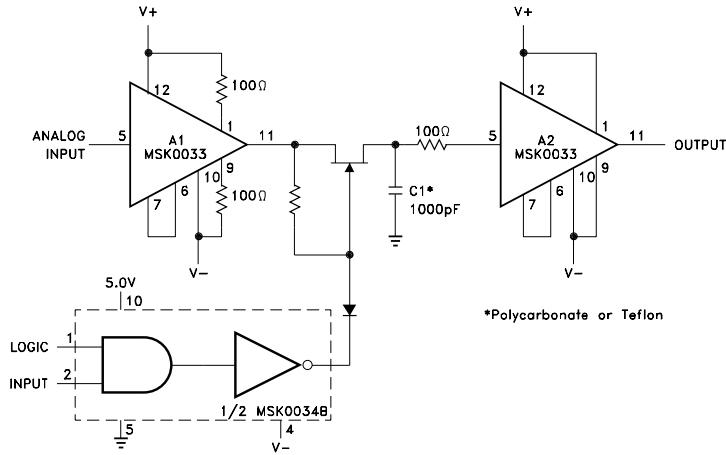
$$+R_{lim} \cong \frac{V_{be}}{I_{sc}} \quad -R_{lim} \cong \frac{V_{be}}{I_{sc}}$$

Since current limit is directly proportional to the base-emitter voltage drop of the 2N2222's and 2N2907's in the current limit scheme, the current limit value will change slightly with ambient temperature changes. The base-emitter voltage drop will decrease as temperature increases causing the actual current limit point to decrease.

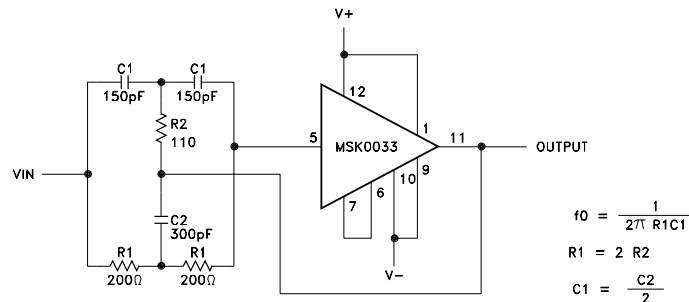
POWER SUPPLY BYPASSING

Both the negative and the positive power supplies must be effectively decoupled with a high and low frequency bypass circuit to avoid power supply induced oscillation. An effective decoupling scheme consists of a 0.1 microfarad ceramic capacitor in parallel with a 4.7 microfarad tantalum capacitor from each power supply pin to ground.

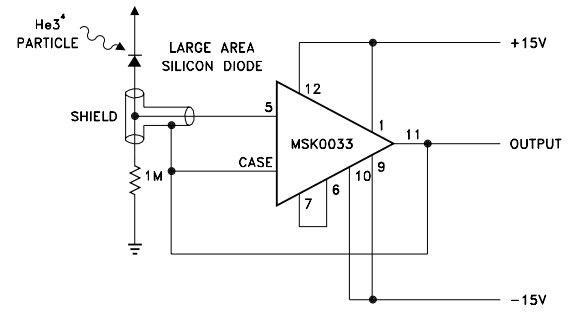
TYPICAL APPLICATIONS



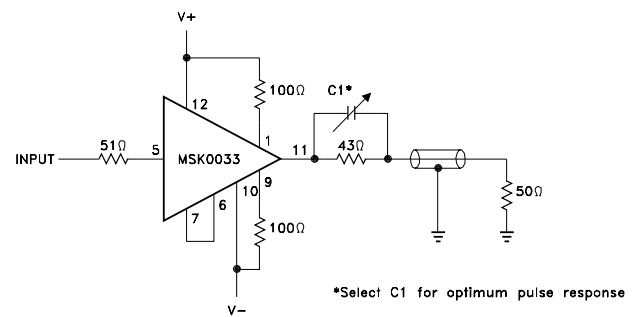
HIGH SPEED SAMPLE AND HOLD



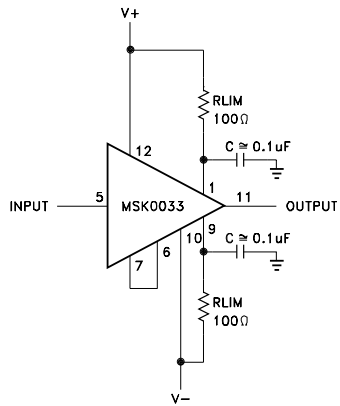
4.5MHz NOTCH FILTER



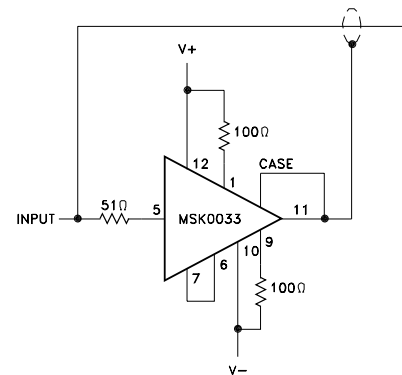
NUCLEAR PARTICLE DETECTOR



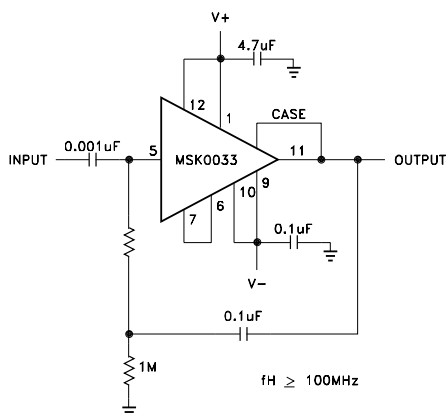
COAXIAL CABLE DRIVER



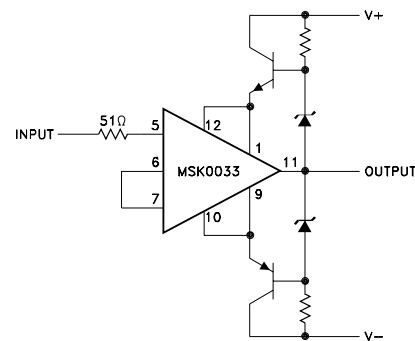
MSK0033 USING RESISTOR CURRENT LIMITING



INSTRUMENTATION SHIELD/LINE DRIVER

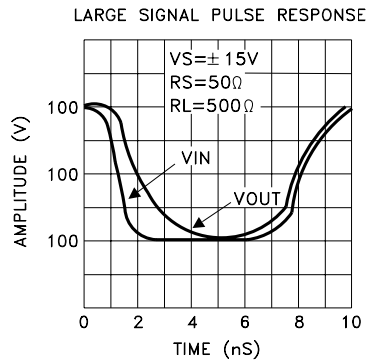
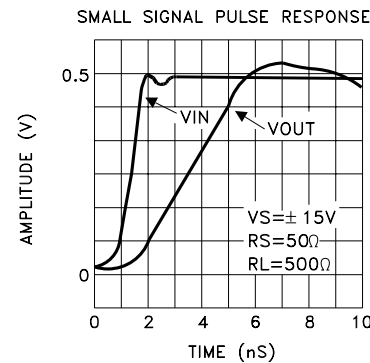
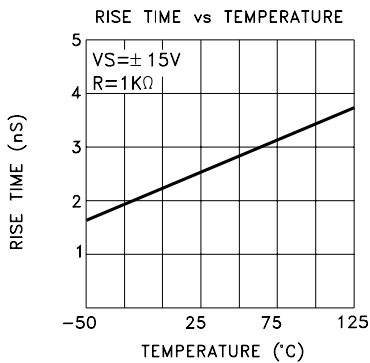
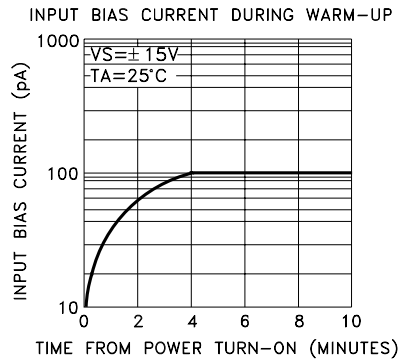
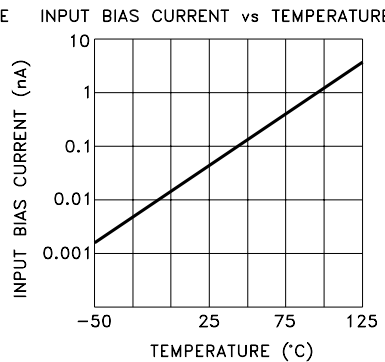
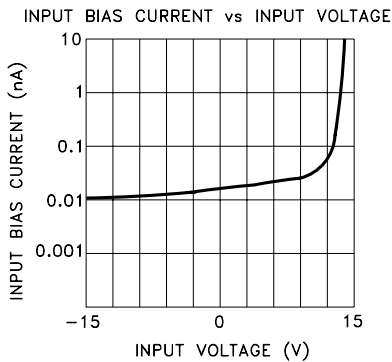
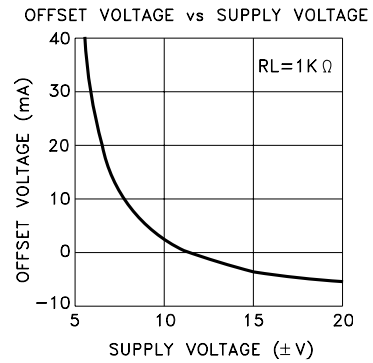
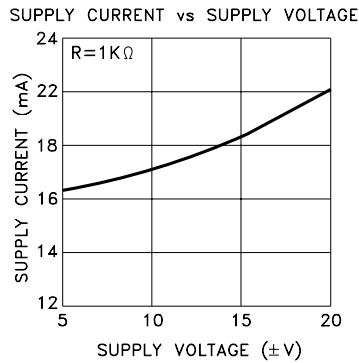
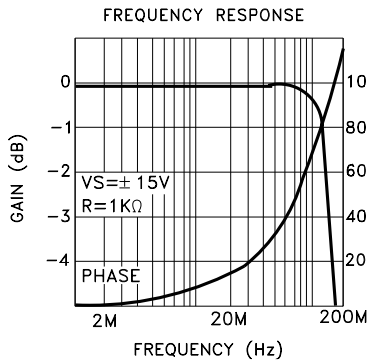
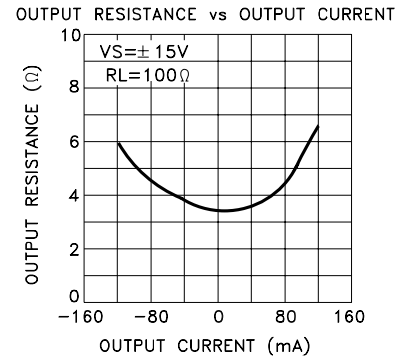
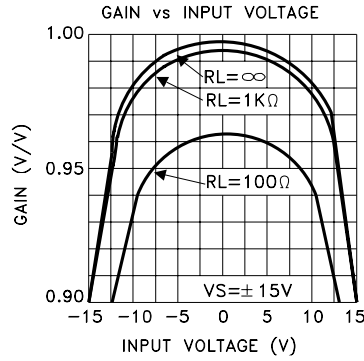
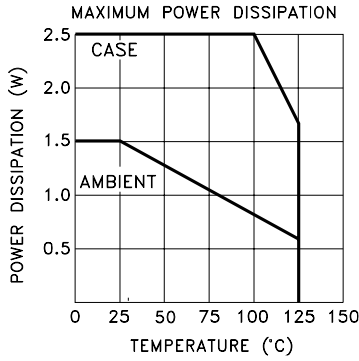


HIGH INPUT IMPEDANCE AC COUPLED AMPLIFIER

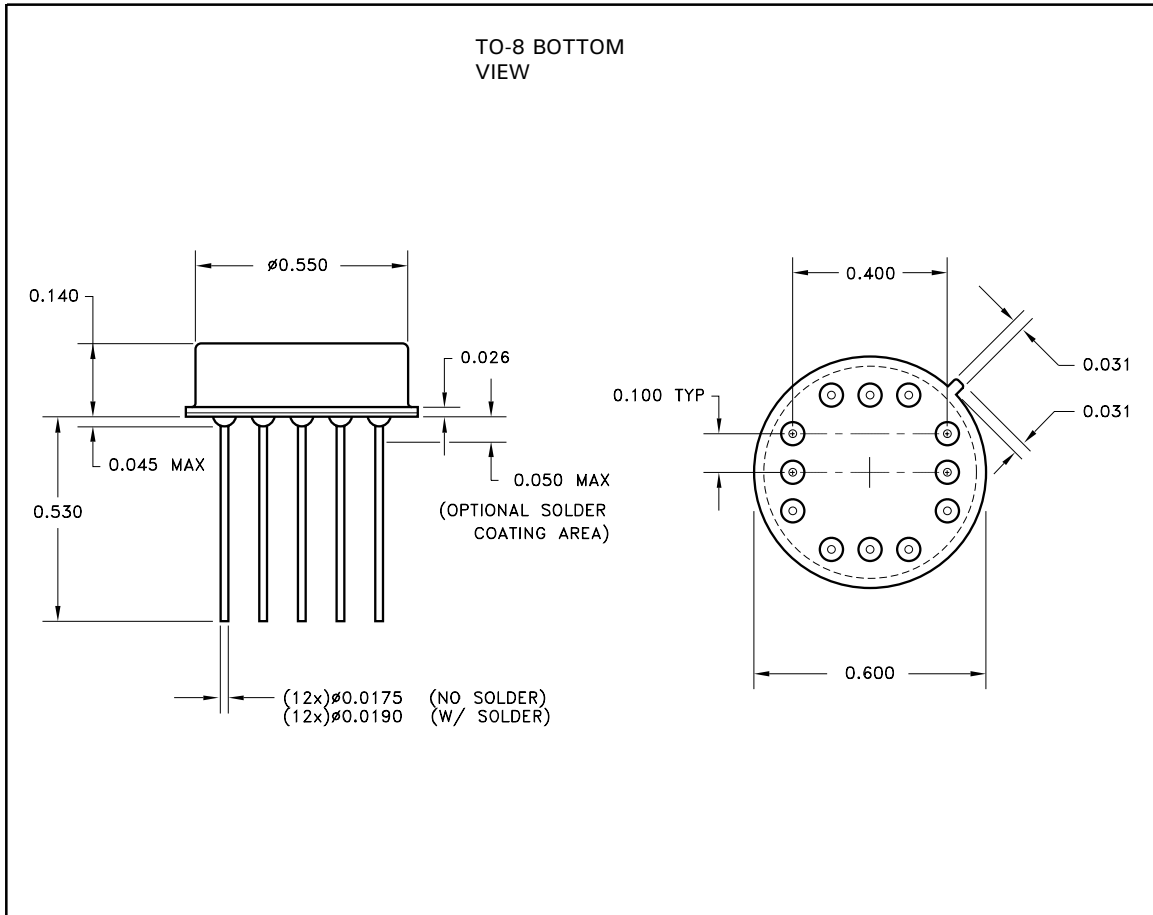


BOOTSTRAPPED SUPPLIES FOR HIGH VOLTAGE APPLICATIONS

TYPICAL PERFORMANCE CURVES



MECHANICAL SPECIFICATIONS



ALL DIMENSIONS ARE ± 0.010 INCHES UNLESS OTHERWISE LABELED

ORDERING INFORMATION

| Part Number | Screening Level |
|-------------|------------------------|
| MSK0033 | Industrial |
| MSK0033B | Military-Mil-PRF-38534 |
| 8001401ZX | DSCC - SMD |

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