

# Thyristors

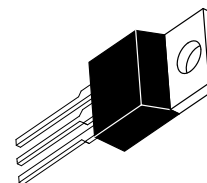
## Silicon-Controlled Rectifiers

... designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass-Passivated Junctions
- Blocking Voltage to 800 Volts
- TO-220 Construction — Low Thermal Resistance, High Heat Dissipation and Durability

### MCR218 Series

SCRs  
8 AMPERES RMS  
50 thru 800 VOLTS



CASE 221A-04  
(TO-220AB)  
STYLE 3

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Voltage <sup>(1)</sup> (T <sub>J</sub> = 25 to 125°C, Gate Open)	V <sub>DRM</sub> V <sub>RRM</sub>	50 100 200 400 600 800	Volts
Forward Current RMS (All Conduction Angles)	I <sub>T(RMS)</sub>	8	Amps
Peak Forward Surge Current (1/2 Cycle, Sine Wave, 60 Hz)	I <sub>TSM</sub>	80	Amps
Circuit Fusing Considerations (t = 8.3 ms)	I <sup>2</sup> t	26	A <sup>2</sup> s
Forward Peak Gate Power	P <sub>GM</sub>	5	Watts
Forward Average Gate Power	P <sub>G(AV)</sub>	0.5	Watt
Forward Peak Gate Current	I <sub>GM</sub>	2	Amps
Operating Junction Temperature Range	T <sub>J</sub>	-40 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-40 to +150	°C

1. V<sub>DRM</sub> and V<sub>RRM</sub> for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

# MCR218 Series

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	$^{\circ}C/W$

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}C$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current ( $V_{AK} = \text{Rated } V_{DRM} \text{ or } V_{RRM}$ , Gate Open) $T_J = 25^{\circ}C$ $T_J = 125^{\circ}C$	$I_{DRM}, I_{RRM}$	— —	— —	10 2	$\mu A$ mA
Peak On-State Voltage <sup>(1)</sup> ( $I_{TM} = 16 \text{ A Peak}$ )	$V_{TM}$	—	1.5	1.8	Volts
Gate Trigger Current (Continuous dc) ( $V_D = 12 \text{ V}, R_L = 100 \text{ Ohms}$ )	$I_{GT}$	—	10	25	mA
Gate Trigger Voltage (Continuous dc) ( $V_D = 12 \text{ V}, R_L = 100 \text{ Ohms}$ ) (Rated $V_{DRM}$ , $R_L = 1000 \text{ Ohms}, T_J = 125^{\circ}C$ )	$V_{GT}$	— 0.2	— —	1.5 —	Volts
Holding Current (Anode Voltage = 24 Vdc, Peak Initiating On-State Current = 0.5 A, 0.1 to 10 ms Pulse, Gate Trigger Source = 7 V, 20 Ohms)	$I_H$	—	16	30	mA
Critical Rate-of-Rise of Off-State Voltage ( $V_D = \text{Rated } V_{DRM}$ , Exponential Waveform, Gate Open, $T_J = 125^{\circ}C$ )	dv/dt	—	100	—	V/ $\mu s$

1. Pulse Test: Pulse Width = 1 ms, Duty Cycle  $\leq 2\%$ .

FIGURE 1 — CURRENT DERATING

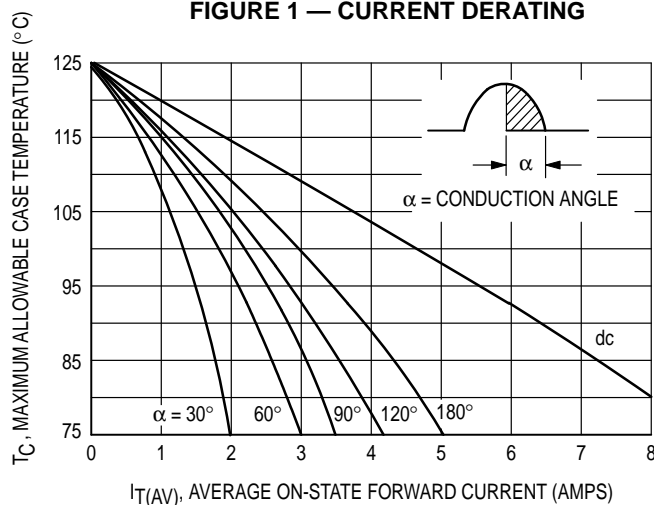


FIGURE 2 — ON-STATE POWER DISSIPATION

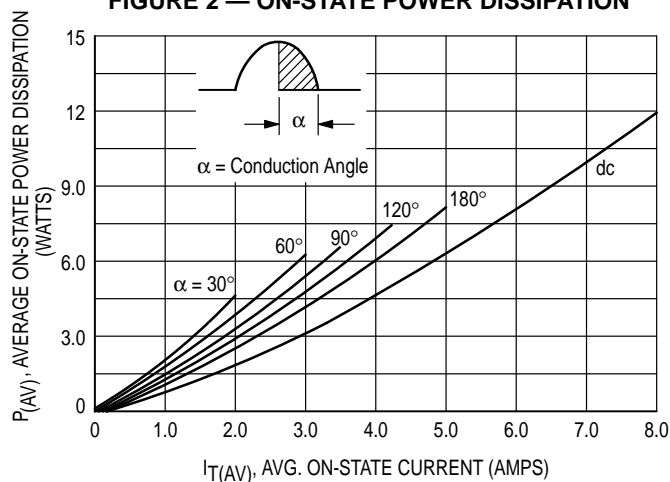


FIGURE 3 — NORMALIZED GATE TRIGGER CURRENT

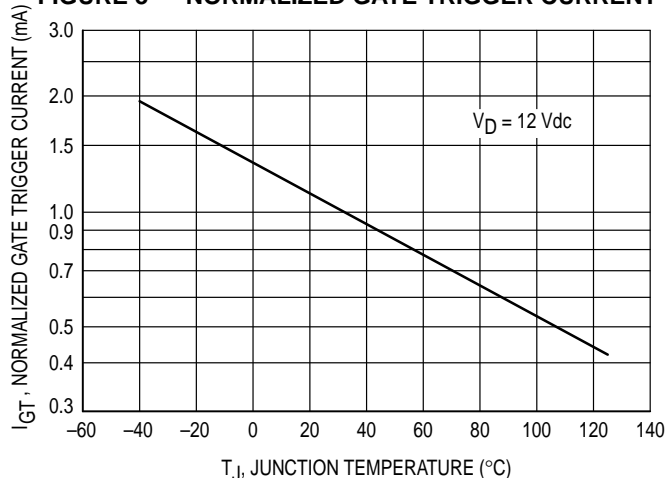


FIGURE 4 — NORMALIZED GATE TRIGGER VOLTAGE

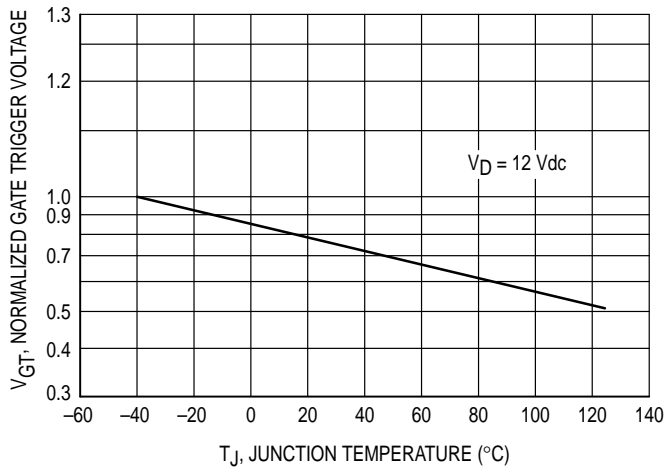
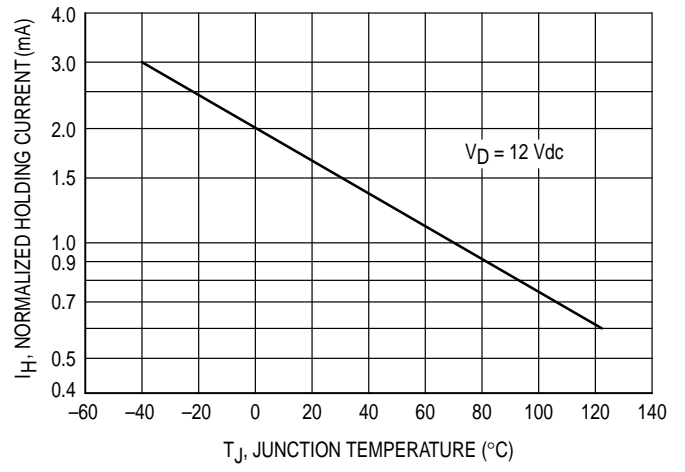
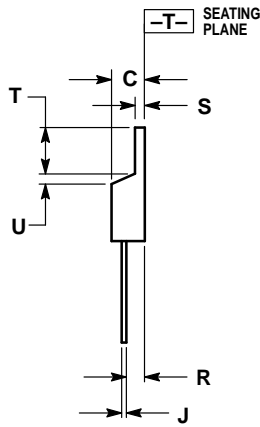
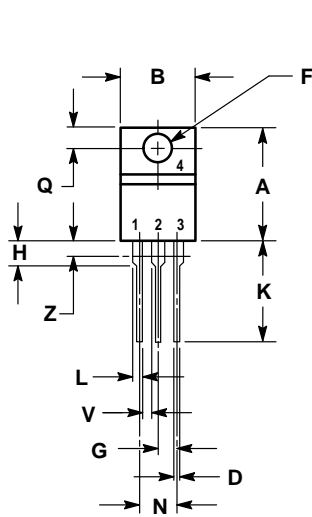


FIGURE 5 — NORMALIZED HOLDING CURRENT



**PACKAGE DIMENSIONS**




STYLE 3:  
 PIN 1. CATHODE  
 2. ANODE  
 3. GATE  
 4. ANODE

- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.  
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.022	0.36	0.55
K	0.500	0.562	12.70	14.27
L	0.045	0.055	1.15	1.39
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

**CASE 221A-04  
 (TO-220AB)**

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