1 PRODUCT OVERVIEW

SAM88RCRI PRODUCT FAMILY

Samsung's SAM88RCRI family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes.

A dual address/data bus architecture and a large number of bit- or nibble-configurable I/O ports provide a flexible programming environment for applications with varied memory and I/O requirements. Timer/counters with selectable operating modes are included to support real-time operations. Many SAM88RCRI microcontrollers have an external interface that provides access to external memory and other peripheral devices.

KS86C6308/P6308 MICROCONTROLLER

The KS86C6308/P6308 single-chip 8-bit microcontroller is fabricated using an advanced CMOS process. It is built around the powerful SAM88RCRI CPU core.

Stop and Idle power-down modes were implemented to reduce power consumption. To increase on-chip register space, the size of the internal register file was logically expanded. The KS86C6308 has 8 K bytes of program memory on-chip.

Using the SAM88RCRI design approach, the following peripherals were integrated with the SAM88RCRI core:

— Five configurable I/O ports (32 pins)
— 20 bit-programmable pins for external interrupts
— 8-bit timer/counter and 16-bit timwe/counter with three operating modes
— Full speed low speed USB function

The KS86C6308/P6308 is a versatile microcontroller that can be used in a wide range of full/low speed USB support general purpose applications. It is especially suitable for use as a keyboard with hub controller and is available in a 64-pin SDIP and a 64-pin QFP package.

OTP

The KS86C6308 microcontroller is also available in OTP (One Time Programmable) version, KS86P6308. KS86P6308 microcontroller has an on-chip 8-Kbyte one-time-programmable EPROM instead of masked ROM. The KS86P6308 is comparable to KS86C6308, both in function and in pin configuration.

FEATURES

CPU

- SAM88RCRI CPU core

Memory

- 8-KB Internal program memory(ROM)
- 256-byte internal register file

  (160-byte:General Purpose)

Instruction Set

- 41 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 332ns at 12 MHz f_{OSC}

Interrupts

- 32 interrupt sources with one vector, each source has its pending bits
- One level, one vector interrupt structure

Oscillation Frequency

- 12 MHz crystal/ceramic oscillator
- External clock source

General I/O

- Bit programmable five I/O ports (30 pins total)

Timer A

- One 8-bit basic timer for watchdog function and programmable oscillation stabilization programmable 8-bit timer internal generation function interval, capture, PWM mode match/capture overflow interrupt

Timer B

- Programmable 16-bit timer interval generation function interval, capture, PWM mode match/capture overflow interrupt

Universal Serial Bus with HUB

- 1 upstream port
- 4 downstream port and one embedded function each port supports separated enable LED built-in 3.3 V voltage regulator

USB/GPIO Function

- Upstream port

Operation Temperature Range

- - 40 °C to + 85 °C

Operation Voltage Range

- 4.0 V to 5.5 V

Package Types

- 64-pin SDIP
- 64-pin QFP

BLOCK DIAGRAM

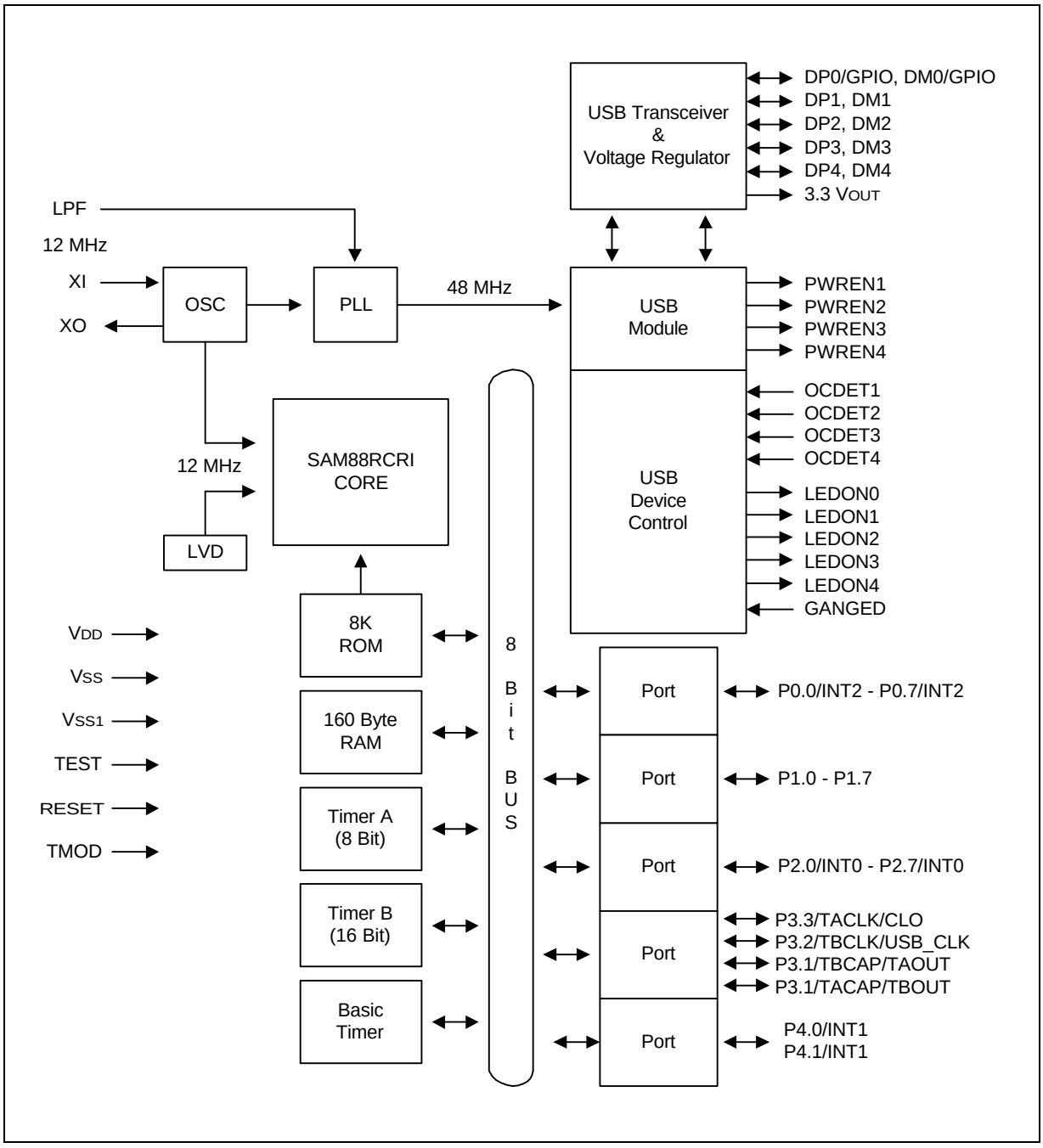


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

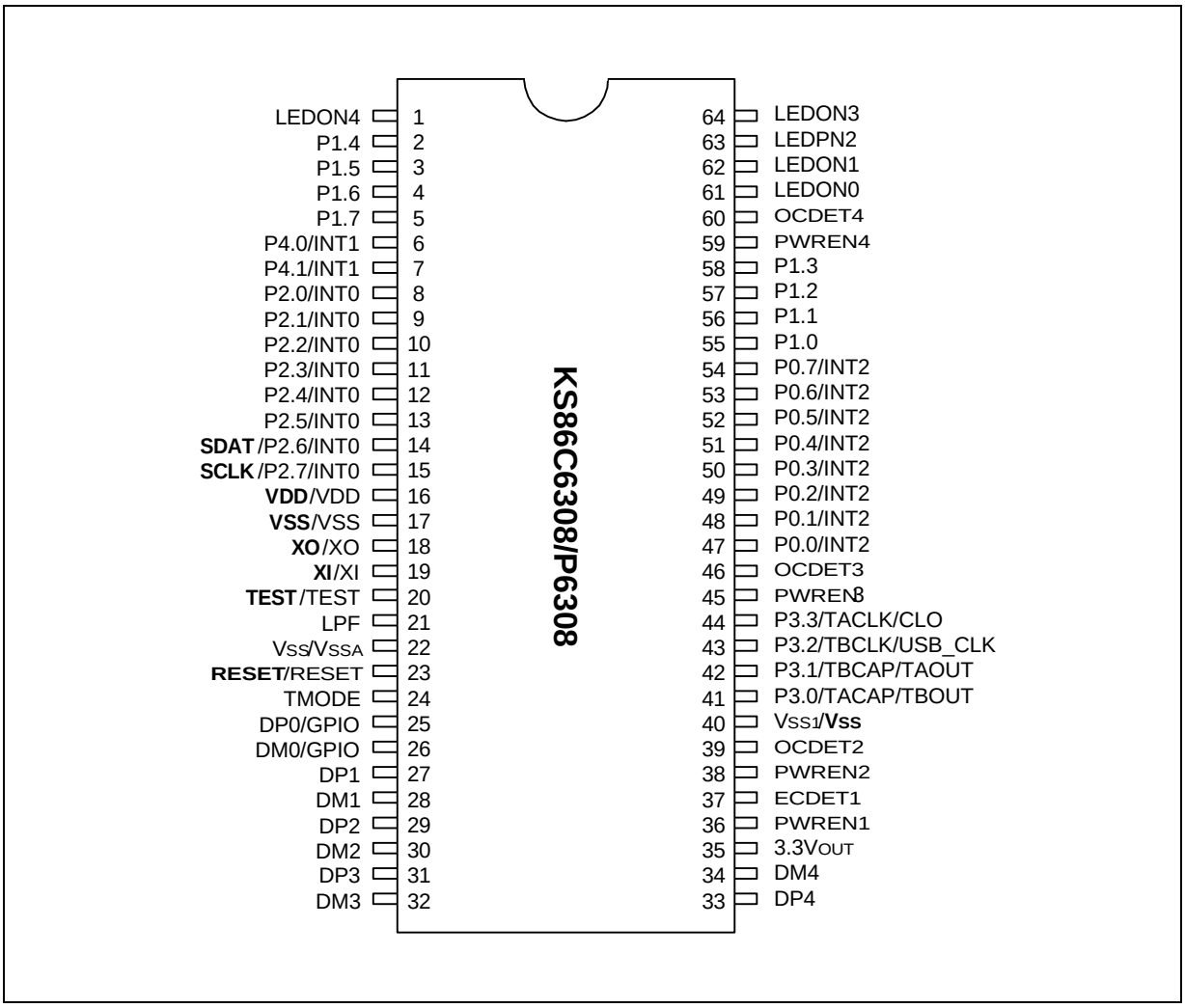


Figure 1-2. Pin Assignment Diagram (64-Pin SDIP Package)

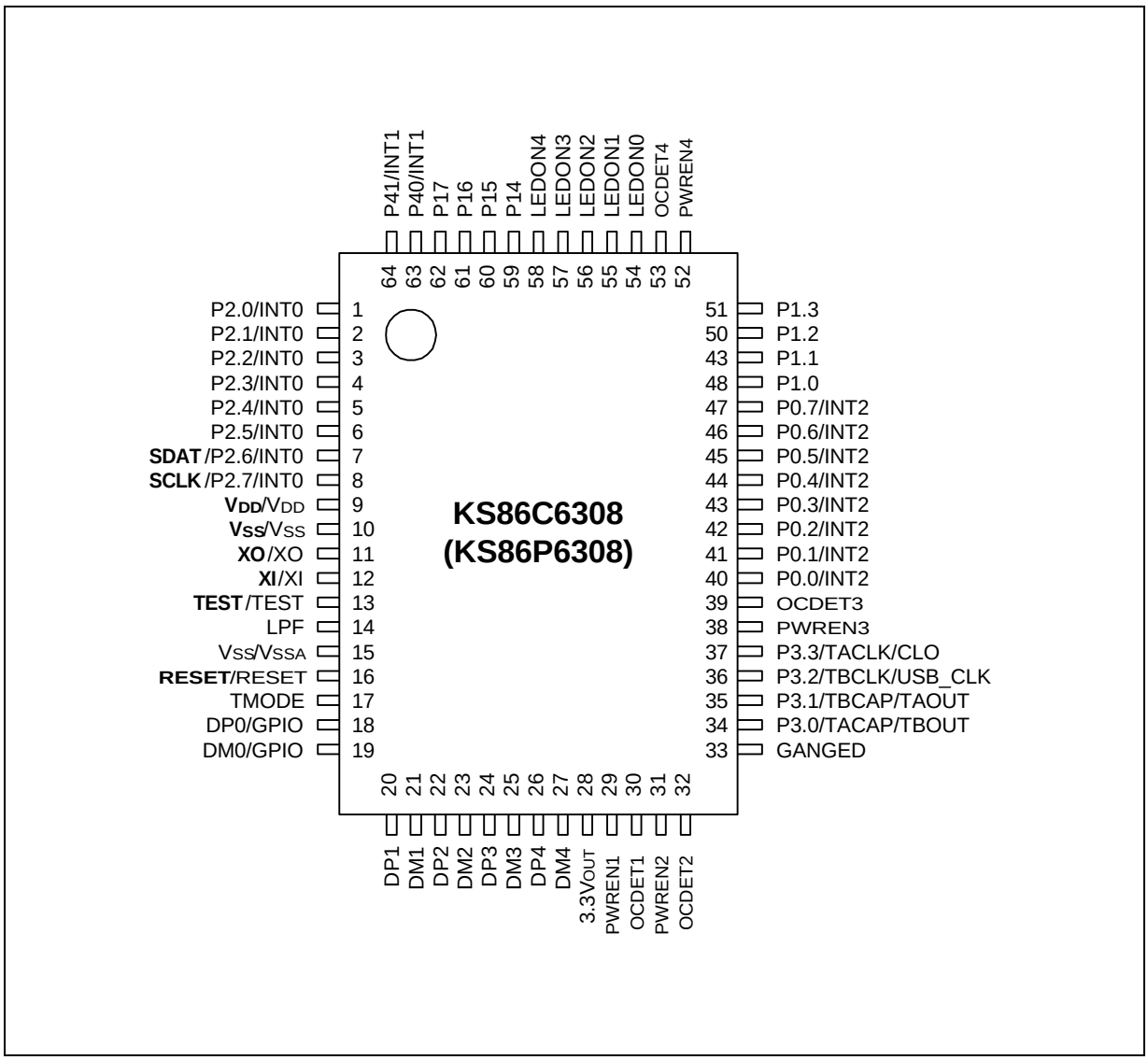


Figure 1-3. Pin Assignment Diagram (64-Pin QFP Package)

PIN DESCRIPTIONS

Table 1-1. KS86C6308/P6308 Pin Descriptions

Pin Names	I/O	Pin Description	Pin Type	Share Pins
P0.0-P0.7	I/O	Bit-programmable I/O port for Schmitt trigger input or open-drain output. Port 0 can be individually configured as external interrupt inputs. Pull-up resistors are assignable by software.	B	INT2
P1.0-P1.7	I/O	Bit-programmable I/O port for Schmitt trigger input or open-drain output. Pull-up resistors are assignable by software.	B	–
P2.0-P2.7	I/O	Bit-programmable I/O port for Schmitt trigger input or open-drain output. Port 2 can also be individually configured as external interrupt inputs. Pull-up resistors are assignable by software.	B	INT0
P3.0-P3.3	I/O	Bit-programmable I/O port for Schmitt trigger input, open-drain output or push-pull output. Port 3 are designed for to drive LED directly. P3.3 can be used to system clock output(CLO) pin. P3.2 PLL clock out for PLL Block.	C	P3.3/TACLK/CLO P3.2/TBCLK/ USB_CLK P3.1/TBCAP/TAOUT P3.0/TACAP/TBOUT
P4.0-P4.1	I/O	Bit-programmable I/O port for Schmitt trigger input or open-drain output or push-pull output. Port4 can also be individually configured as external interrupt inputs. In output mode, pull-up resistors are assignable by software. But in input mode, pull-up resistors are fixed.	D	INT1
3.3 V_{OUT}	–	3.3 V output from internal voltage regulator	–	–
X_{IN} X_{OUT}	–	System clock input and output pin (crystal/ceramic oscillator, or external clock source)	–	–
INT0 INT1 INT2	I	External interrupt for bit-programmable port0, port2 and port4 pins when set to input mode.	–	P2.0-P2.7 P4.0/P4.1 P0.0/P0.7
RESET	I	RESET signal input pin with LVD	A	–
LPF	I	Low Pass Filter Pin for PLL	–	–
TEST	I	Test signal input pin (for factory use only; must be connected to V_{SS})	–	–
TMODE	I	Test signal input pin (for factory use only, must be connected to V_{SS})	–	–
V_{DD}	–	Power input pin	–	–
V_{SS} V_{SS1}	–	VSS1 is a ground power for CPU core. VSS2 is a ground power for I/O and OSC block.	–	–

Table 1-1. KS86C6308/P6308 Pin Descriptions (Continued)

Pin Names	I/O	Pin Description	Pin Type	Share Pins
DP1, DM1 DP2, DM2 DP3, DM3 DP4, DM4	I/O	These pins are an USB Downstream pins.	K	–
DP0/GPIO DM0/GPIO	I/O	These pins are an USB Upstream pin, programmable port for USB interface or General purpose I/O interface.	–	–
LEDON0	O	Root port LED enable. N-channel open-drain output. = 0 Turn LED ON. HUB not Suspend = 1 Turn LED OFF. Reset, Suspend, Transfer in progress	G	–
LEDON1-4	O	Four downstream port LED enable. N-channel open-drain output. = 0 Turn LED ON. Port Enable and HUB not Suspend = 1 Turn LED OFF. Reset, Suspend, Transfer in progress	G	–
OCDET1-4	I	Four downstream power sense = 0 Over Current Detected = 1 Power Okay	F	–
PWREN1-4	O	Power on/off control signals. PWREN1 - PWREN4 are active low, N-CH open-drain outputs. In GANGED mode, all output are swithed together.	G	–
GANGED	I	Gang or Individual Power Control of downstream ports = 0 Individual = 1 Gang	F	–

PIN CIRCUIT DIAGRAMS

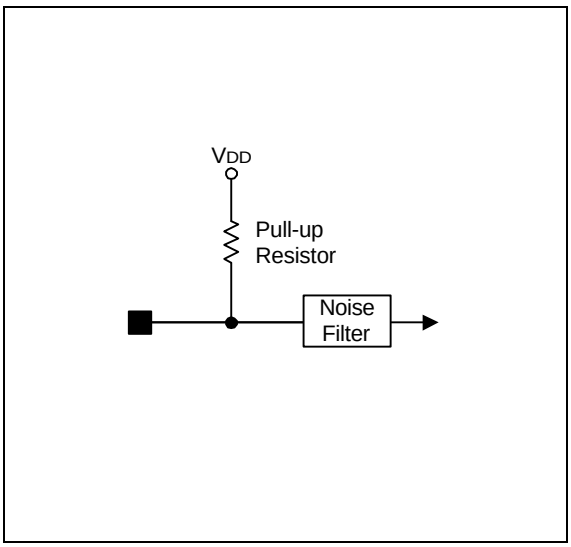


Figure 1-4. Pin Circuit Type A (RESET)

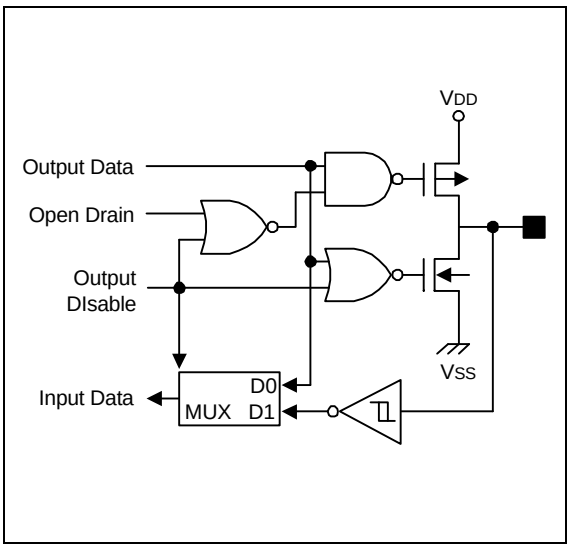


Figure 1-6. Pin Circuit Type C (Port 3)

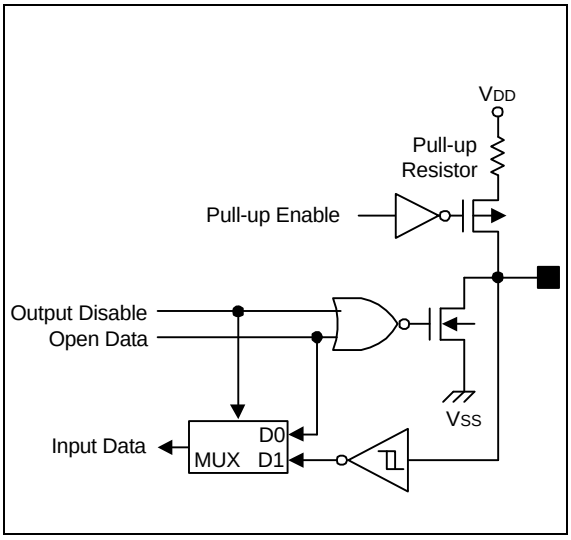


Figure 1-5. Pin Circuit Type B (Port 0, 1, 2)

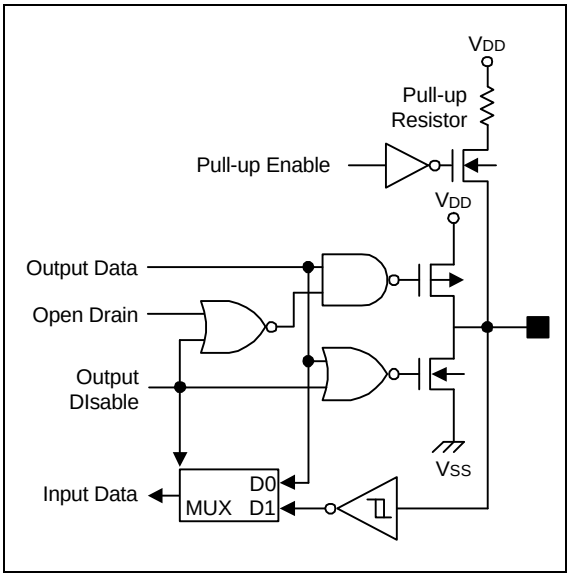


Figure 1-7. Pin Circuit Type D (Port 4)

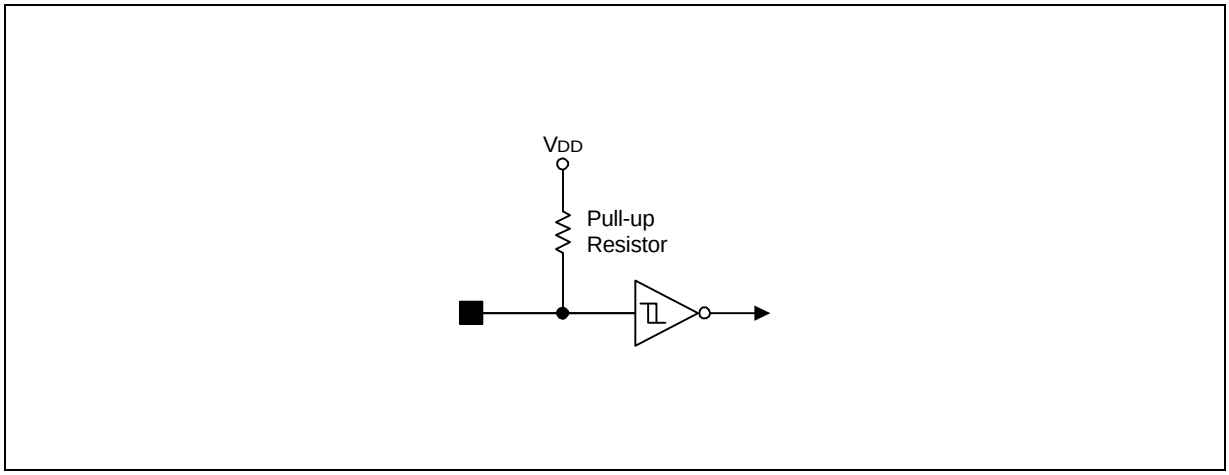


Figure 1-8. Pin Circuit Type F

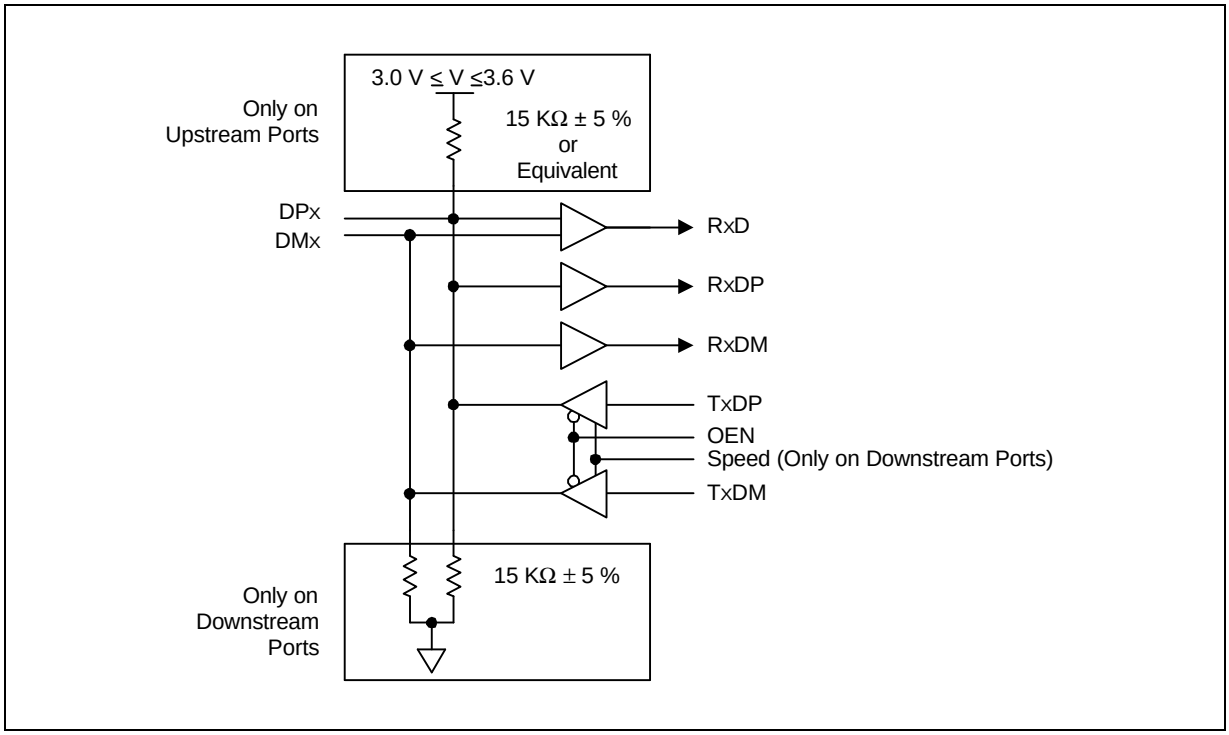


Figure 1-9. Pin Circuit Type K

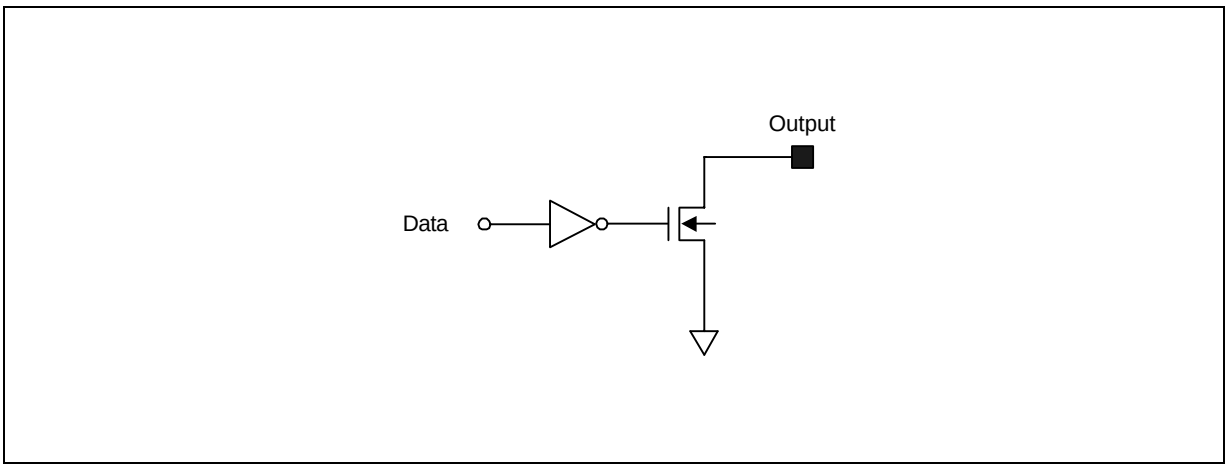
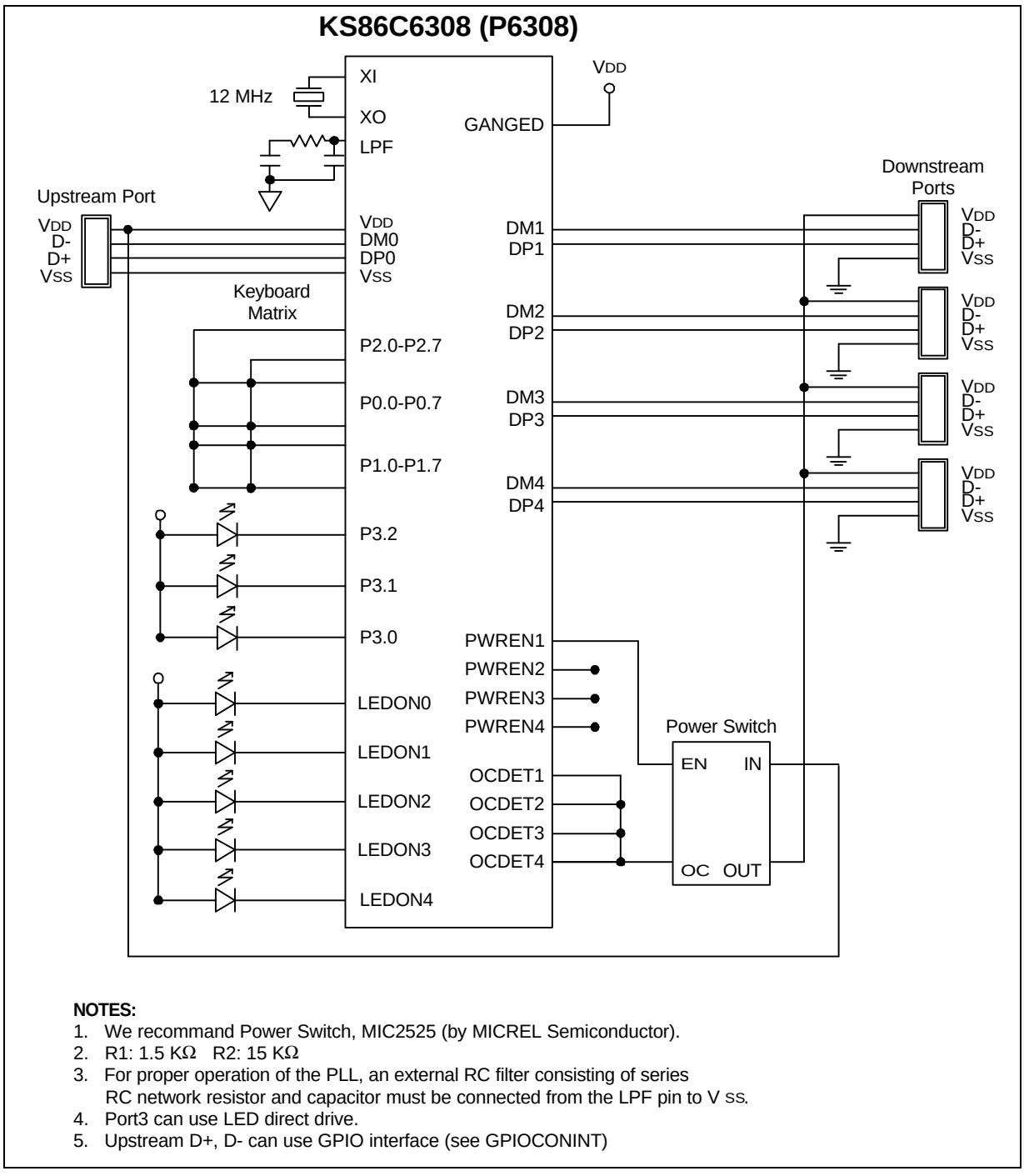


Figure 1-10. Pin Circuit Type G

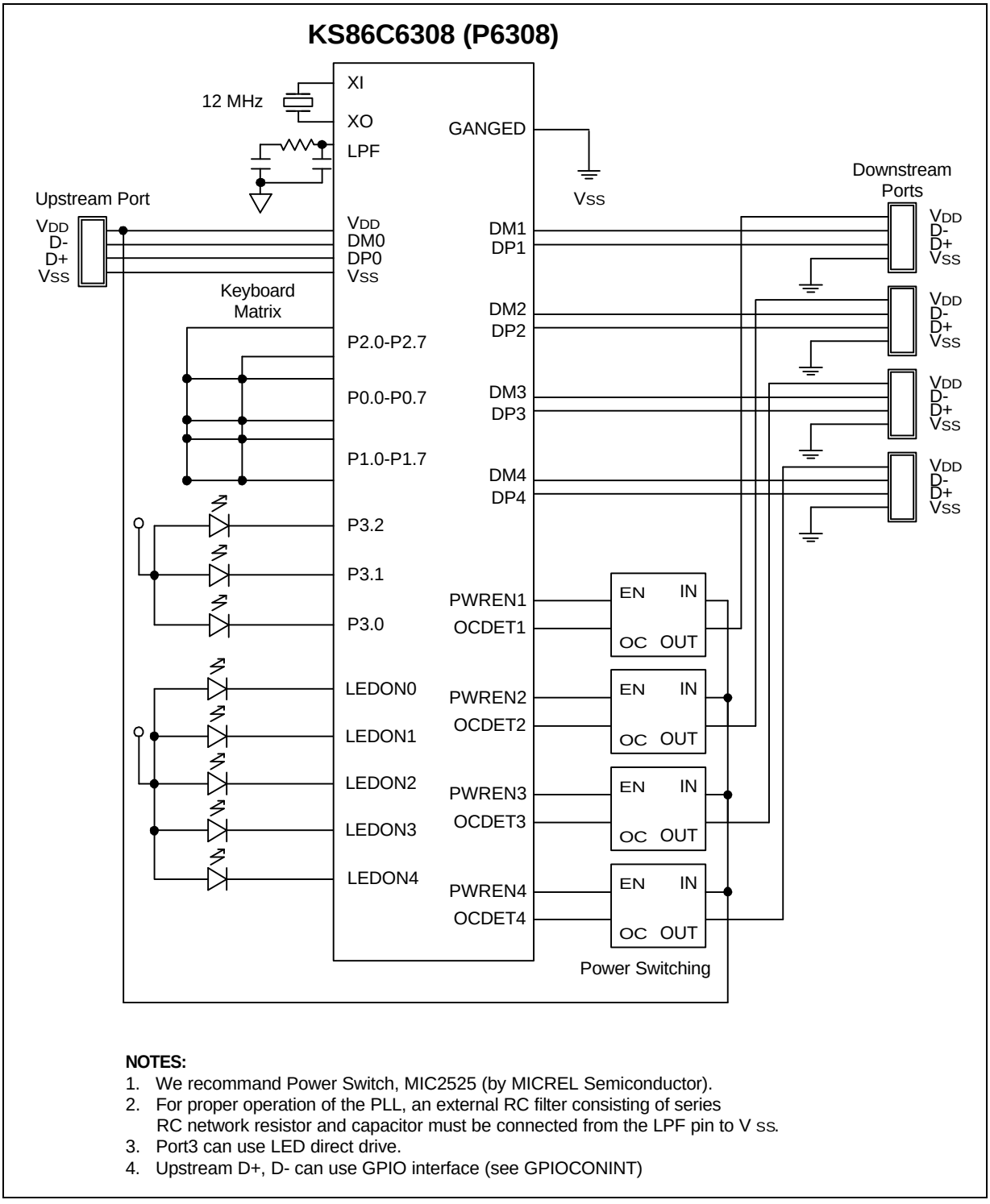
APPLICATION CITCUIT



NOTES:

1. We recommand Power Switch, MIC2525 (by MICREL Semiconductor).
2. R1: 1.5 KΩ R2: 15 KΩ
3. For proper operation of the PLL, an external RC filter consisting of series RC network resistor and capacitor must be connected from the LPF pin to V_{SS}.
4. Port3 can use LED direct drive.
5. Upstream D+, D- can use GPIO interface (see GPIOCONINT)

Figure 1-11. Bus-Powered, Gang Port (64-SDIP, 64-QFP)



NOTES:

1. We recommand Power Switch, MIC2525 (by MICREL Semiconductor).
2. For proper operation of the PLL, an external RC filter consisting of series RC network resistor and capacitor must be connected from the LPF pin to V SS.
3. Port3 can use LED direct drive.
4. Upstream D+, D- can use GPIO interface (see GPIOCONINT)

Figure 1-12. Bus-Powered, Individual Port (64-SDIP, 64-QFP)

12 ELECTRICAL DATA

OVERVIEW

In this section, the following KS86C6308/P6308 electrical characteristics are presented in tables and graphs:

— Absolute maximum ratings
— D.C. electrical characteristics
— Input/Output capacitance
— A.C. electrical characteristics
— Input timing for external interrupt (Ports 0, 2 and 4) DP0/GPIO, DM0/GPIO : GPIO Mode Only
— Input timing for RESET
— Oscillator characteristics
— Oscillation stabilization time
— Clock timing measurement points at X_{IN}
— Data retention supply voltage in Stop mode
— Stop mode release timing when initiated by a reset
— Stop mode release timing when initiated by an external interrupt
— Characteristic curves

Table 12-1. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_{IN}	All input ports	– 0.3 to V_{DD} + 0.3	V
Output Voltage	VO	All output ports	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output Current Low	I_{OL}	One I/O pin active	+ 30	mA
		Total pin current for ports 0, 1, 2, 4	+ 100	
		Total pin current for port 3	+ 100	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{STG}	–	– 65 to + 150	°C

Table 12-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 4.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	f_{OSC} = 12 MHz	4.0	–	5.5	V
Input High Voltage	V_{IH1}	All input except V_{IH2}	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	X_{IN}	V_{DD} – 0.5		V_{DD}	
Input Low Voltage	V_{IL1}	All input pins except V_{IL2}	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN}			0.4	
Output High Voltage	V_{OH}	I_{OH} = – 200 µA; All output ports except ports 0, 1, 2, DP's, DM's	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL}	I_{OL} = 1 mA All output ports except DP's, DM's	–	–	0.4	V
Input High Leakage Current	I_{LIH1} (4)	V_{IN} = V_{DD} All inputs excepts I_{LIH2}, DP's, DM's	–	–	3	µA
	I_{LIH2} (4)	V_{IN} = V_{DD} X_{IN}, X_{OUT}, RESET	–	–	20	µA
Input Low Leakage Current	I_{LIL1} (4)	V_{IN} = 0 V All inputs excepts I_{LIL2}, DP's, DM's	–	–	– 3	µA
	I_{LIL2} (4)	V_{IN} = 0 V X_{IN}, X_{OUT}, RESET	–	–	– 20	µA

Table 12-2. D.C. Electrical Characteristics (continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 4.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output High Leakage Current	I_{LOH} (1)	$V_{OUT} = V_{DD}$ All I/O pins and output pins except DP's and DM's	–	–	3	µA
Output Low Leakage Current	I_{LOL} (1)	V_{OUT} = 0 V All I/O pins and output pins except DP's and DM's	–	–	– 3	µA
Pull-up Resistors	R_L	V_{IN} = 0 V Ports 0, 1, 2, 4, Reset	25	50	100	kΩ
Supply Current	I_{DD1}	Normal operation mode : 12 MHz Crystal Oscillator	–		30	mA
	I_{DD2}	Idle mode; 12 MHz Crystal Oscillator			15	
	I_{DD3}	Stop mode: Oscillator stop			500	µA

NOTES:
1. Except X_{IN} and X_{OUT}.
2. Supply current does not include through internal pull-up resistors or external output current loads.
3. Figure 11-3 Transition Rise Timer (tR), Fall Timer (tF) parameter is guaranteed, but not tested.
3. When USB Mode Only in 4.20 V to 5.25 V, DP's and DP's satisfy the USB Specification version 1.0.

Table 12-3. Input/Output Capacitance

(T_A = – 40 °C to + 85 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are connected to V_{SS}	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 12-4. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 4.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	P0, P2 and P4	–	200	–	ns
RESET Input Low Width	t_{RSL}	RESET	–	1000	–	

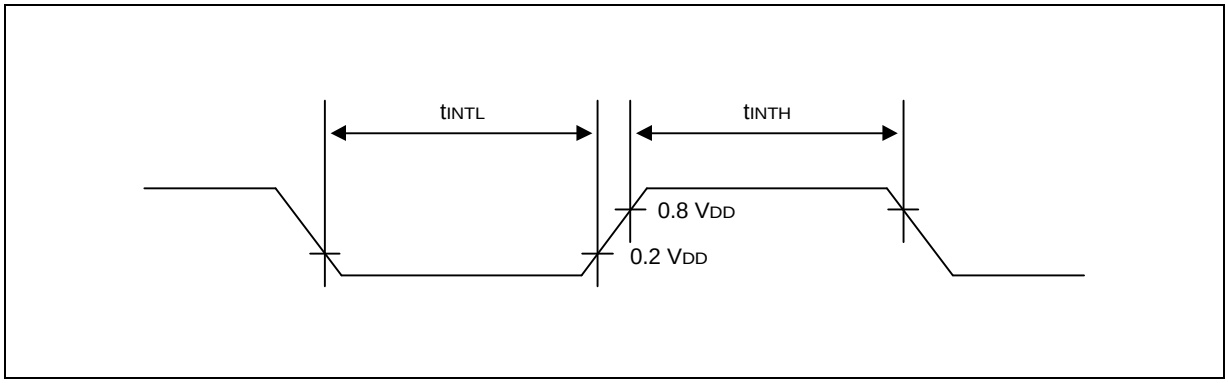


Figure 12-1. Input Timing Measurement Points (Ports 0, 2, and 4)

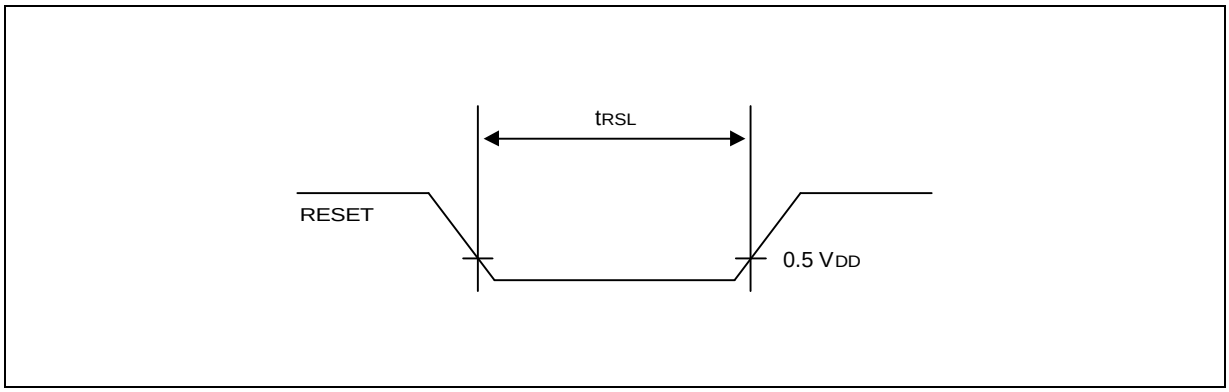


Figure 12-2. Input Timing for RESET

Figure 12-3. USB Data Signal Timing

Table 12-5. DPx, DMx Driver Characteristics, Full Speed Operation

Symbol	Parameter	Condition	Min	Max	Unit
t_R	Rise Time	C_L = 50pF	4	20	ns
t_F	Fall Time	C_L = 50pF	4	20	ns
t_{RFM}	t_R/t_F Matching	–	90	11	%

Table 12-6. DPx, DMx Driver Characteristics, Low Speed Operation

Symbol	Parameter	Condition	Min	Max	Unit
t_R	Rise Time	C_L = 200-600pF	75	300	ns
t_F	Fall Time	C_L = 200-600pF	75	300	ns
t_{RFM}	t_R/t_F Matching	–	80	125	%

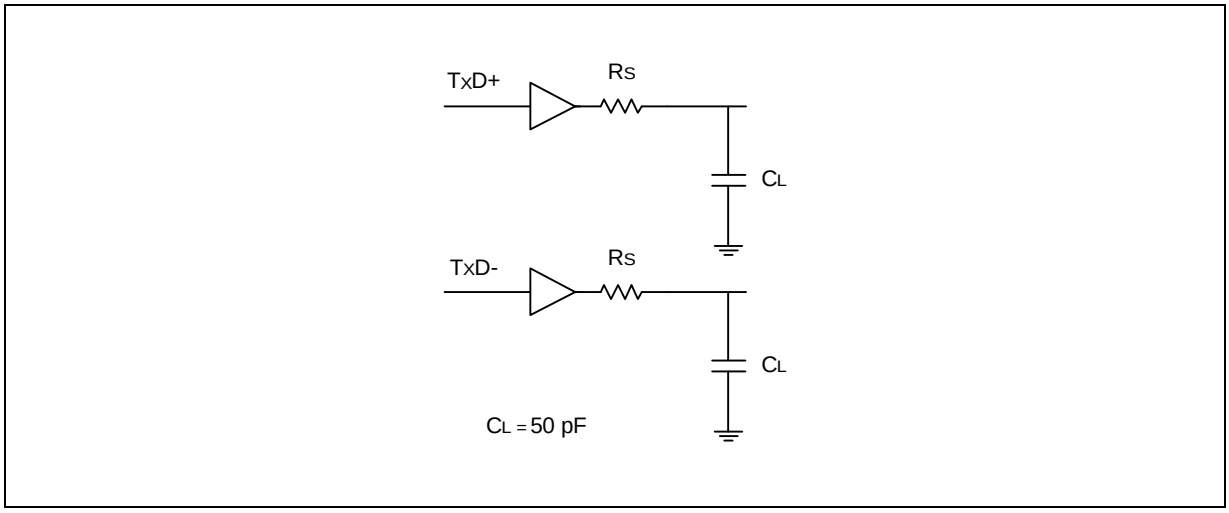


Figure 12-4. Full-Speed Load

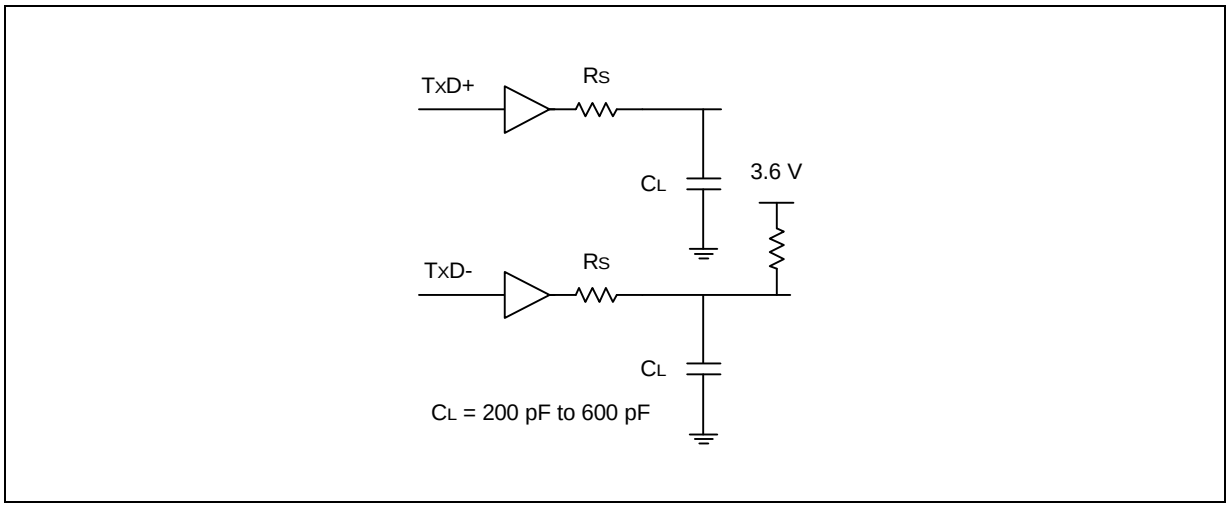


Figure 12-5. Low-Speed Load

Table 12-7. Oscillator Characteristics

(T_A = – 40°C + 85°C)

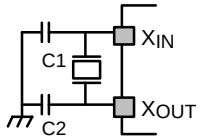
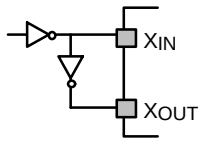
Oscillator	Circuit	Condition	Min	Typ	Max	Unit
Main crystal Main ceramic (f_{OSC})		V_{DD} = 4.0V to 5.5V	–	12	–	MHz
External clock		V_{DD} = 4.0V to 5.5V	–	12	–	

Table 12-8. Oscillation Stabilization Time

(T_A = – 40°C + 85°C, V_{DD} = 4.0 V to 5.5 V)

Oscillator	Symbol	Condition	Min	Typ	Max	Unit
Crystal	–	V_{DD} = 4.0V to 5.5V	–	–	20	ms
Ceramic	–		–	–	10	
External	–	XIN input high & low level width	25	–	500	ns

NOTE: The oscillator stabilization wait time, t_{WAIT}, is determined by the setting in the basic timer control register, BTCON.

Table 12-9. Data Retention Supply Voltage in Stop Mode

(T_A = – 40°C to + 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Supply Voltage	V_{DDDR}	Stop mode	2.0	–	6	V
Data Retention Supply Current	I_{DDDR}	Stop mode; V_{DDDR} = 2.0 V	–	–	500	uA

13 MECHANICAL DATA

OVERVIEW

The KS86C6308/P6308 is available in a 64-pin SDIP package (Samsung: 64-SDIP-750) and a 64-pin QFP package (64-QFP-1420F). Package dimensions are shown in Figures 13-1 and 13-2.

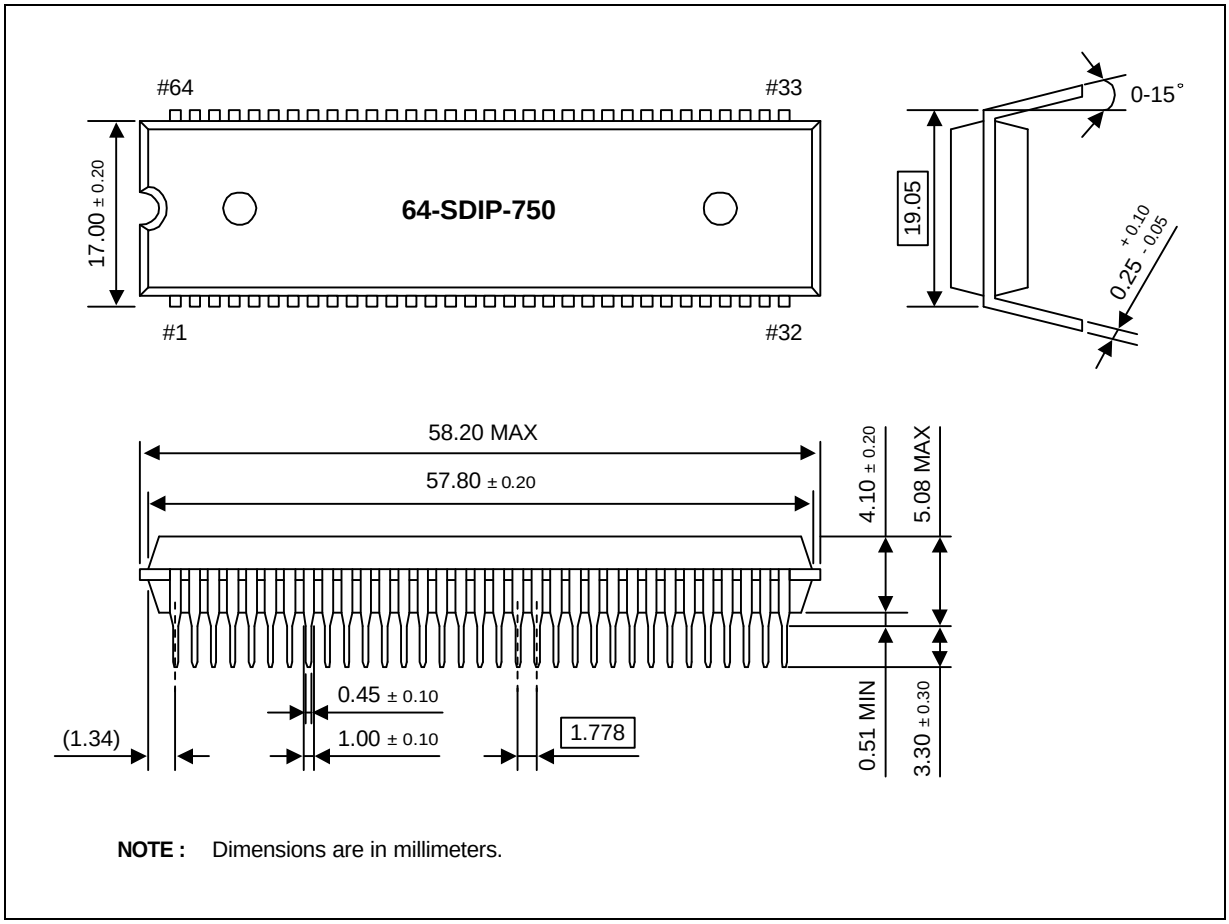
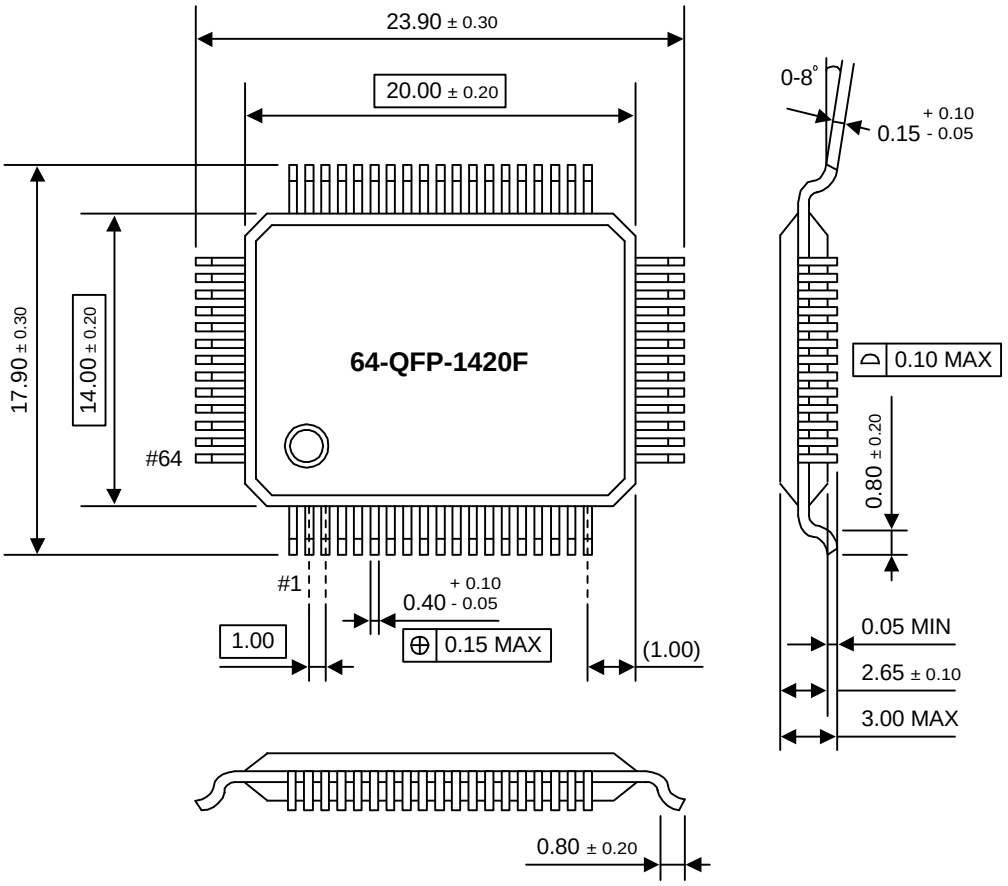


Figure 13-1. 64-Pin SDIP Package Mechanical Data (64-SDIP-750)



NOTE : Dimensions are in millimeters.

Figure 13-2. 64-Pin QFP Package Mechanical Data (64-QFP-1420F)

14 KS86P6308 OTP

OVERVIEW

The KS86P6308 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the KS86C6308 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The KS86P6308 is fully compatible with the KS86C6308, both in function and in pin configuration. Because of its simple programming requirements, the KS86P6308 is ideal for use as an evaluation chip for the KS86C6308.

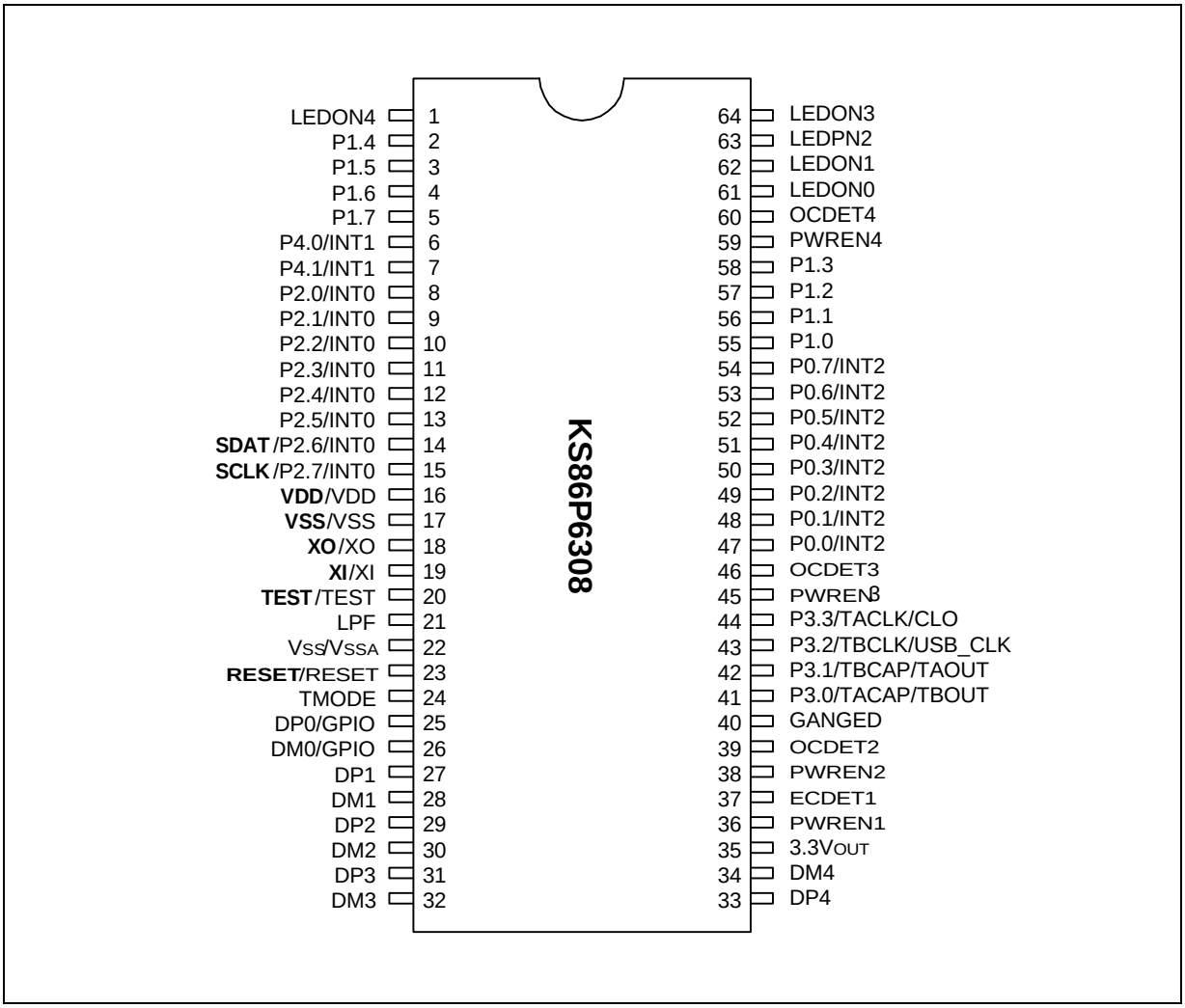


Figure 14-1. Pin Assignment Diagram (64-Pin SDIP Package)

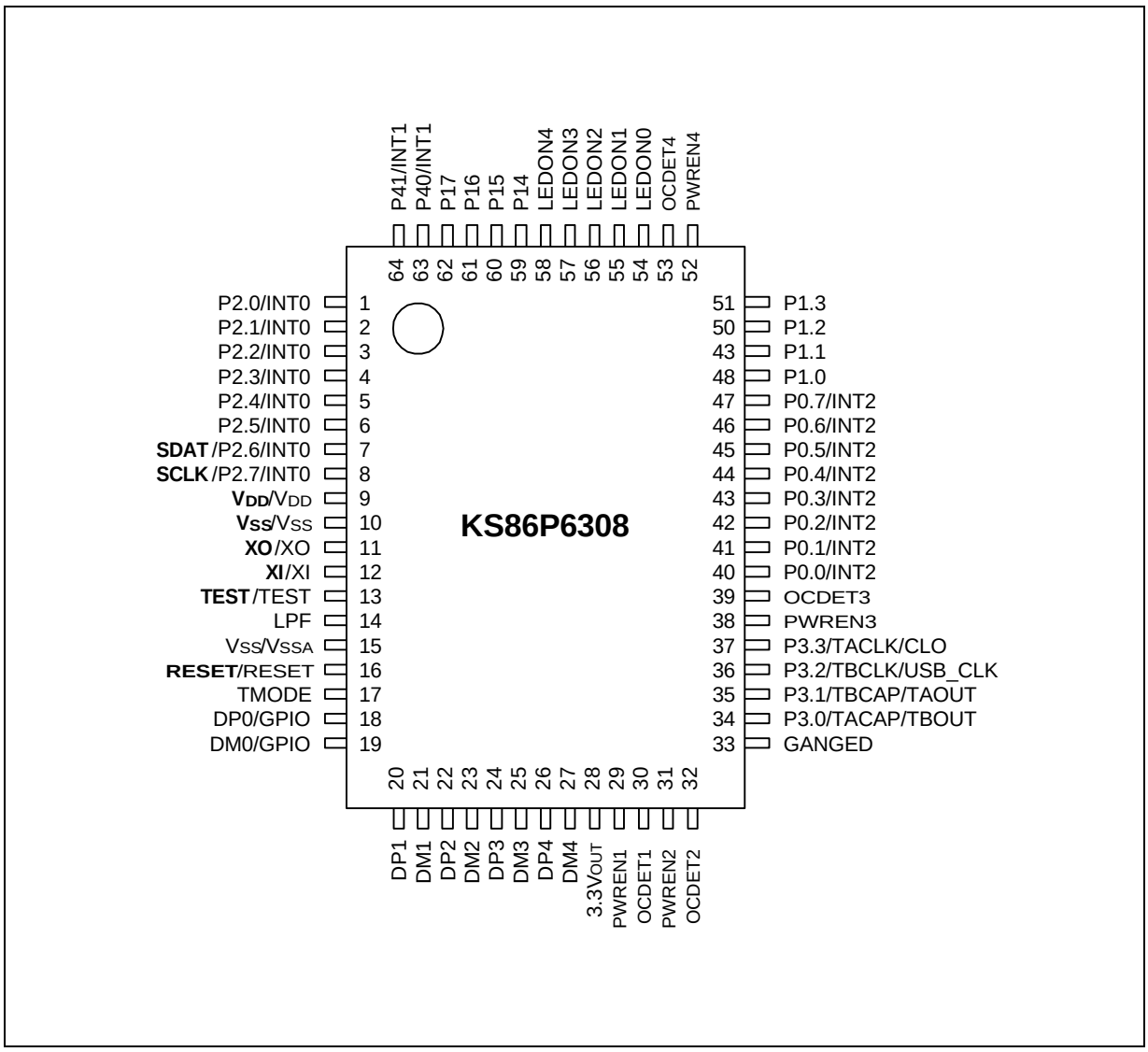


Figure 14-2. Pin Assignment Diagram (64-Pin QFP Package)

Table 14-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P2.6	SDAT	9 (3)	I/O	Serial Data Pin (Output when reading, Input when writing) Input and Push-pull Output Port can be assigned
P2.7	SCLK	10 (4)	I/O	Serial Clock Pin (Input Only Pin)
TEST	TEST	15 (9)	I	Chip Initialization and EPROM Cell Writing Power Supply Pin (Indicates OTP Mode Entering) When writing 12.5 V is applied and when reading.
RESET	RESET	18 (12)	I	0 V: OTP write and test mode 5 V: Operating mode
V_{DD} / V_{SS}	V_{DD} / V_{SS}	11(5)/12(6)	–	Logic Power Supply Pin.

NOTE: ( ) means 64 QFP package.

Table 14-2. Comparison of KS86P6308 and KS86C308 Features

Characteristic	KS86P6308	KS86C6308
Program Memory	8-Kbyte EPROM	8-Kbyte mask ROM
Operating Voltage (V_{DD})	4.0 V to 5.25 V	4.0 V to 5.25 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (RESET) = 12.5 V	
Pin Configuration	64 SDIP/64 QFP	64 SDIP/64 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the VPP (RESET) pin of the KS86P6308, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 14-3 below.

Table 14-3. Operating Mode Selection Criteria

V_{DD}	VPP (RESET)	REG/ MEM	ADDRESS (A15-A0)	R/W	MODE
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

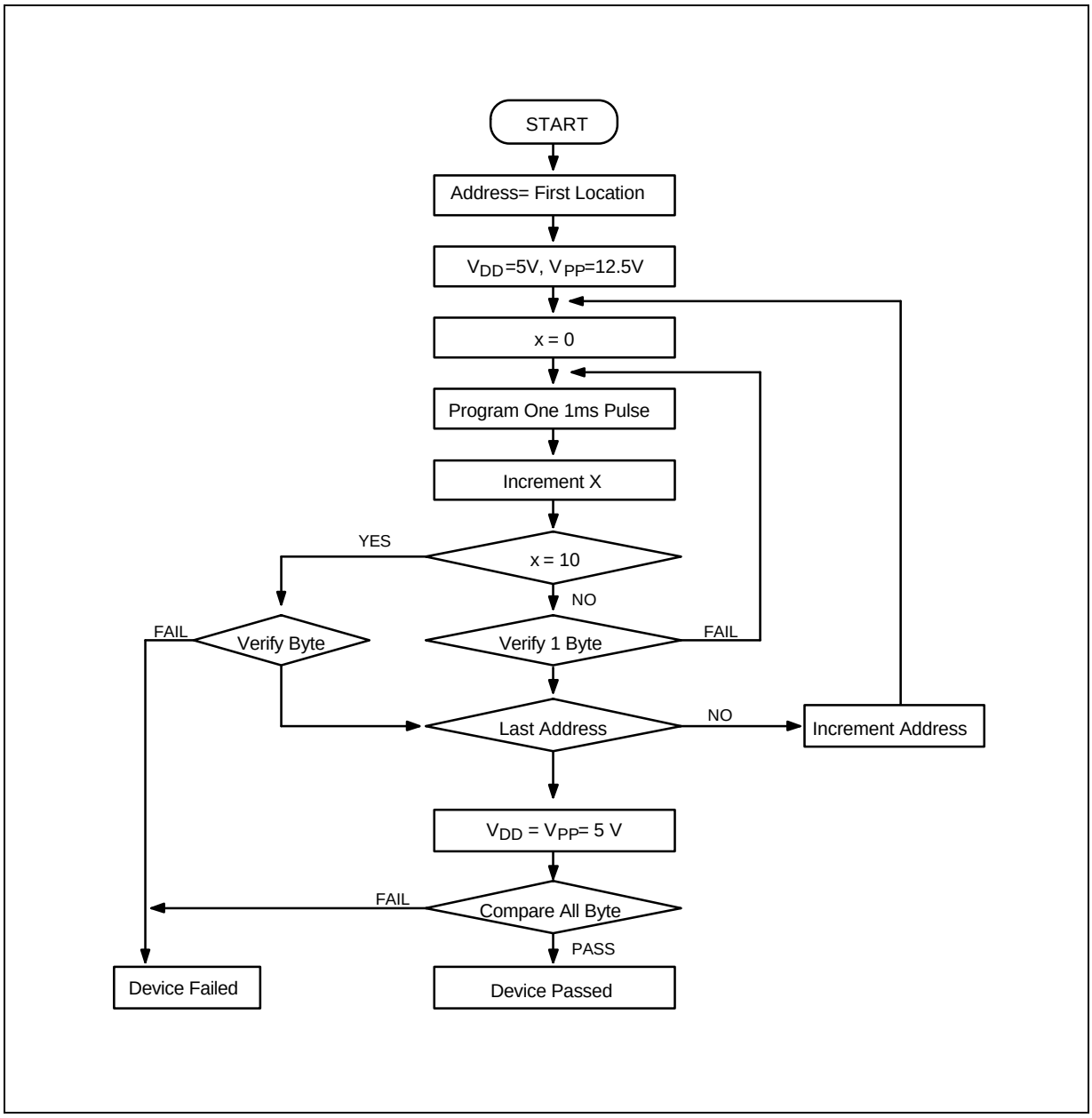


Figure 14-3. OTP Programming Algorithm

Table 14-4. D.C. Electrical Characteristics

(T_A = – 40_C to + 85_C, V_{DD} = 5.25 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Current (note)	I_{DD1}	Normal mode; 12 MHz crystal oscillator	–	–	30	mA
	I_{DD2}	Idle mode; 12 MHz CPU clock		–	15	
	I_{DD3}	Stop mode		–	500	µA

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.