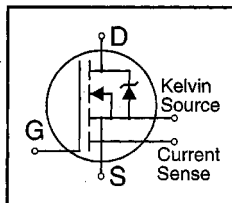


## HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Current Sense
- Isolated Central Mounting Hole
- 175°C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



$$V_{DSS} = 60V$$

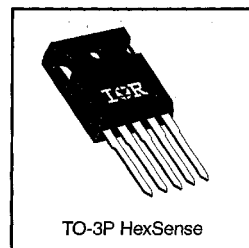
$$R_{DS(on)} = 0.014\Omega$$

$$I_D = 70^*A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The HEXSense device provides an accurate fraction of the drain current through the additional two leads to be used for control or protection of the device. These devices exhibit similar electrical and thermal characteristics as their IRF-series equivalent part numbers. The provision of a kelvin source connection effectively eliminates problems of common source inductance when the HEXSense is used as a fast, high-current switch in non current-sensing applications.



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### Absolute Maximum Ratings

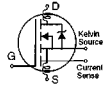
	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{ V}$	70*	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{ V}$	64	
$I_{DM}$	Pulsed Drain Current ①	360	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation	230	W
	Linear Derating Factor	1.5	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	640	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
$T_J$	Operating Junction and	-55 to +175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	

### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.65	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	40	

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.056	—	V/°C	Reference to 25°C, I <sub>D</sub> =1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.014	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =54A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
g <sub>fs</sub>	Forward Transconductance	25	—	—	S	V <sub>DS</sub> =25V, I <sub>D</sub> =54A ④
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> =20V
	Gate-to-Source Reverse Leakage	—	—	-100	nA	V <sub>GS</sub> =-20V
Q <sub>g</sub>	Total Gate Charge	—	—	160	nC	I <sub>D</sub> =64A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	48	nC	V <sub>DS</sub> =48V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	54	nC	V <sub>GS</sub> =10V See Fig. 6 and 13 ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	20	—	ns	V <sub>DD</sub> =30V I <sub>D</sub> =64A R <sub>G</sub> =6.2Ω R <sub>D</sub> =0.45Ω See Figure 10 ④
t <sub>r</sub>	Rise Time	—	160	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	83	—		
t <sub>f</sub>	Fall Time	—	150	—		
L <sub>D</sub>	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	13	—		
C <sub>iss</sub>	Input Capacitance	—	4500	—	pF	V <sub>GS</sub> =0V V <sub>DS</sub> =25V f=1.0MHz See Figure 5
C <sub>oss</sub>	Output Capacitance	—	2000	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	300	—		
r	Current Sensing Ratio	2190	—	2430	—	I <sub>D</sub> =90A, V <sub>GS</sub> =10V
C <sub>oss</sub>	Output Capacitance of Sensing Cells	—	9.0	—	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1.0MHz



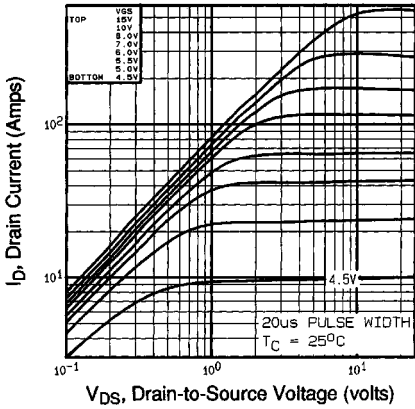
## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	70*	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	360		
V <sub>SD</sub>	Diode Forward Voltage	—	—	2.5	V	T <sub>J</sub> =25°C, I <sub>S</sub> =90A, V <sub>GS</sub> =0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	270	540	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =64A
Q <sub>rr</sub>	Reverse Recovery Charge	—	1.1	2.2	μC	di/dt=100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

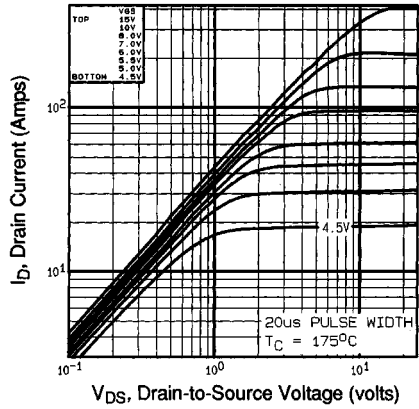
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V<sub>DD</sub>=25V, starting T<sub>J</sub>=25°C, L=92μH, R<sub>G</sub>=25Ω, I<sub>AS</sub>=90A (See Figure 12)
- ③ I<sub>SD</sub>≤90A, di/dt≤300A/μs, V<sub>DD</sub>≤V<sub>(BR)DSS</sub>, T<sub>J</sub>≤175°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.

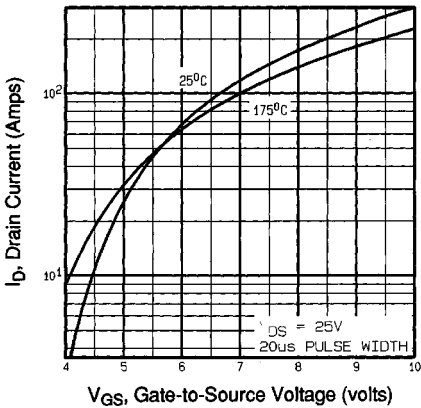
\* Current limited by the package, (Die Current =90A)



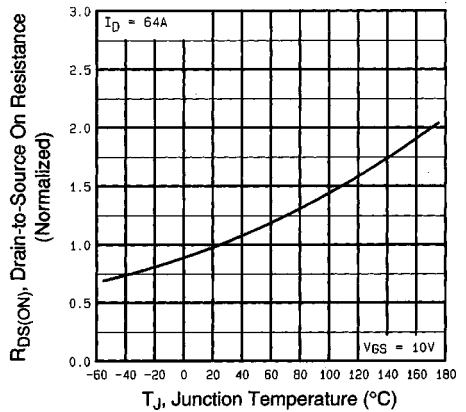
**Fig 1.** Typical Output Characteristics,  $T_C=25^\circ\text{C}$



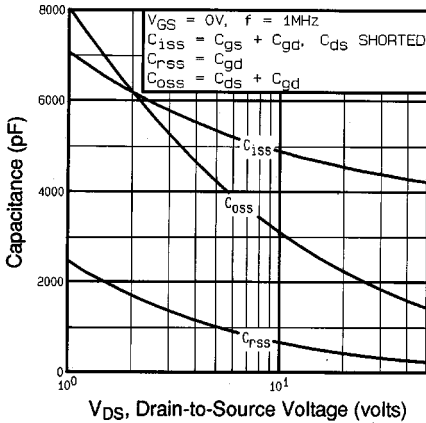
**Fig 2.** Typical Output Characteristics,  $T_C=175^\circ\text{C}$



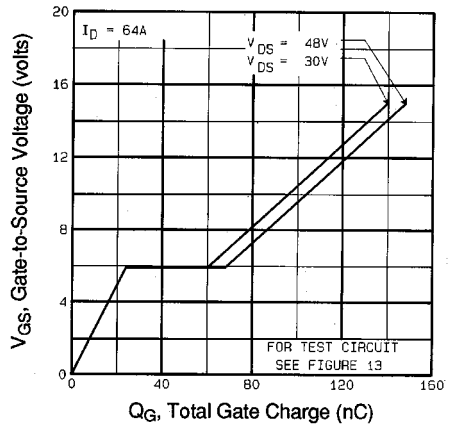
**Fig 3.** Typical Transfer Characteristics



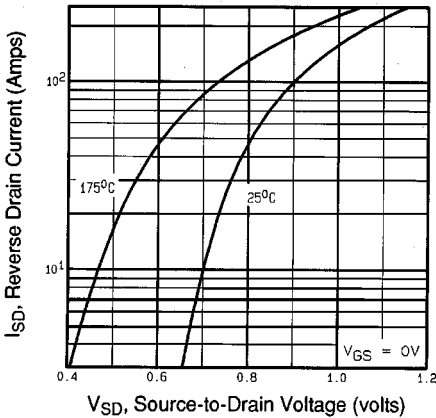
**Fig 4.** Normalized On-Resistance Vs. Temperature



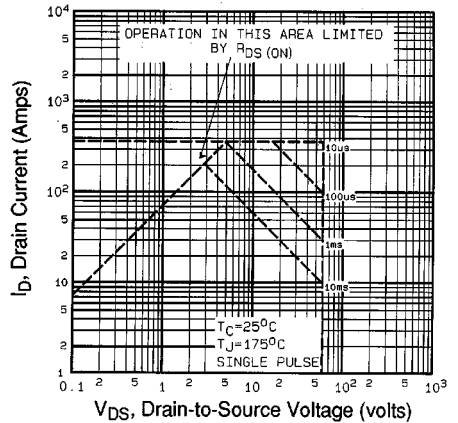
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



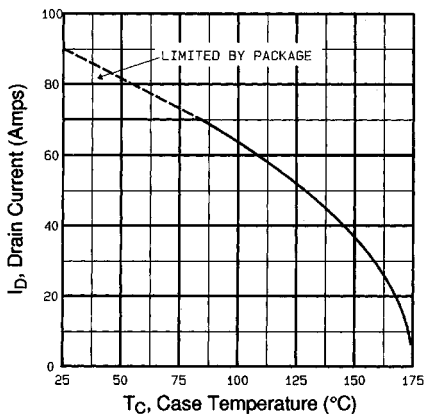
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



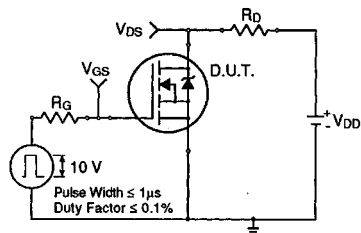
**Fig 7.** Typical Source-Drain Diode Forward Voltage



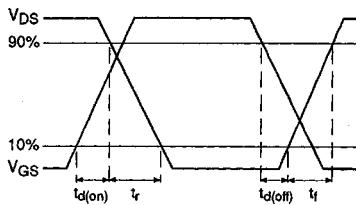
**Fig 8.** Maximum Safe Operating Area



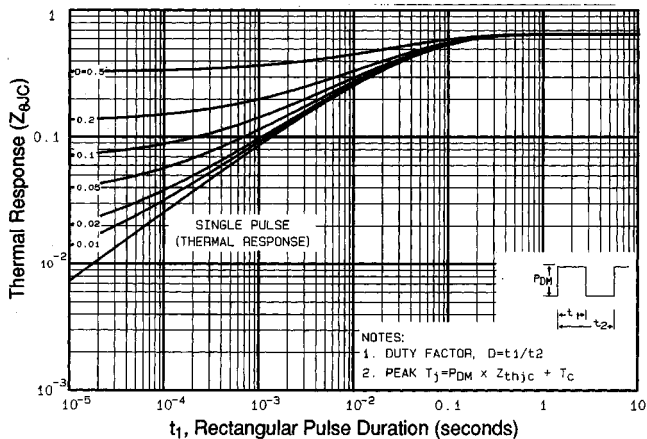
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

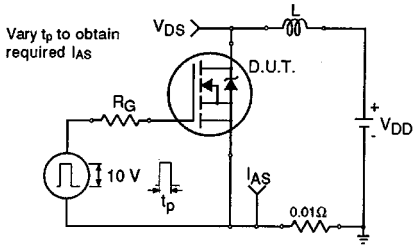


**Fig 10b.** Switching Time Waveforms

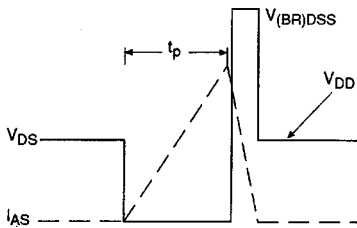


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

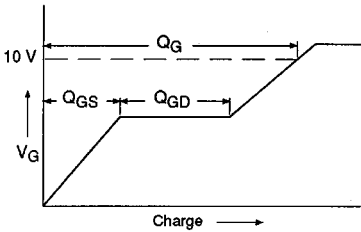
DATA SHEETS



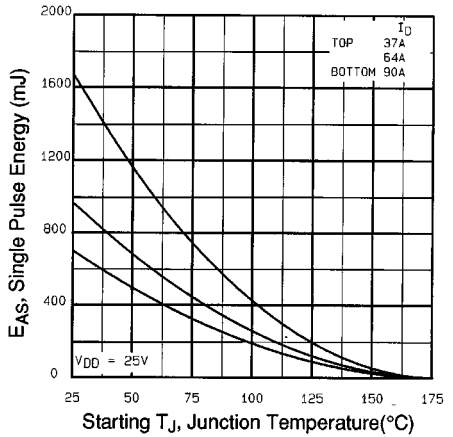
**Fig 12a.** Unclamped Inductive Test Circuit



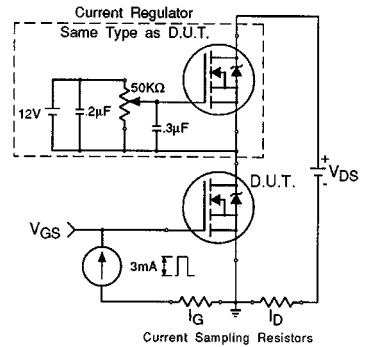
**Fig 12b.** Unclamped Inductive Waveforms



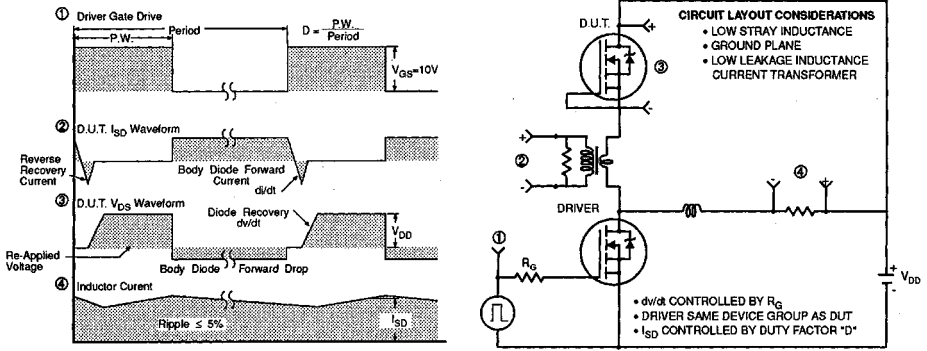
**Fig 13a.** Basic Gate Charge Waveform



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

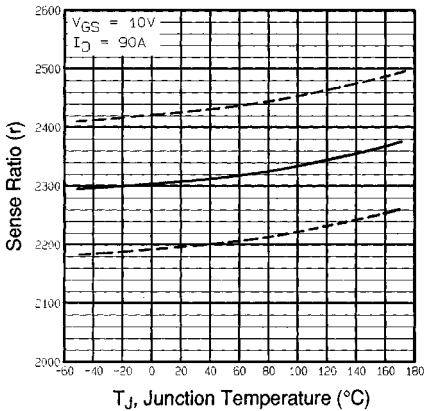


**Fig 13b.** Gate Charge Test Circuit

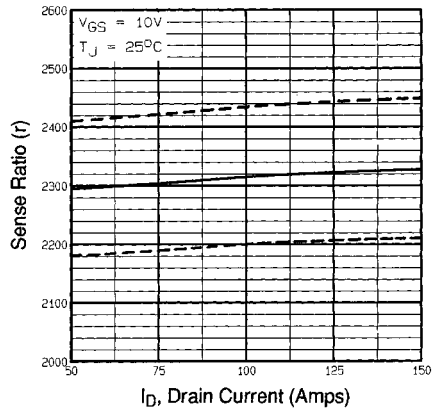


**Fig 14. Peak Diode Recovery dv/dt Test Circuit**

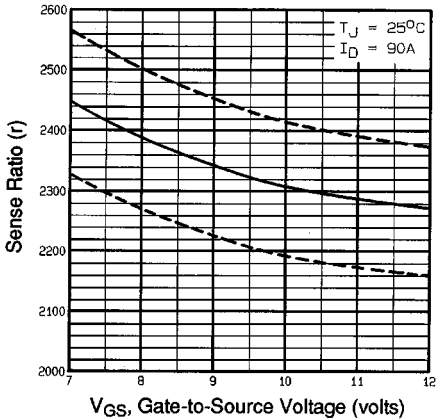
DATA SHEETS



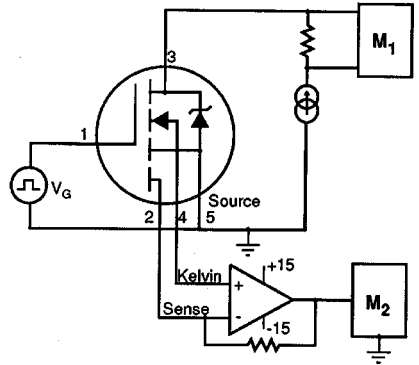
**Fig 15. Typical HEXSense Ratio Vs. Junction Temperature**



**Fig 16. Typical HEXSense Ratio Vs. Drain Current**

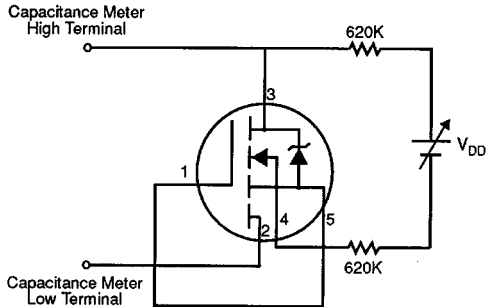


**Fig 17.** Typical HEXSense Ratio Vs. Gate Voltage



M1, M2 = HIGH SPEED DIGITAL VOLTMETERS

**Fig 18.** HEXSense Ratio Test Circuit



**Fig 19.** HEXSense Sensing Cell Output Capacitance Test Circuit

**Appendix B:** Package Outline Mechanical Drawing – See page 1512

**Appendix C:** Part Marking Information – See page 1517