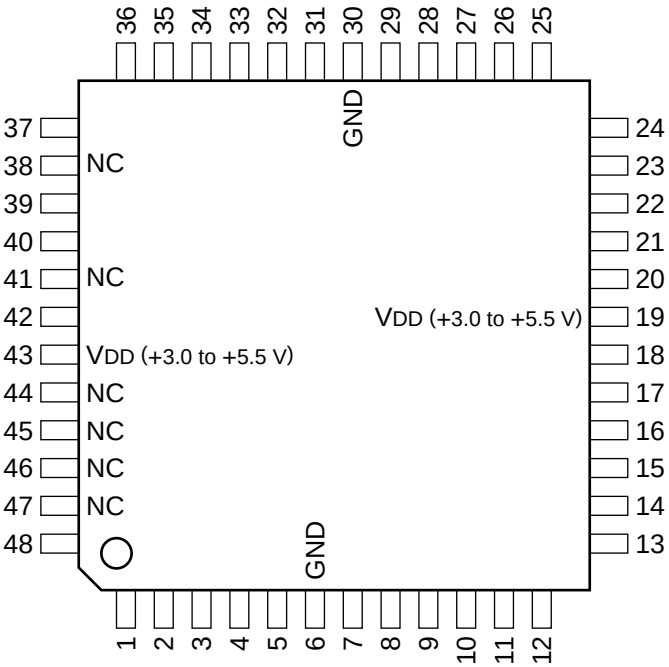
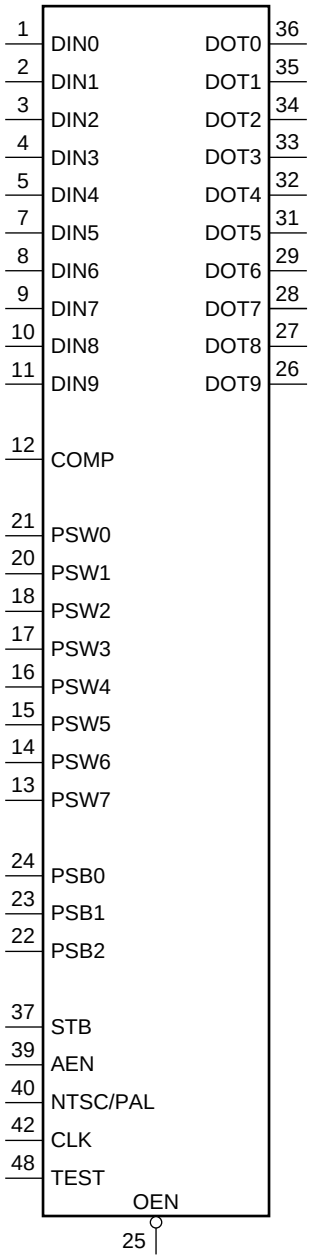
C-MOS DIGITAL LINE MEMORY

—TOP VIEW—





(VDD = +3.3 to +5.5 V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	DIN0	25	I	$\overline{\text{OEN}}$
2	I	DIN1	26	O	DOT9
3	I	DIN2	27	O	DOT8
4	I	DIN3	28	O	DOT7
5	I	DIN4	29	O	DOT6
6	—	GND	30	—	GND
7	I	DIN5	31	O	DOT5
8	I	DIN6	32	O	DOT4
9	I	DIN7	33	O	DOT3
10	I	DIN8	34	O	DOT2
11	I	DIN9	35	O	DOT1
12	I	COMP	36	O	DOT0
13	I	PSW7	37	I	STB
14	I	PSW6	38	—	NC
15	I	PSW5	39	I	AEN
16	I	PSW4	40	I	NTSC/PAL
17	I	PSW3	41	—	NC
18	I	PSW2	42	I	CLK
19	—	VDD	43	—	VDD
20	I	PSW1	44	—	NC
21	I	PSW0	45	—	NC
22	I	PSB2	46	—	NC
23	I	PSB1	47	—	NC
24	I	PSB0	48	I	TEST

INPUT

AEN	:	AMOUNT OF DELAY SELECT
CLK	:	CLOCK
COM	:	COMPATIBILITY SELECT
DIN0 - DIN9	:	DATA
NTSC/PAL	:	AMOUNT OF DELAY FOR NTSC/PAL/SECAM SELECT
OEN	:	OUTPUT ENABLE
PSB0 - PSB2	:	NUMBER OF SMALL DELAY SETTING
PSW0 - PSW7	:	NUMBER OF DELAY SETTING
STB	:	STANDBY
TEST	:	TEST

OUTPUT

DOT0 - DOT9	:	DATA