

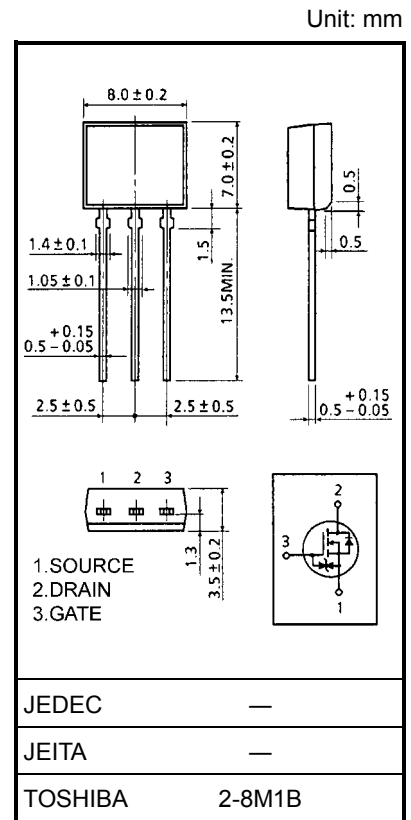
# 2SK3374

## Switching Regulator Applications

- Low drain-source ON resistance:  $R_{DS(ON)} = 4.0 \Omega$  (typ.)
- High forward transfer admittance:  $|Y_{fs}| = 0.8 S$  (typ.)
- Low leakage current:  $I_{DSS} = 100 \mu A$  (max) ( $V_{DS} = 450 V$ )
- Enhancement-model:  $V_{th} = 2.0$  to  $4.0 V$  ( $V_{DS} = 10 V, I_D = 1 mA$ )

## Maximum Ratings ( $T_a = 25^\circ C$ )

Characteristics		Symbol	Rating	Unit
Drain-source voltage		$V_{DSS}$	450	V
Drain-gate voltage ( $R_{GS} = 20 k\Omega$ )		$V_{DGR}$	450	V
Gate-source voltage		$V_{GSS}$	$\pm 30$	V
Drain current	DC (Note 1)	$I_D$	1	A
	Pulse (Note 1)	$I_{DP}$	2	A
Drain power dissipation		$P_D$	1.3	W
Single pulse avalanche energy (Note 2)		$E_{AS}$	122	mJ
Avalanche current		$I_{AR}$	1	A
Repetitive avalanche energy (Note 3)		$E_{AR}$	0.13	mJ
Channel temperature		$T_{ch}$	150	$^\circ C$
Storage temperature range		$T_{stg}$	-55 to 150	$^\circ C$



Weight: 0.54 g (typ.)

## Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	96.1	$^\circ C/W$

Note 1: Please use devices on condition that the channel temperature is below  $150^\circ C$ .

Note 2:  $V_{DD} = 90 V, T_{ch} = 25^\circ C$  (initial),  $L = 203 mH, R_G = 25 \Omega, I_{AR} = 1 A$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic sensitive device. Please handle with caution.

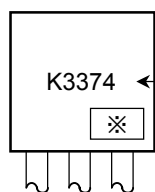
## Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		$I_{GSS}$	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	$\pm 10$	$\mu\text{A}$
Drain-source breakdown voltage		$V_{(BR)GSS}$	$I_G = \pm 10 \mu\text{A}, V_{DS} = 0 \text{ V}$	$\pm 30$	—	—	V
Drain cut-OFF current		$I_{DSS}$	$V_{DS} = 450 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	100	$\mu\text{A}$
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	450	—	—	V
Gate threshold voltage		$V_{th}$	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$	2.0	—	4.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = 10 \text{ V}, I_D = 0.5 \text{ A}$	—	3.7	4.6	$\Omega$
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10 \text{ V}, I_D = 0.5 \text{ A}$	0.3	0.7	—	S
Input capacitance		$C_{iss}$	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	180	—	pF
Reverse transfer capacitance		$C_{rss}$		—	2	—	
Output capacitance		$C_{oss}$		—	20	—	
Switching time	Rise time	$t_r$		—	7	—	ns
	Turn-ON time	$t_{on}$		—	15	—	
	Fall time	$t_f$		—	30	—	
	Turn-OFF time	$t_{off}$		—	70	—	
Total gate charge (gate-source plus gate-drain)		$Q_g$	$V_{DD} \approx 360 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 1 \text{ A}$	—	5	—	nC
Gate-source charge		$Q_{gs}$		—	3	—	
Gate-drain ("miller") charge		$Q_{gd}$		—	2	—	

## Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	$I_{DR}$	—	—	—	1	A
Pulse drain reverse current (Note 1)	$I_{DRP}$	—	—	—	2	A
Forward voltage (diode)	$V_{DSF}$	$I_{DR} = 1 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	-1.7	V
Reverse recovery time	$t_{rr}$	$I_{DR} = 1 \text{ A}, V_{GS} = 0 \text{ V},$	—	350	—	ns
Reverse recovery charge	$Q_{rr}$	$dI_{DR}/dt = 100 \text{ A}/\mu\text{s}$	—	1.3	—	nC

## Marking

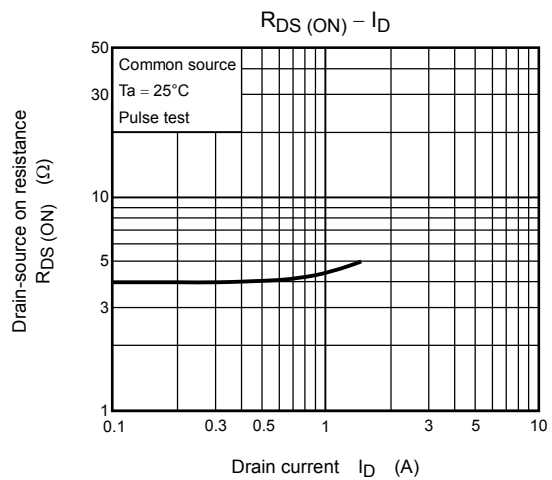
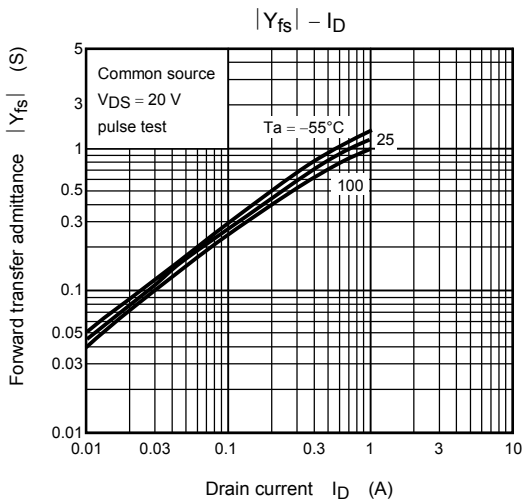
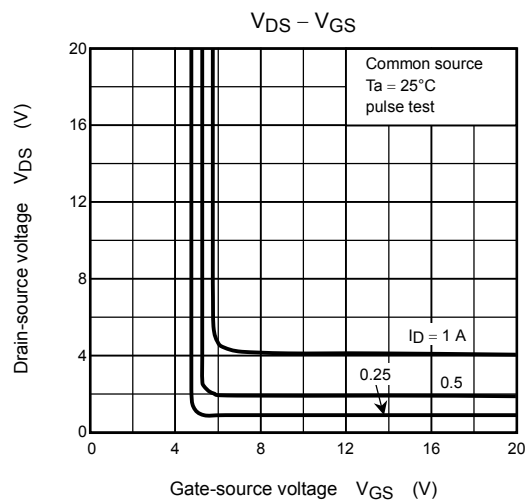
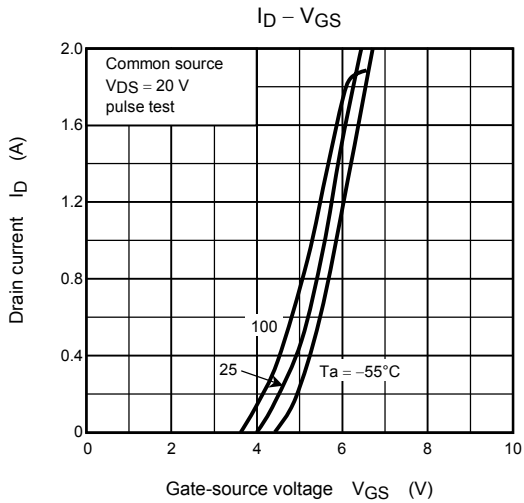
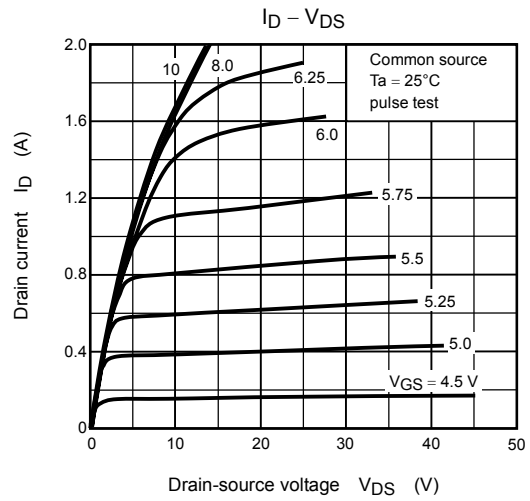
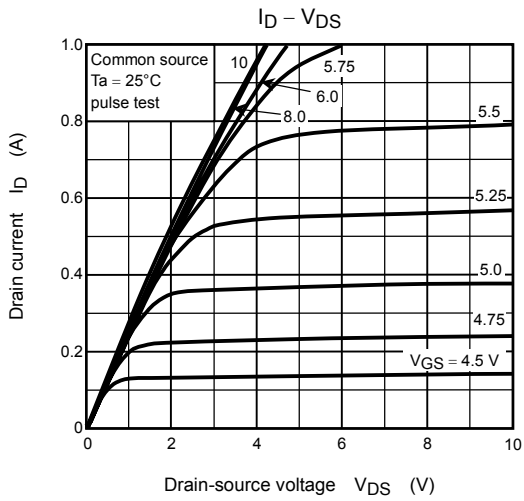


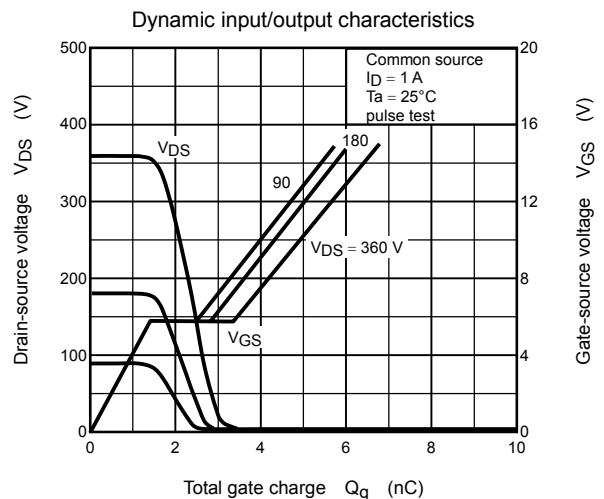
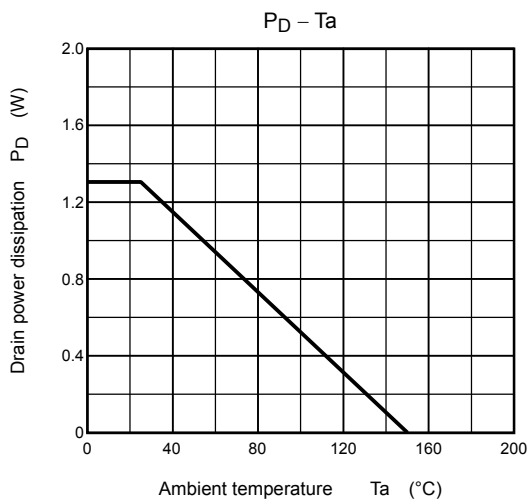
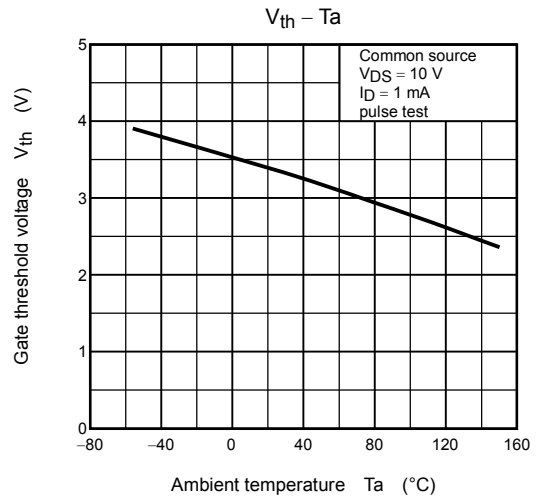
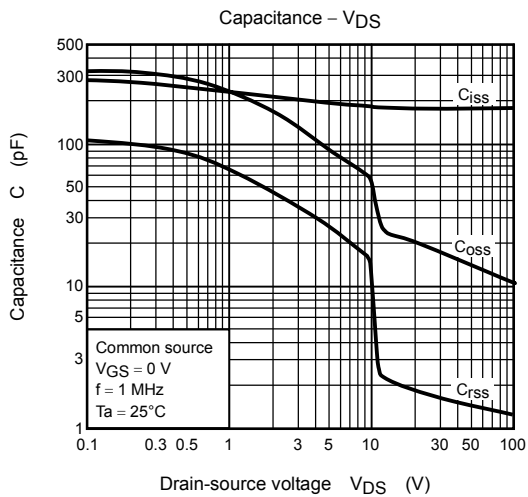
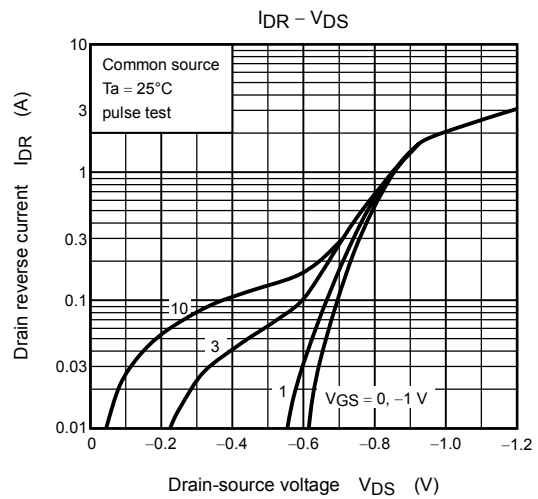
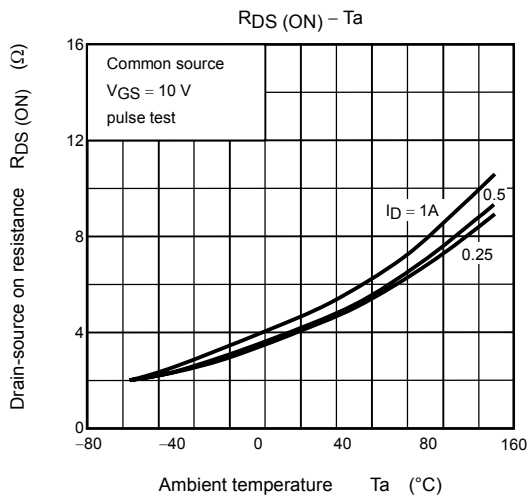
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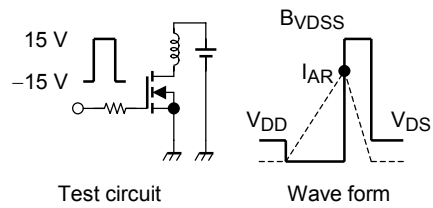
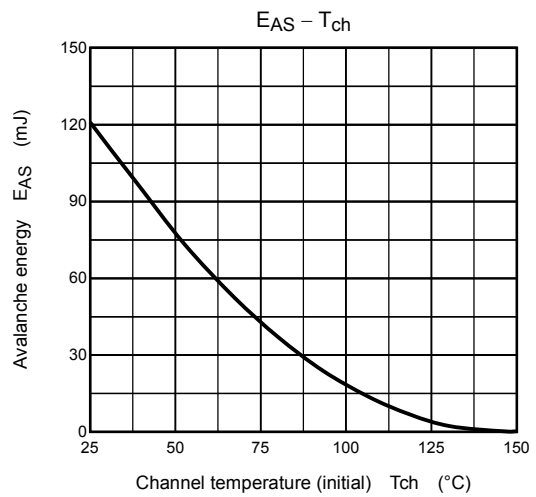
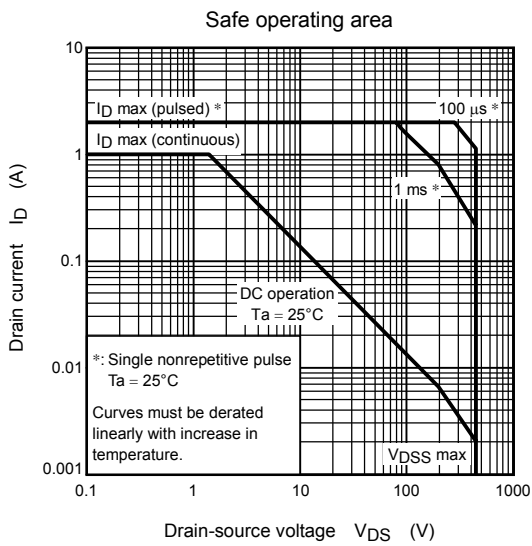
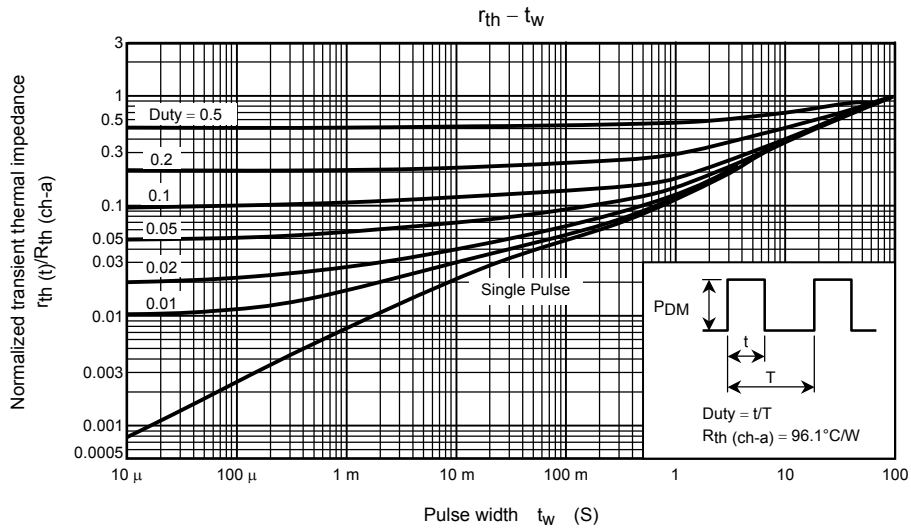
※ Lot Number

□ □ — Month (starting from alphabet A)

□ — Year (last number of the christian era)







$R_G = 25 \Omega$   
 $V_{DD} = 90 \text{ V}, L = 203 \text{ mH}$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left( \frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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