

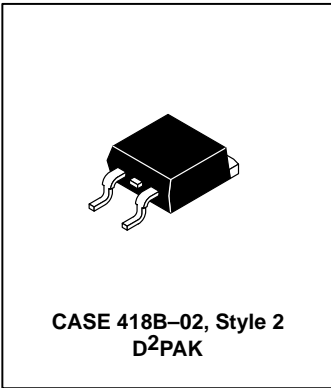
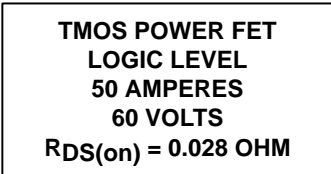
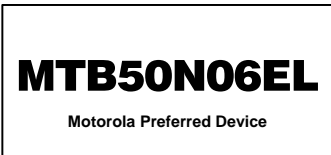
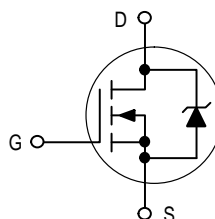
Advance Information

TMOS E-FET™

**Power Field Effect Transistors
D2PAK for Surface Mount
Logic Level TMOS (L2TMOS™)
N-Channel Enhancement-Mode Silicon Gate**

These TMOS Power FETs are designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers. This Logic Level Series part is specified to operate with level logic gate-to-source voltage of 5 volt and 4 volt.

- Silicon Gate for Fast Switching Speeds
- Low $R_{DS(on)}$ — 0.028 Ω max
- Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13-inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number



MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous	V_{GS}	± 15	Vdc
Drain Current — Continuous	I_D	50	Adc
— Continuous @ 100°C	I_D	28	
— Single Pulse ($t_p \leq 10 \mu\text{s}$)	I_{DM}	142	Apk
Total Power Dissipation	P_D	125	Watts
Derate above 25°C		1.0	W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$, when mounted with the minimum recommended pad size		2.5	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy — Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 25 \text{ Vdc}$, $V_{GS} = 5.0 \text{ Vpk}$, $I_L = 50 \text{ Apk}$, $L = 0.32 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	400	mJ
Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
— Junction to Ambient	$R_{\theta JA}$	62.5	
— Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JA}$	50	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Preferred devices are Motorola recommended choices for future use and best overall value.

MTB50N06EL

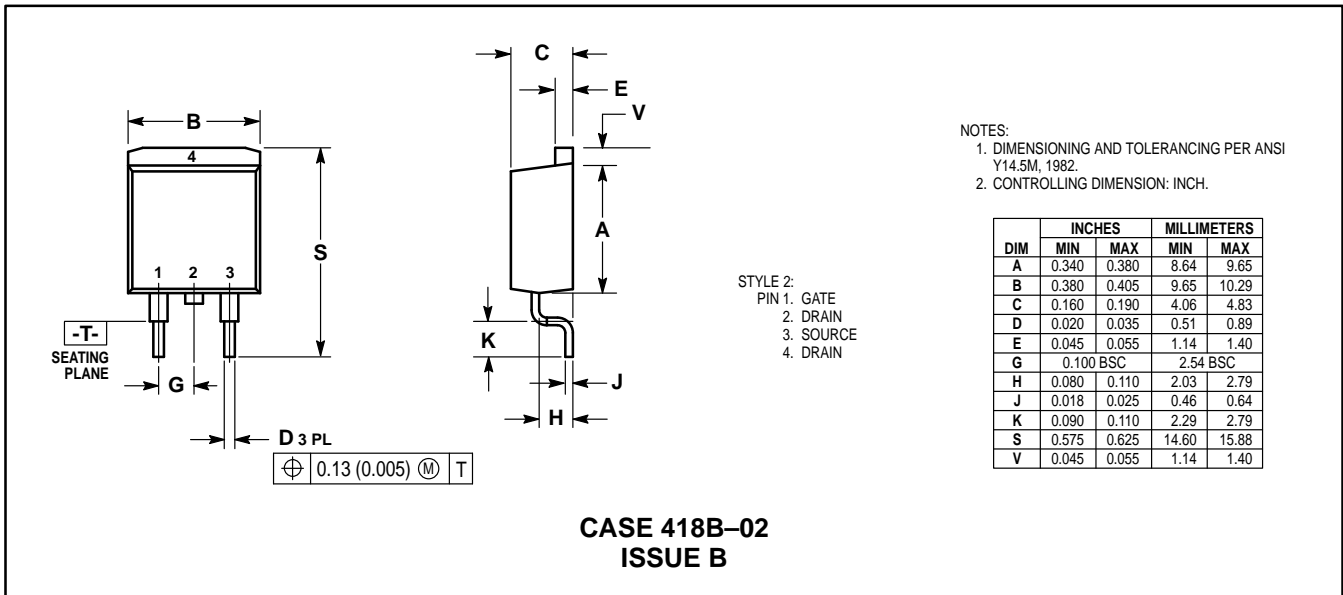
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)


Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V _{GS} = 0 V, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	60 —	— 64	— —	Vdc mV/°C	
Zero Gate Voltage Drain Current (V _{DS} = 60 Vdc, V _{GS} = 0) (V _{DS} = 60 Vdc, V _{GS} = 0, T _J = 125°C)	I _{DSS}	— —	— —	10 100	μAdc	
Gate–Body Leakage Current (V _{GS} = ±15 Vdc, V _{DS} = 0)	I _{GSS}	—	—	100	nAdc	
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc) Temperature Coefficient (Negative)	V _{GS(th)}	1.0 —	— 4.78	2.0 —	Vdc mV/°C	
Static Drain–Source On–Resistance (V _{GS} = 5.0 Vdc, I _D = 25 Adc) (V _{GS} = 4.0 Vdc, I _D = 25 Adc)	R _{DS(on)}	— —	— —	0.028 0.039	Ohm	
Drain–Source On–Voltage (V _{GS} = 5.0 Vdc) (I _D = 50 Adc) (I _D = 25 Adc, T _J = 125°C)	V _{DS(on)}	— —	— —	1.68 1.40	Vdc	
Forward Transconductance (V _{DS} = 15 Vdc, I _D = 25 Adc)	g _{FS}	17	—	—	mhos	
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0, f = 1.0 MHz)	C _{iss}	—	3100	4340	pF
Output Capacitance		C _{oss}	—	1065	1491	
Reverse Transfer Capacitance		C _{rss}	—	260	520	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V _{DD} = 25 Vdc, I _D = 50 Adc, V _{GS} = 5.0 Vdc, R _G = 9.1 Ω)	t _{d(on)}	—	21	42	ns
Rise Time		t _r	—	365	730	
Turn–Off Delay Time		t _{d(off)}	—	55	110	
Fall Time		t _f	—	150	300	
Gate Charge	(V _{DS} = 48 Vdc, I _D = 50 Adc, V _{GS} = 5.0 Vdc)	Q _T	—	52	73	nC
		Q ₁	—	13	—	
		Q ₂	—	34	—	
		Q ₃	—	27	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I _S = 50 Adc, V _{GS} = 0) (I _S = 50 Adc, V _{GS} = 0, T _J = °C)	V _{SD}	— —	1.52 1.1	2.5 —	Vdc
Reverse Recovery Time	(I _S = 50 Adc, V _{GS} = 0, dI _S /dt = 100 A/μs)	t _{rr}	—	200	—	ns
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the tab to center of die)	L _d	—	3.5	—	nH	
Internal Source Inductance (Measured from the source lead 0.1" from package to source bond pad)	L _s	—	7.5	—	nH	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS



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