ISO^2-CMOS MT91L60/61

3 Volt Multi-Featured Codec (MFC)

Data Sheet

March 2006

Features

- Single 2.7-3.6 volt supply operation
- MT91L61 version features a delayed framing pulse in SSI and ST-BUS modes to facilitate cascaded devices
- Programmable μ-Law/A-Law Codec and Filters
- Programmable ITU-T (G.711)/sign-magnitude coding
- Programmable transmit, receive and side-tone gains
- Fully differential interface to handset transducers - including 300 ohm receiver driver
- Flexible digital interface including ST-BUS/SSI
- Serial microport
- Low power operation
- ITU-T G.714 compliant
- Multiple power down modes

Ordering Information

MT91L61AE	24 Pin PDIP	Tubes
MT91L60AE	24 Pin PDIP	Tubes
MT91L61AS	24 Pin SOIC	Tubes
MT91L60AS	20 Pin SOIC	Tubes
MT91L61AN	24 Pin SSOP	Tubes
MT91L60AN	20 Pin SSOP	Tubes
MT91L60ASR	20 Pin SOIC	Tape & Reel
MT91L61ASR	24 Pin SOIC	Tape & Reel
MT91L61ASR1	24 Pin SOIC*	Tape & Reel
MT9160AN1	20 Pin SSOP*	Tubes

*Pb Free Matte Tin

-40°C to +85°C

Applications

- Battery operated equipment
- Digital telephone sets
- Cellular radio sets
- Local area communications stations
- Pair Gain Systems
- Line cards

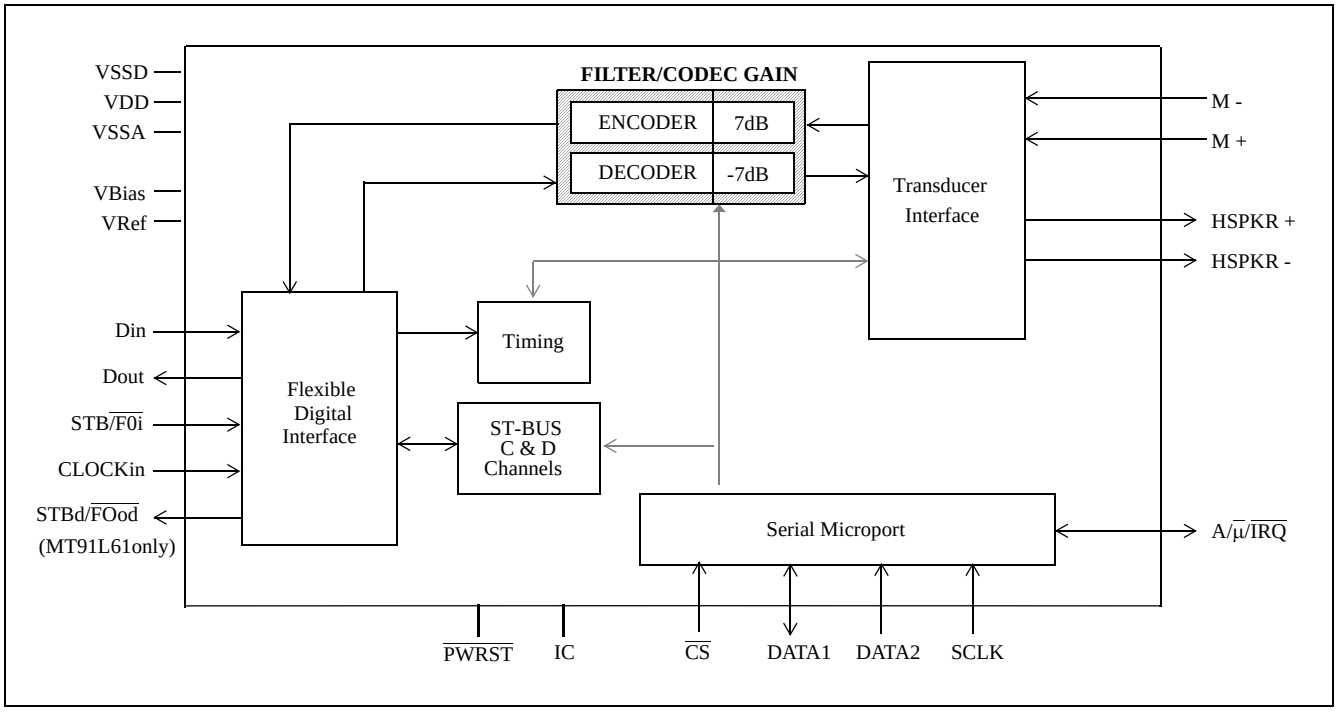


Figure 1 - Functional Block Diagram

Description

The MT91L60/61 3 V Multi-featured Codec incorporates a built-in Filter/Codec, gain control and programmable sidetone path as well as on-chip anti-alias filters, reference voltage and bias source. The device supports both ITU-T and sign- magnitude A-Law and μ-Law requirements. The MT91L60/61 is a true 3 V device employing a fully differential architecture to ensure wide dynamic range.

Complete telephony interfaces are provided for connection to handset transducers. Internal register access is provided through a serial microport compatible with various industry standard micro-controllers.

The MT91L60/61 is fabricated in Zarlink's ISO^2-CMOS technology ensuring low power consumption and high reliability.

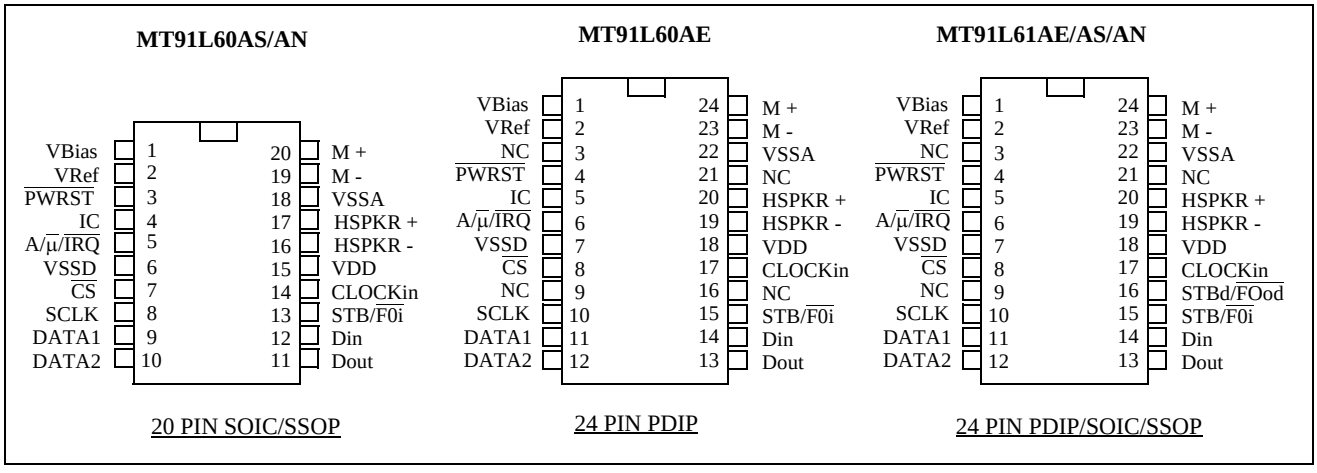


Figure 2 - Pin Connections

Pin Description

Pin # 20 Pin	Pin # 24 Pin	Name	Description
1	1	V_{Bias}	**Bias Voltage (Output).** (V_{DD}/2) volts is available at this pin for biasing external amplifiers. Connect 0.1 μF capacitor to V_{SSA}.
2	2	V_{Ref}	**Reference Voltage for Codec (Output).** Used internally. Nominally [Vdd/2 - 1.1] volts. Connect 0.1 μF capacitor to V_{SSA}.
3	4	PWRST	**Power-up Reset (Input).** CMOS compatible input with Schmitt Trigger (active low).
4	5	IC	**Internal Connection.** Tie externally to V_{SSD} for normal operation.
5	6	A/$\overline{\mu}$/$\overline{IRQ}$	**A/$\overline{\mu}$** - When internal control bit DEn = 0 this CMOS level compatible input pin governs the companding law used by the filter/Codec; μ-Law when tied to V_{SSD} and A-Law when tied to V_{DD}. Logically OR'ed with A/$\overline{\mu}$ register bit. **$\overline{IRQ}$** - When internal control bit DEn = 1 this pin becomes an open-drain interrupt output signalling valid access to the D-Channel registers in ST-BUS mode.
6	7	V_{SSD}	**Digital Ground.** Nominally 0 volts.
7	8	CS	**Chip Select (Input).** This input signal is used to select the device for microport data transfers. Active low. CMOS level compatible.
8	10	SCLK	**Serial Port Synchronous Clock (Input).** Data clock for microport. CMOS level compatible.
9	11	DATA 1	**Bidirectional Serial Data.** Port for microprocessor serial data transfer. In Motorola/National mode of operation, this pin becomes the data transmit pin only and data receive is performed on the DATA 2 pin. Input CMOS level compatible.
10	12	DATA 2	**Serial Data Receive.** In Motorola/National mode of operation, this pin is used for data receive. In Intel mode, serial data transmit and receive are performed on the DATA 1 pin and DATA 2 is disconnected. Input CMOS level compatible.
11	13	D_{out}	**Data Output.** A high impedance three-state digital output for 8 bit wide channel data being sent to the Layer 1 transceiver. Data is shifted out via this pin concurrent with the rising edge of the bit clock during the timeslot defined by STB, or according to standard ST-BUS timing.

Pin Description (continued)

Pin # 20 Pin	Pin # 24 Pin	Name	Description
12	14	D_{in}	**Data Input.** A digital input for 8 bit wide channel data received from the Layer 1 transceiver. Data is sampled on the falling edge of the bit clock during the timeslot defined by STB, or according to standard ST-BUS timing. Input level is CMOS compatible.
13	15	STB/$\overline{F0i}$	**Data Strobe/Frame Pulse (Input).** For SSI mode this input determines the 8 bit timeslot used by the device for both transmit and receive data. This active high signal has a repetition rate of 8 kHz. Standard frame pulse definitions apply in ST-BUS mode. CMOS level compatible input.
	16	STBd/$\overline{F0od}$ (MT91L61 only)	**Delayed Frame Pulse Output**. In SSI mode, an 8 bit wide strobe is output after the first strobe goes low. In ST-BUS mode, a frame pulse is output after 4 channel timeslots.
14	17	CLOCKin	**Clock (Input).** The clock provided to this input pin is used for the internal device functions. For SSI mode connect the bit clock to this pin when it is 512 kHz or greater. Connect a 4096 kHz clock to this input when the available bit clock is 128 kHz or 256 kHz. For ST-BUS mode connect $\overline{C4i}$ to this pin. CMOS level compatible.
15	18	V_{DD}	**Positive Power Supply (Input).** Nominally 3 volts.
16	19	HSPKR-	**Inverting Handset Speaker (Output).** Output to the handset speaker (balanced).
17	20	HSPKR+	**Non-Inverting Handset Speaker (Output).** Output to the handset speaker (balanced).
18	22	V_{SSA}	**Analog Ground (Input).** Nominally 0 volts.
19	23	M-	**Inverting Microphone (Input).** Inverting input to microphone amplifier from the handset microphone.
20	24	M+	**Non-Inverting Microphone (Input).** Non-inverting input to microphone amplifier from the handset microphone.
	3,9, 16,21	NC	**No Connect**. (24 Packages only). Pin 16 is NC for MT91L60.

Overview

The 3 V Multi-featured Codec (MFC) features complete Analog/Digital and Digital/Analog conversion of audio signals (Filter/Codec) and an analog interface to a standard handset transmitter and receiver (Transducer Interface). The receiver amplifier is capable of driving a 300 ohm load.

Each of the programmable parameters within the functional blocks is accessed through a serial microcontroller port compatible with Intel MCS-51®, Motorola SPI® and National Semiconductor Microwire® specifications. These parameters include: gain control, power down, mute, B-Channel select (ST-BUS mode), C&D channel control/access, law control, digital interface programming and loopback. Optionally the device may be used in a controllerless mode utilizing the power-on default settings.

Functional Description

Filter/Codec

The Filter/Codec block implements conversion of the analog 0-3.3 kHz speech signals to/from the digital domain compatible with 64 kb/s PCM B-Channels. Selection of companding curves and digital code assignment are programmable. These are ITU-T G.711 A-law or μ-Law, with true-sign/Alternate Digit Inversion or true-sign/Inverted Magnitude coding, respectively. Optionally, sign-magnitude coding may also be selected for proprietary applications.

The Filter/Codec block also implements transmit and receive audio path gains in the analog domain. A programmable gain, voice side-tone path is also included to provide proportional transmit speech feedback to the handset receiver. This side tone path feature is disabled by default. Figure 3 depicts the nominal half-channel and side-tone gains for the MT91L60/61.

In the event of $\overline{\text{PWRST}}$, the MT91L60/61 defaults such that the side-tone path is off, all programmable gains are set to 0dB and ITU-T μ-Law is selected. Further, the digital port is set to SSI mode operation at 2048 kb/s and the FDI and driver sections are powered up. (See Microport section.)

The internal architecture is fully differential to provide the best possible noise rejection as well as to allow a wide dynamic range from a single 3 volt supply design. This fully differential architecture is continued into the Transducer Interface section to provide full chip realization of these capabilities for the handset functions.

A reference voltage (V_{Ref}), for the conversion requirements of the Codec section, and a bias voltage (V_{Bias}), for biasing the internal analog sections, are both generated on-chip. V_{Bias} is also brought to an external pin so that it may be used for biasing external gain setting amplifiers. A 0.1μF capacitor must be connected from V_{Bias} to analog ground at all times. Although V_{Ref} may only be used internally, a 0.1μF capacitor must be connected from V_{Ref} to ground. The analog ground reference point for these two capacitors must be physically the same point. To facilitate this the V_{Ref} and V_{Bias} pins are situated on adjacent pins.

The transmit filter is designed to meet ITU-T G.714 specifications. The nominal gain for this filter is 0 dB (gain control = 0 dB). Gain control allows the output signal to be increased up to 7 dB. An anti-aliasing filter is included. This is a second order lowpass implementation with a corner frequency at 25 kHz.

The receive filter is designed to meet ITU-T G.714 specifications. The nominal gain for this filter is 0 dB (gain control = 0 dB). Gain control allows the output signal to be attenuated up to 7 dB. Filter response is peaked to compensate for the sinx/x attenuation caused by the 8 kHz sampling rate.

Side-tone is derived from the input of the Tx filter and is not subject to the gain control of the Tx filter section. Side-tone is summed into the receive handset transducer driver path after the Rx filter gain control section so that Rx gain adjustment will not affect side-tone levels. The side-tone path may be enabled/disabled with the gain control bits located in Gain Control Register 2 (address 01h).

Transmit and receive filter gains are controlled by the $TxFG_0$-$TxFG_2$ and $RxFG_0$-$RxFG_2$ control bits, respectively. These are located in Gain Control Register 1 (address 00h). Transmit filter gain is adjustable from 0dB to +7dB and receive filter gain from 0dB to -7dB, both in 1dB increments.

Side-tone filter gain is controlled by the STG_0-STG_2 control bits located in Gain Control Register 2 (address 01h). Side-tone gain is adjustable from -9.96 dB to +9.96 dB in 3.32 dB increments.

Companding law selection for the Filter/Codec is provided by the A/$\overline{\mu}$ companding control bit while the coding scheme is controlled by the Smag/$\overline{\text{ITU-T}}$ control bit. The A/$\overline{\mu}$ control bit is logically OR'ed with the A/$\overline{\mu}$ pin providing access in both controller and controllerless modes. Both A/$\overline{\mu}$ and Smag/$\overline{\text{ITU-T}}$ reside in Control Register 2 (address 04h). Table 1 illustrates these choices.

Code	Sign/ Magnitude	ITU-T (G.711)	
		μ-Law	A-Law
+ Full Scale	1111 1111	1000 0000	1010 1010
+ Zero	1000 0000	1111 1111	1101 0101
-Zero (quiet code)	0000 0000	0111 1111	0101 0101
- Full Scale	0111 1111	0000 0000	0010 1010

Table 1

Transducer Interfaces

Standard handset transducer interfaces are provided by the MT91L60/61. These are:

- The handset microphone inputs (transmitter), pins M+/M-. The nominal transmit path gain may be adjusted to either 6.0 dB or 15.3 dB. Control of this gain is provided by the TxINC control bit (Gain Control register 1, address 00h).
- The handset speaker outputs (receiver), pins HSPKR+/HSPKR-. This internally compensated fully differential output driver is capable of driving the load shown in Figure 3. The nominal receive path gain may be adjusted to either 0 dB, -6 dB or -12 dB. Control of this gain is provided by the RxINC control bit (Gain Control register 1, address 00h). This gain adjustment is in addition to the programmable gain provided by the receive filter.

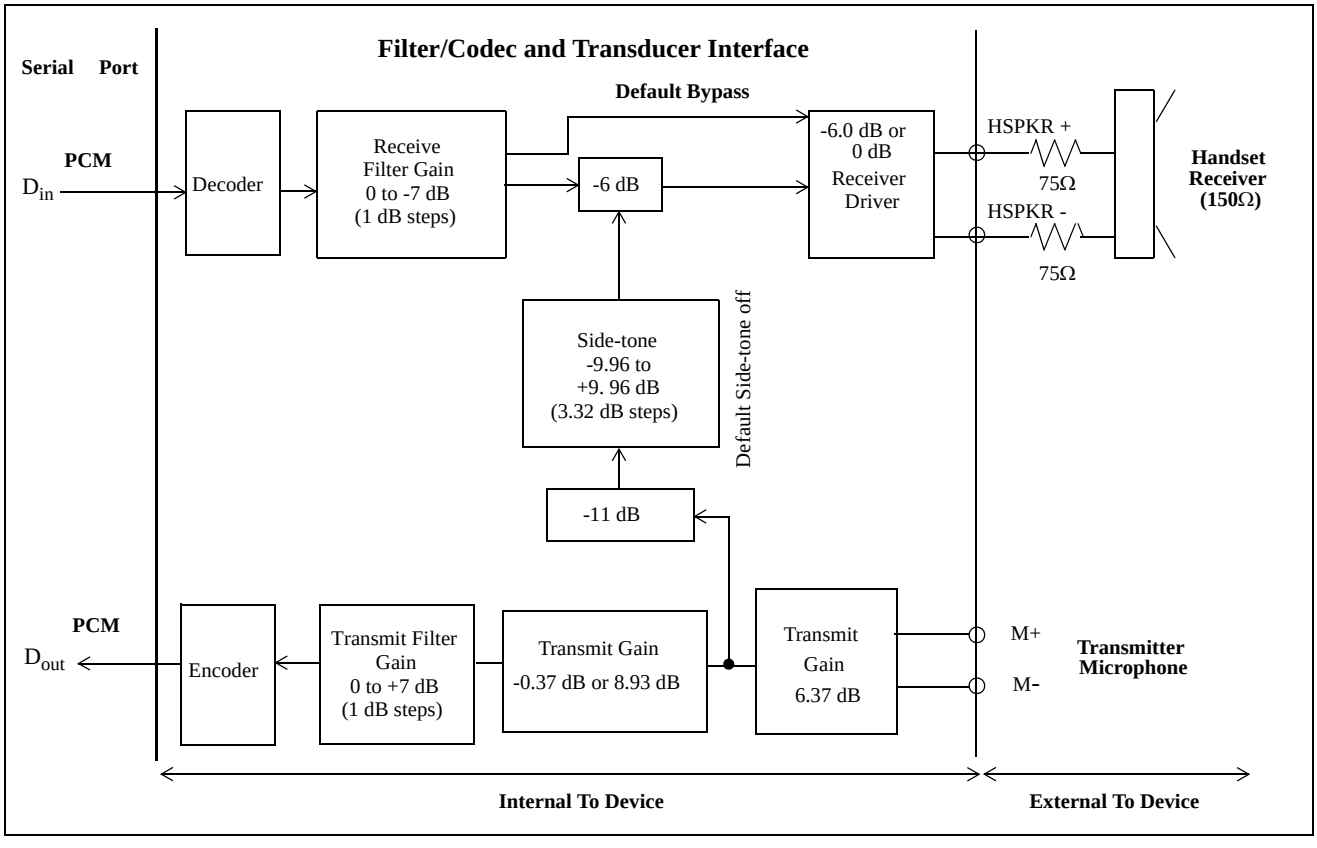


Figure 3 - Audio Gain Partitioning

Microport

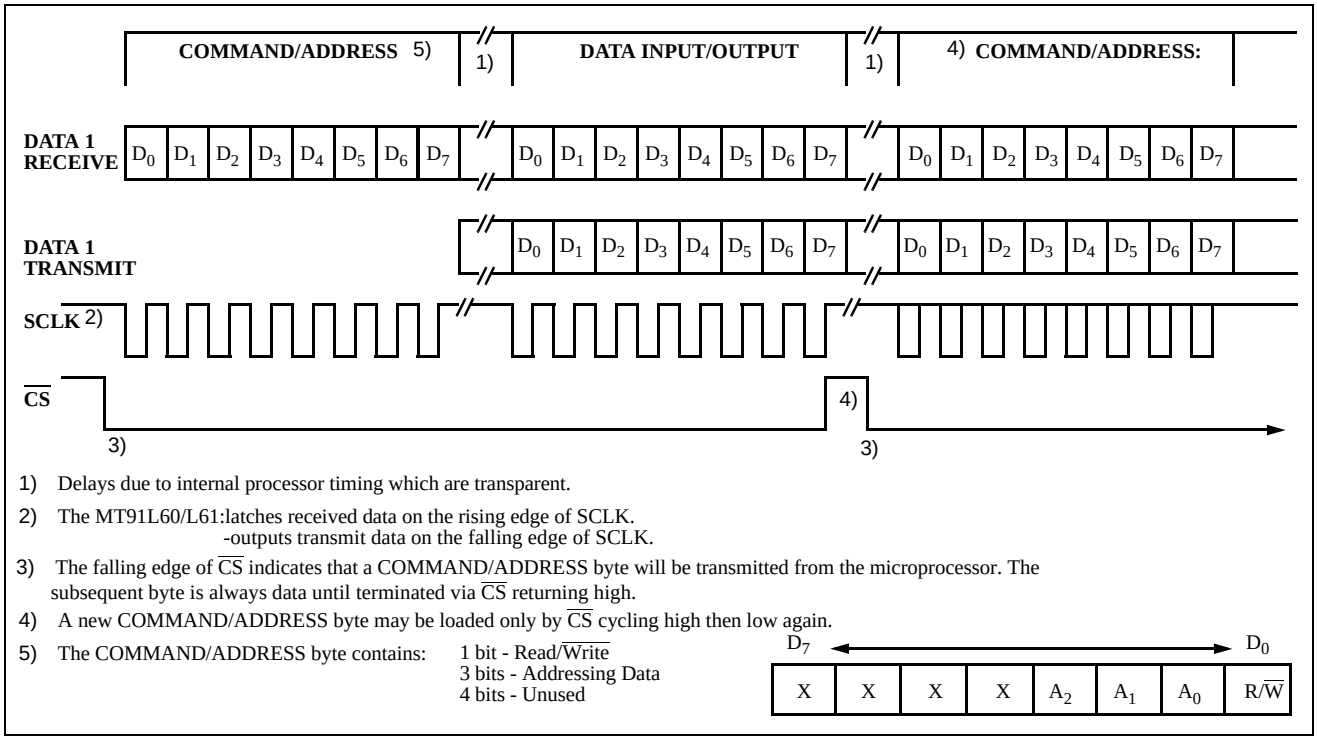
The serial microport, compatible with Intel MCS-51 (mode 0), Motorola SPI (CPOL=0,CPHA=0) and National Semiconductor Microwire specifications provides access to all MT91L60/61 internal read and write registers. This microport consists of a transmit/receive data pin (DATA1), a receive data pin (DATA2), a chip select pin ($\overline{CS}$) and a synchronous data clock pin (SCLK). For D-channel contention control, in ST-BUS mode, this interface provides an open-drain interrupt output ($\overline{IRQ}$).

The microport dynamically senses the state of the serial clock (SCLK) each time chip select becomes active. The device then automatically adjusts its internal timing and pin configuration to conform to Intel or Motorola/National requirements. If SCLK is high during chip select activation then Intel mode 0 timing is assumed. The DATA1 pin is defined as a bi-directional (transmit/receive) serial port and DATA2 is internally disconnected. If SCLK is low during chip select activation then Motorola/National timing is assumed. Motorola processor mode CPOL=0, CPHA=0 must be used. DATA1 is defined as the data transmit pin while DATA2 becomes the data receive pin. Although the dual port Motorola controller configuration usually supports full-duplex communication, only half-duplex communication is possible in the MT91L60/61. The micro must discard non-valid data which it clocks in during a valid write transfer to the MT91L60/61. During a valid read transfer from the MT91L60/61 data simultaneously clocked out by the micro is ignored by the MT91L60/61.

All data transfers through the microport are two-byte transfers requiring the transmission of a Command/Address byte followed by the data byte written or read from the addressed register. $\overline{CS}$ must remain asserted for the duration of this two-byte transfer. As shown in Figures 5 and 6 the falling edge of $\overline{CS}$ indicates to the MT91L60/61 that a microport transfer is about to begin. The first 8 clock cycles of SCLK after the falling edge of $\overline{CS}$ are always used to receive the Command/Address byte from the microcontroller. The Command/Address byte contains information detailing whether the second byte transfer will be a read or a write operation and at what address. The next 8 clock cycles are used to transfer the data byte between the MT91L60/61 and the microcontroller. At the end of the two-byte transfer $\overline{CS}$ is brought high again to terminate the session. The rising edge of $\overline{CS}$ will tri-state the output driver of DATA1 which will remain tri-stated as long as $\overline{CS}$ is high.

Intel processors utilize least significant bit first transmission while Motorola/National processors employ most significant bit first transmission. The MT91L60/61 microport automatically accommodates these two schemes for normal data bytes. However, to ensure decoding of the R/$\overline{W}$ and address information, the Command/Address byte is defined differently for Intel operation than it is for Motorola/National operation. Refer to the relative timing diagrams of Figures 5 and 6.

Receive data is sampled on the rising edge of SCLK while transmit data is made available concurrent with the falling edge of SCLK.



1) Delays due to internal processor timing which are transparent.

2) The MT91L60/L61:latches received data on the rising edge of SCLK.
-outputs transmit data on the falling edge of SCLK.

3) The falling edge of $\overline{CS}$ indicates that a COMMAND/ADDRESS byte will be transmitted from the microprocessor. The subsequent byte is always data until terminated via $\overline{CS}$ returning high.

4) A new COMMAND/ADDRESS byte may be loaded only by $\overline{CS}$ cycling high then low again.

5) The COMMAND/ADDRESS byte contains: 1 bit - Read/$\overline{Write}$
3 bits - Addressing Data
4 bits - Unused

Figure 4 - Audio Gain Partitioning

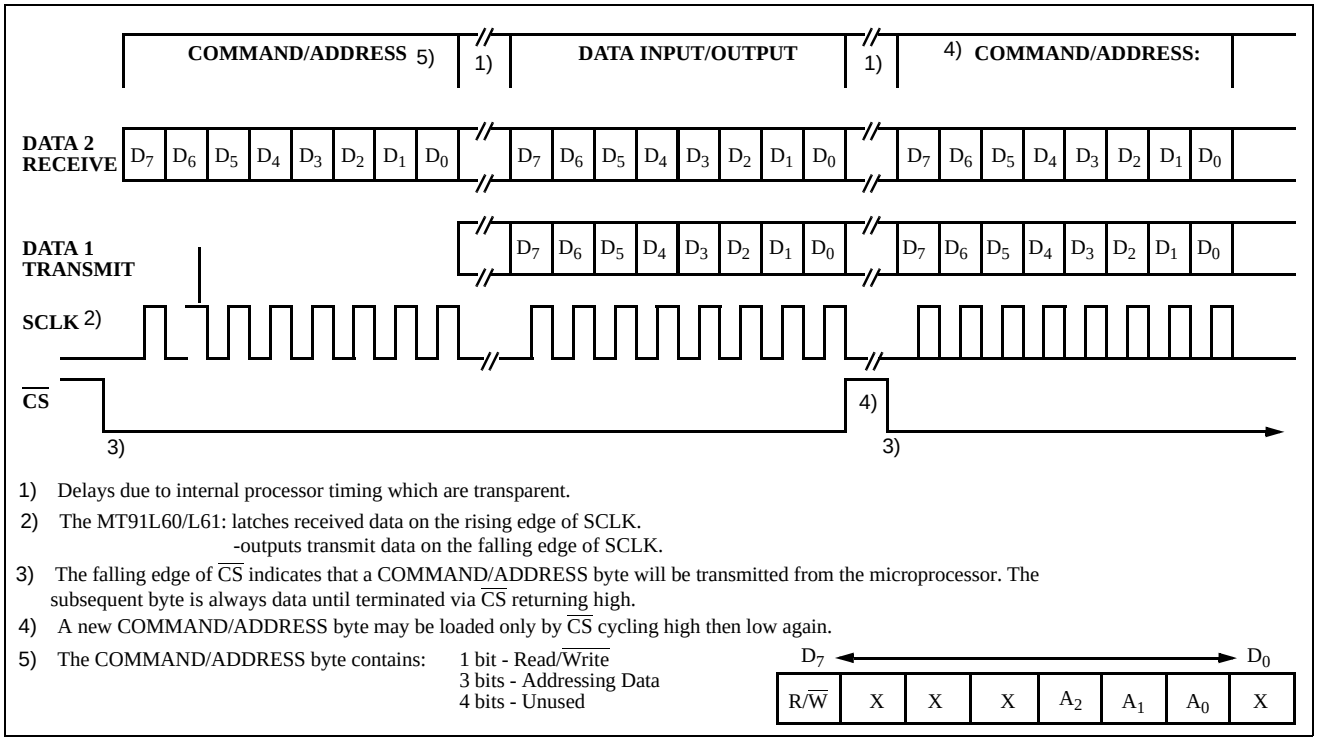


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Figure 5 - Serial Port Relative Timing for Motorola Mode 00/National Microwire

Flexible Digital Interface

A serial link is required to transport data between the MT91L60/61 and an external digital transmission device. The MT91L60/61 utilizes the ST-BUS architecture defined by Zarlink Semiconductor but also supports a strobed data interface found on many standard Codec devices. This interface is commonly referred to as Simple Serial Interface (SSI). The combination of ST-BUS and SSI provides a Flexible Digital Interface (FDI) capable of supporting all Zarlink basic rate transmission devices as well as many other 2B+D transceivers.

The required mode of operation is selected via the CSL2-0 control bits (Control Register 2, address 04h). Pin definitions alter dependent upon the operational mode selected, as described in the following subsections as well as in the Pin Description tables.

Quiet Code

The FDI can be made to send quiet code to the decoder and receive filter path by setting the RxMute bit high. Likewise, the FDI will send quiet code in the transmit path when the TxMute bit is high. Both of these control bits reside in Control Register 1 at address 03h. When either of these bits are low their respective paths function normally. The -Zero entry of Table 1 is used for the quiet code definition.

ST-BUS Mode

The ST-BUS consists of output (DSTo) and input (DSTi) serial data streams, in FDI these are named Dout and Din respectively, a synchronous clock input signal CLOCKin ($\overline{C4i}$), and a framing pulse input ($\overline{F0i}$). These signals are direct connections to the corresponding pins of Zarlink basic rate devices. The CSL2, CSL1 and CSL0 bits are set to 1 for ST-BUS operation.

The data streams operate at 2048 kb/s and are Time Division Multiplexed into 32 identical channels of 64 kb/s bandwidth. A frame pulse (a 244 nSec low going pulse) is used to separate the continuous serial data streams into the 32 channel TDM frames. Each frame has a 125 μSecond period translating into an 8 kHz frame rate. A valid frame begins when $\overline{F0i}$ is logic low coincident with a falling edge of $\overline{C4i}$. Refer to Figure 11 for detailed ST-BUS timing. $\overline{C4i}$ has a frequency (4096 kHz) which is twice the data rate. This clock is used to sample the data at the 3/4 bit-cell position on DSTi and to make data available on DSTo at the start of the bit-cell. $\overline{C4i}$ is also used to clock the MT91L60/61 internal functions (i.e., Filter/Codec, Digital gain and tone generation) and to provide the channel timing requirements.

The MT91L60/61 uses only the first four channels of the 32 channel frame. These channels are always defined, beginning with Channel 0 after the frame pulse, as shown in Figure 6 (ST-BUS channel assignments). The MT91L60/61 provides a delayed frame pulse ($\overline{F0od}$), 4 channels after the input frame pulse.

The first two (D & C) Channels are enabled for use by the DEN and CEN bits respectively, (Control Register 2, address 04h). ISDN basic rate service (2B+D) defines a 16 kb/s signalling (D) Channel. The MT91L60/61 supports transparent access to this signalling channel. ST-BUS basic rate transmission devices, which may not employ a microport, provide access to their internal control/status registers through the ST-BUS Control (C) Channel. The MT91L60/61 supports microport access to this C-Channel.

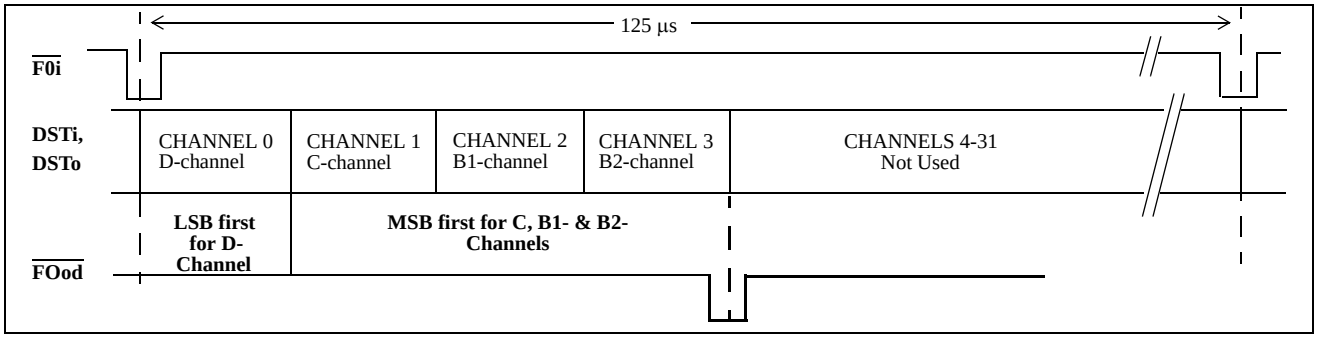


Figure 6 - ST-BUS Channel Assignment

DEN - D-Channel

In ST-BUS mode access to the D-Channel (transmit and receive) data is provided through an 8-bit read/write register (address 06h). D-Channel data is accumulated in, or transmitted from this register at the rate of 2 bits/frame for 16 kb/s operation (1 bit/frame for 8 kb/s operation). Since the ST-BUS is asynchronous, with respect to the microport, valid access to this register is controlled through the use of an interrupt ($\overline{IRQ}$) output. D-Channel access is enabled via the (DEn) bit.

DEN:

When 1, ST-BUS D-channel data (1 or 2 bits/frame depending on the state of the D8 bit) is shifted into/out of the D-channel (READ/WRITE) register.

When 0, the receive D-channel data (READ) is still shifted into the proper register while the DSTo D-channel timeslot and $\overline{IRQ}$ outputs are tri-stated (default).

D8:

When 1, D-Channel data is shifted at the rate of 1 bit/frame (8 kb/s).

When 0, D-Channel data is shifted at the rate of 2 bits/frame (16 kb/s default).

16 kb/s D-Channel operation is the default mode which allows the microprocessor access to a full byte of D-Channel information every fourth ST-BUS frame. By arbitrarily assigning ST-BUS frame n as the reference frame, during which the microprocessor D-Channel read and write operations are performed, then:

a. A microport read of address 04 hex will result in a byte of data being extracted which is composed of four I-bits (designated by roman numerals I,II,III,IV). These di-bits are composed of the two D-Channel bits received during each of frames n, n-1, n-2 and n-3. Referring to Fig. 7a: di-bit I is mapped from frame n-3, di-bit II is mapped from frame n-2, di-bit III is mapped from frame n-1 and di-bit IV is mapped from frame n.

The D-Channel read register is not preset to any particular value on power-up ($\overline{PWRST}$) or software reset (RST).

b. A microport write to Address 04 hex will result in a byte of data being loaded which is composed of four di-bits (designated by roman numerals I, II, III, IV). These di-bits are destined for the two D-Channel bits transmitted during each of frames n+1, n+2, n+3, n+4. Referring to Fig. 7a: di-bit I is mapped to frame n+1, di-bit II is mapped to frame n+2, di bit III is mapped to frame n+3 and di bit IV is mapped to frame n+4.

If no new data is written to address 04 hex, the current D-channel register contents will be continuously re-transmitted. The D-Channel write register is preset to all ones on power-up ($\overline{PWRST}$) or software reset (RST).

An interrupt output is provided ($\overline{IRQ}$) to synchronize microprocessor access to the D-Channel register during valid ST-BUS periods only. $\overline{IRQ}$ will occur every fourth (eighth in 8 kb/s mode) ST-BUS frame at the beginning of the third (second in 8 kb/s mode) ST-BUS bit cell period. The interrupt will be removed following a microprocessor Read or Write of Address 04 hex or upon encountering the following frames $\overline{F0i}$ input, whichever occurs first. To ensure D-Channel data integrity, microport read/write access to Address 04 hex must occur before the following frame pulse. See Figure 7b for timing.

8 kb/s operation expands the interrupt to every eight frames and processes data one-bit-per-frame. D-Channel register data is mapped according to Figure 7c.

CEn - C-Channel

Channel 1 conveys the control/status information for the Layer 1 transceiver. C-Channel data is transferred MSB first on the ST-BUS by the MT91L60/61. The full 64 kb/s bandwidth is available and is assigned according to which transceiver is being used. Consult the data sheet for the selected transceiver for its C-Channel bit definitions and order of bit transfer.

When CEN is high, data written to the C-Channel register (address 05h) is transmitted, most significant bit first, on DSTo. On power-up reset ($\overline{PWRST}$) or software reset (Rst, address 03h) all C-Channel bits default to logic high. Receive C-Channel data (DSTi) is always routed to the read register regardless of this control bit's logic state.

When low, data transmission is halted and this timeslot is tri-stated on DSTo.

B1-Channel and B2-Channel

Channels 2 and 3 are the B1 and B2 channels, respectively. B-channel PCM associated with the Filter/Codec and transducer audio paths is selected on an independent basis for the transmit and receive paths. TxBSel and RxBSel (Control Register 1, address 03h) are used for this purpose.

If no valid transmit path has been selected then the timeslot output on DSTo is tri-stated (see PDFDI and PDDR control bits, Control Register 1 address 03h).

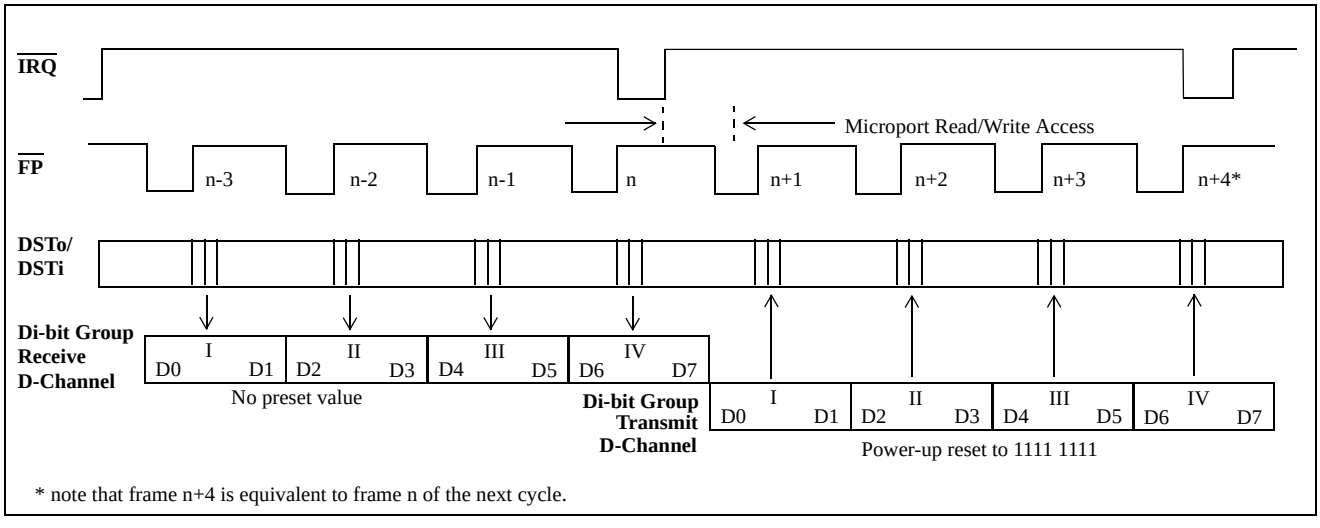


Figure 7a - D-Channel 16 kb/s Operation

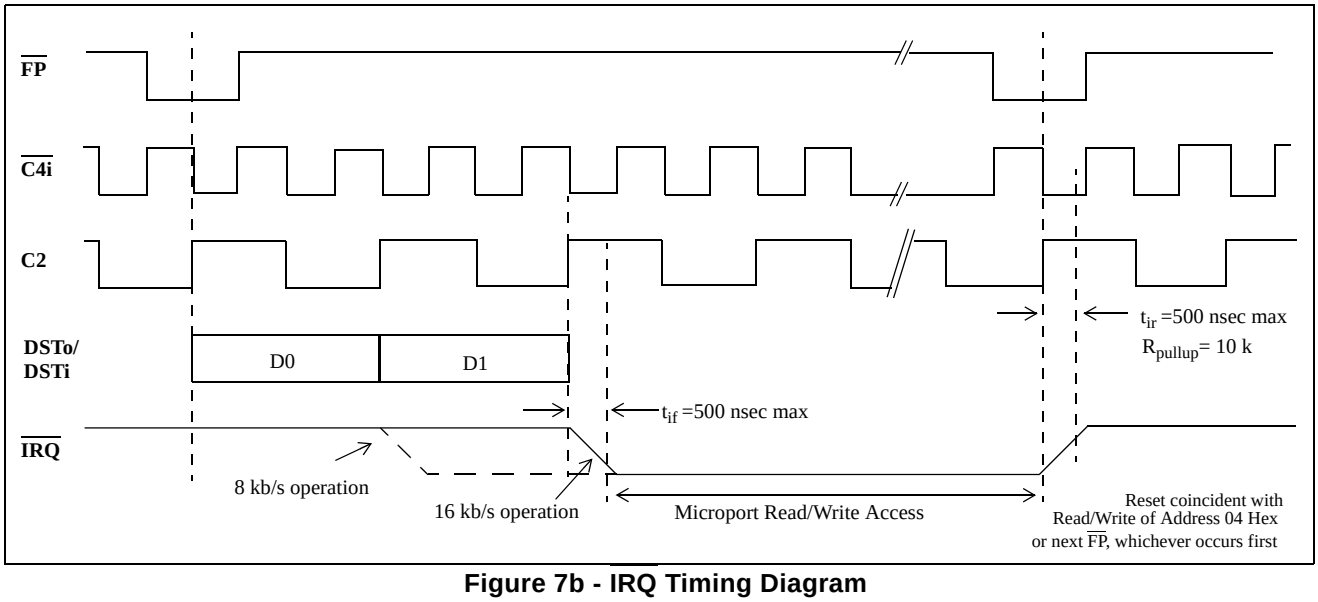


Figure 7b - IRQ Timing Diagram

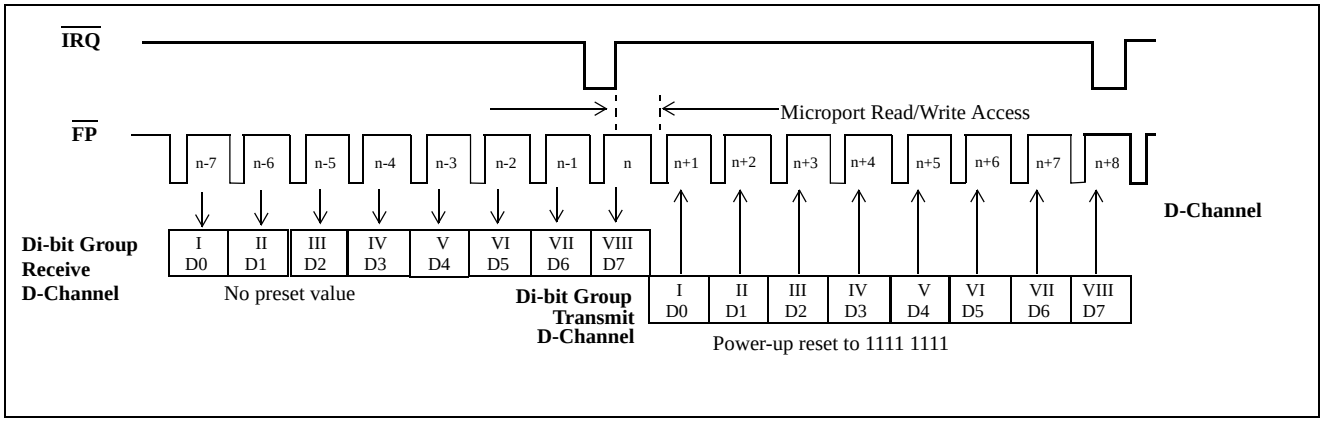


Figure 7c - D-Channel 8 kb/s Operation

SSI Mode

The SSI BUS consists of input and output serial data streams named Din and Dout respectively, a Clock input signal (CLOCKin), and a framing strobe input (STB). The frame strobe must be synchronous with, and eight cycles of, the bit clock. A 4.096 MHz master clock is also required for SSI operation if the bit clock is less than 512 kHz. The timing requirements for SSI are shown in Figures 12 & 13.

In SSI mode the MT91L60/61 supports only B-Channel operation. The internal C and D Channel registers used in ST-BUS mode are not functional for SSI operation. The control bits TxBSel and RxBSel, as described in the ST-BUS section, are ignored since the B-Channel timeslot is defined by the input STB strobe. Hence, in SSI mode transmit and receive B-Channel data are always in the channel defined by the STB input.

The data strobe input STB determines the 8-bit timeslot used by the device for both transmit and receive data. This is an active high signal with an 8 kHz repetition rate. The MT91L61 provides a delayed strobe pulse which occurs after the initial strobe goes low and is held high for the duration of 8 pcm bits.

SSI operation is separated into two categories based upon the data rate of the available bit clock. If the bit clock is 512 kHz or greater then it is used directly by the internal MT91L60/61 functions allowing synchronous operation. If the available bit clock is 128 kHz or 256 kHz, then a 4096 kHz master clock is required to derive clocks for the internal MT91L60/61 functions.

Applications where Bit Clock (BCL) is below 512 kHz are designated as asynchronous. The MT91L60/61 will re-align its internal clocks to allow operation when the external master and bit clocks are asynchronous. Control bits CSL2, CSL1 and CSL0 in Control Register 2 (address 04h) are used to program the bit rates.

For synchronous operation data is sampled, from Din, on the falling edge of BCL during the time slot defined by the STB input. Data is made available, on Dout, on the rising edge of BCL during the time slot defined by the STB input. Dout is tri-stated at all times when STB is not true. If STB is valid and PDDR is set, then quiet code will be transmitted on Dout during the valid strobe period. There is no frame delay through the FDI circuit for synchronous operation.

For asynchronous operation Dout and Din are as defined for synchronous operation except that the allowed output jitter on Dout is larger. This is due to the resynchronization circuitry activity and will not affect operation since the bit cell period at 128 kb/s and 256 kb/s is relatively large. There is a one frame delay through the FDI circuit for asynchronous operation. Refer to the specifications of Figures 12 & 13 for both synchronous and asynchronous SSI timing.

$\overline{\text{PWRST}}$/Software Reset (Rst)

While the MT91L60/61 is held in $\overline{\text{PWRST}}$ no device control or functionality is possible. While in software reset (Rst=1, address 03h) only the microport is functional. Software reset can only be removed by writing the Rst bit low or by performing a hardware $\overline{\text{PWRST}}$. While the Rst bit is high, the other bits in Control Register 1 are held low and cannot be reprogrammed. Therefore to modify Control Register 1 the Rst bit must first be written low, followed by a 2nd write operation which writes the desired data. This avoids a race condition between clearing the reset bit and the writing of the other bits in Control Register 1.

After a Power-up reset ($\overline{\text{PWRST}}$) or software reset (Rst) all control bits assume their "Power Reset Value" default states; μ-Law coding, 0 dB Rx and 6dB Tx gains and the device powered up in SSI mode 2048 kb/s operation with Dout tri-stated while there is no strobe active on STB. If a valid strobe is supplied to STB, then Dout will be active, during the defined channel.

To attain complete power-down from a normal operating condition, write PDFDI = 1 and PDDR = 1 (Control Register 1, address 03h) or set the $\overline{\text{PWRST}}$ pin low.

00	RxINC	$RxFG_2$	$RxFG_1$	$RxFG_0$	TxINC	$TxFG_2$	$TxFG_1$	$TxFG_0$	Gain Control Register 1
01	-	-	-	-	-	STG_2	STG_1	STG_0	Gain Control Register 2
02	-	-	-	-	-	-	-	DrGain	Path Control
03	PDFDI	PDDR	RST	-	T_xMute	R_xMute	T_xBsel	R_xBsel	Control Register 1
04	CEN	DEN	D8	A/μ	Smag/ $\overline{\text{ITU-T}}$	CSL_2	CSL_1	CSL_0	Control Register 2
05	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	C-Channel Register
06	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D-Channel Register
07	-	-	-	-	$\overline{\text{PCM}}$/ ANALOG	loopen	-	-	Loop Back

Table 2 - 3V Multi-featured Codec Register Map

Note: Bits marked "-" are reserved bits and should be written with logic "0"

Applications

Figure 8 shows an application in a wireless phone set. Figure 9 shows an MT9161B's delayed frame pulse driving a second MT9161B. This configuration would be used where multiple CODEC's were using a data bus (an example being Zarlink's ST-BUS).

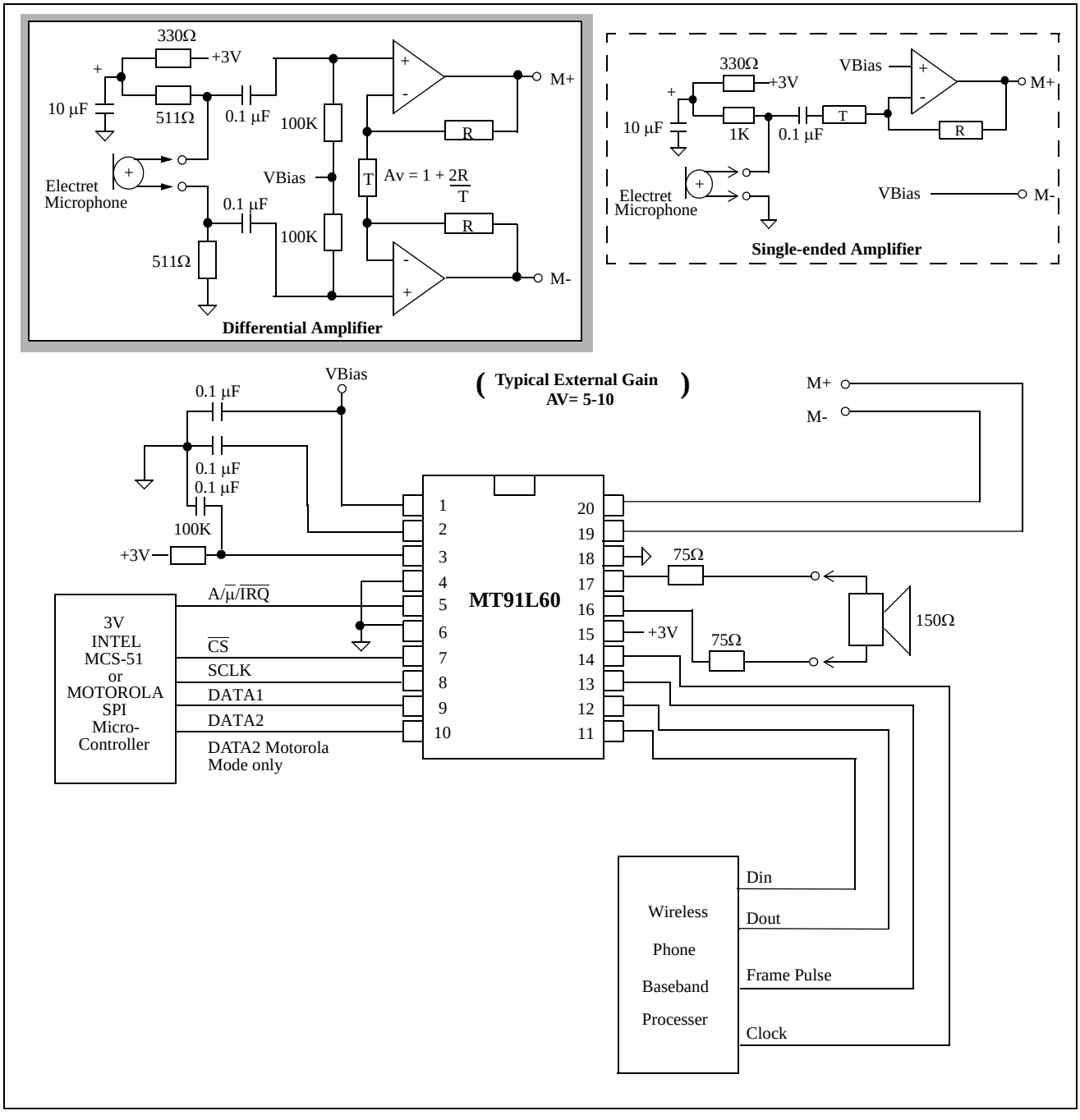


Figure 8 - Wireless Phone Set

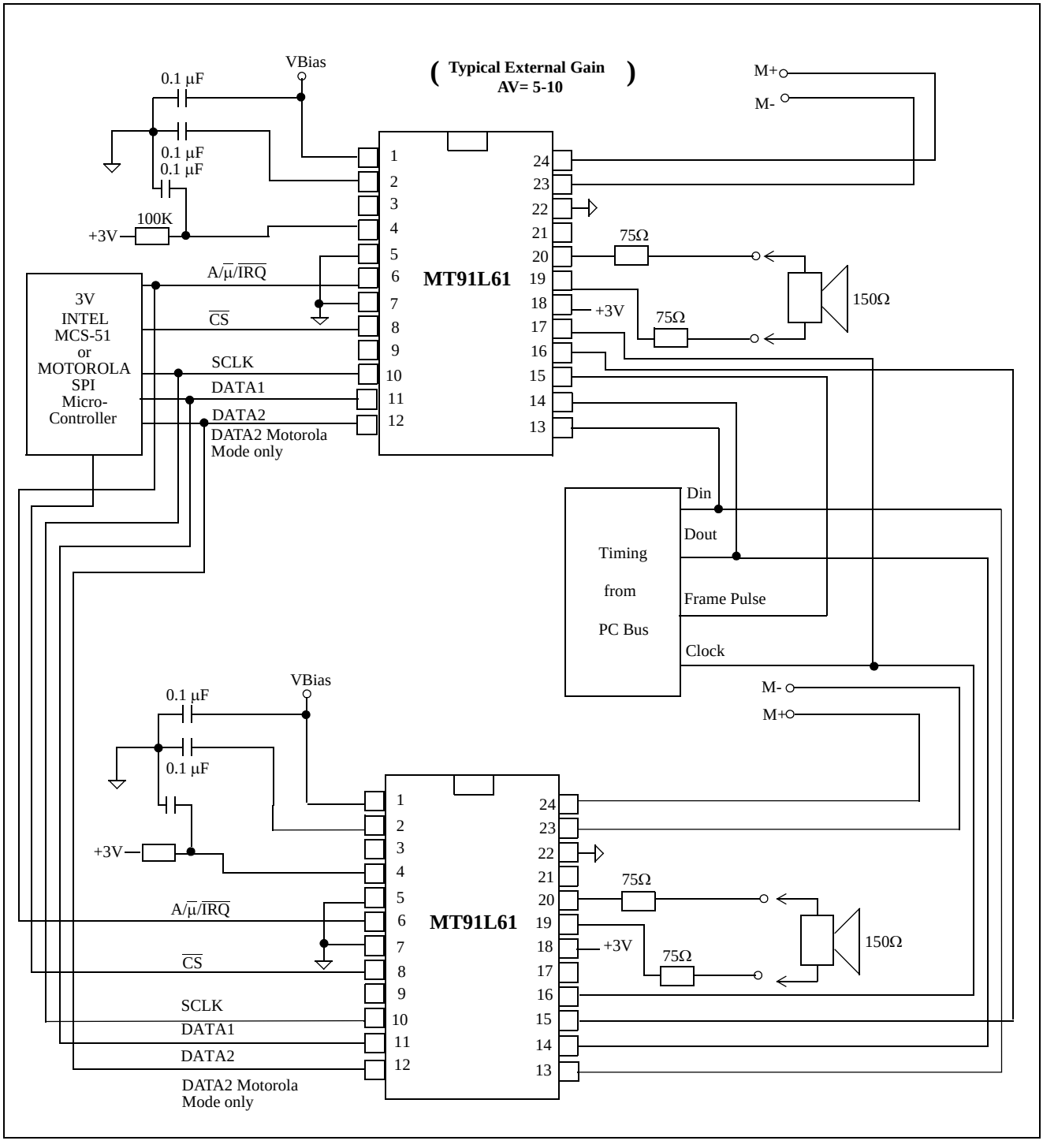


Figure 9 - Delayed Frame Pulse of First MT91L61 Signalling Second MT91L61

Register Summary

Gain Control Register 1 ADDRESS = 00h WRITE/READ VERIFY

Power Reset Value
1000 0000

RxINC	$RxFG_2$	$RxFG_1$	$RxFG_0$	TxINC	$TxFG_2$	$TxFG_1$	$TxFG_0$
7	6	5	4	3	2	1	0

Receive Gain Setting (dB)	$RxFG_2$	$RxFG_1$	$RxFG_0$
(default) 0	0	0	0
-1	0	0	1
-2	0	1	0
-3	0	1	1
-4	1	0	0
-5	1	0	1
-6	1	1	0
-7	1	1	1

$RxFG_n$ = Receive Filter Gain bit n

Transmit Gain Setting (dB)	$TxFG_2$	$TxFG_1$	$TxFG_0$
(default) 0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

$TxFG_n$ = Transmit Filter Gain bit n

RxINC: When high, the receive path nominal gain is set to 0 dB. When low, this gain is -6.0 dB.
TxINC: When high, the transmit path nominal gain is set to 15.3 dB. When low, this gain is 6.0 dB.

Gain Control Register 2 ADDRESS = 01h WRITE/READ VERIFY

Power Reset Value
XXXX X000

-	-	-	-	-	STG_2	STG_1	STG_0
7	6	5	4	3	2	1	0

Side-tone Gain Setting (dB)	STG_2	STG_1	STG_0
(default) OFF	0	0	0
-9.96	0	0	1
-6.64	0	1	0
-3.32	0	1	1
0	1	0	0
3.32	1	0	1
6.64	1	1	0
9.96	1	1	1

STG_n = Side-tone Gain bit n

Note: Bits marked "-" are reserved bits and should be written with logic "0"

Path Control

ADDRESS = 02h WRITE/READ VERIFY

Power Reset Value
XX00 0000

-	-	-	-	-	-	-	DrGain
7	6	5	4	3	2	1	0

DrGain — When high, the receive path is summed with the side tone path and is attenuated by 6dB. When low, the receive path contains no side tone (default).

Control Register 1

ADDRESS = 03h WRITE/READ VERIFY

Power Reset Value
0000 0000

PDFDI	PDDR	Rst	–	TxMute	RxMute	TxBsel	RxBsel
7	6	5	4	3	2	1	0

PDFDI — When high, the FDI PLA and the Filter/Codec are powered down (default). When low, the FDI is active.

PDDR — When high, the ear driver and Filter/Codec are powered down (default). In addition, in ST-BUS mode, the selected output channel is tri-stated. In SSI mode the PCM output code will be -zero code during the valid strobe period. The output will be tri-stated outside of the valid strobe and for the whole frame if no strobe is supplied. When low, the driver and Filter/Codec are active if PDFDI is low.

Rst — When high, a software reset occurs performing the same function as the hardware reset ($\overline{PWRST}$) except that the Rst bit remains high and device remains powered up. A software reset can be removed only by writing this bit low or by means of a hardware reset ($\overline{PWRST}$). This bit is useful for quickly programming the Registers to the default Power Reset Values. When this bit is low, the reset condition is removed allowing the registers to be modified

TxMute — When high the transmit PCM stream is interrupted and replaced with quiet code; thus forcing the output code into a mute state (only the output code is muted, the transmit microphone and transmit Filter/Codec are still functional). When low the full transmit path functions normally (default).

RxMute — When high the received PCM stream is interrupted and replaced with quiet code; thus forcing the receive path into a mute state. When low the full receive path functions normally (default).

TxBsel — When high, the transmit B2 channel is functional in ST-BUS mode. When low, the transmit B1 channel is functional in ST-BUS mode. Not used in SSI mode.

RxBsel — When high, the receive B2 channel is functional in ST-BUS mode. When low, the receive B1 channel is functional in ST-BUS

Note: Bits marked "-" are reserved bits and should be written with logic "0"

Control Register 2 ADDRESS = 04h WRITE/READ VERIFY

CEn	DEn	D8	A/$\overline{\mu}$	Smag/$\overline{\text{ITU-T}}$	CSL_2	CSL_1	CSL_0
7	6	5	4	3	2	1	0

Power Reset Value
0000 0010

CEn — When high, data written into the C-Channel register (address 05h) is transmitted during channel 1 on DSTo. When low, the channel 1 timeslot is tri-stated on DSTo. Channel 1 data received on DSTi is read via the C-Channel register (address 05h) regardless of the state of CEn. This control bit has significance only for ST-BUS operation and is ignored for SSI operation.

DEn — When high, data written into the D-Channel Register (address 06h) is transmitted (2 bits/frame) during channel 0 on DSTo. The remaining six bits of the D-Channel carry no information. When low, the channel 0 timeslot is completely tri-stated on DSTo. Channel 0 data received on DSTi is read via the D-Channel register regardless of the state of DEN. This control bit has significance only for ST-BUS mode and is ignored for SSI operation.

D8 — When high, D-channel operates at 8 kb/s. When low, D-channel operates at 16 kb/s (default).

A/$\overline{\mu}$ — When high, A-Law encoding/decoding is selected for the MT91L60/61. When low, μ-Law encoding/decoding is selected.

Smag/$\overline{\text{ITU-T}}$ — When high, sign-magnitude code assignment is selected for the Codec input/output. When low, ITU-T code assignment is selected for the Codec input/output; true sign, inverted magnitude (μ-Law) or true sign, alternate digit inversion (A-Law).

CSL_2	CSL_1	CSL_0	Bit Clock rate (kHz)	CLOCKin (kHz)	Mode
1	1	1	N/A	4096	ST-BUS
1	0	0	128	4096	SSI
1	0	1	256	4096	SSI
0	0	0	512	512	SSI
0	0	1	1536	1536	SSI
0	1	0	2048	2048	SSI (default)
0	1	1	4096	4096	SSI

Note: Bits marked "-" are reserved bits and should be written with logic "0"

C-Channel Register ADDRESS = 05h WRITE/READ

C7	C6	C5	C4	C3	C2	C1	C0
7	6	5	4	3	2	1	0

Power Reset Value
1111 1111- write
XXXX XXXX - read

Micro-port access to the ST-BUS C-Channel information read and write

D-Channel Register ADDRESS = 06h WRITE/READ

D7	D6	D5	D4	D3	D2	D1	D0
7	6	5	4	3	2	1	0

Power Reset Value
1111 1111- write
XXXX XXXX - read

D7-D0 Data written to this register will be transmitted every frame, in channel 0, if the DEn control bit is set (address 04h). Received D-Channel data is valid, regardless of the state of DEn. These bits are valid for ST-BUS mode only and are accessible only when $\overline{IRQ}$ indicates valid access.

Loopback Register ADDRESS = 07h WRITE/READ VERIFY

-	-	-	-	PCM/ ANALOG	loopen	-	-
7	6	5	4	3	2	1	0

Power Reset Value
XXXX 0000

PCM/$\overline{ANALOG}$ This control bit functions only when loopen is set high. It is ignored when loopen is low.

For loopback operation when this bit is high, the device is configured for digital-to-digital loopback operation. Data on Din is looped back to Dout without conversion to the analog domain. However, the receive D/A path (from Din to HSPKR ±) still functions. When low, the device is configured for analog-to-analog operation. An analog input signal at M± is looped back to the SPKR± outputs through the A/D and D/A circuits as well as through the normal transmit A/D path (from M± to Dout).

loopen When high, loopback operation is enabled and the loopback type is governed by the state of the PCM/$\overline{ANALOG}$ bit. When low, loopbacks are disabled, the device operates normally and the PCM/$\overline{ANALOG}$ bit is ignored.

Note: Bits marked "-" are reserved bits and should be written with logic "0"

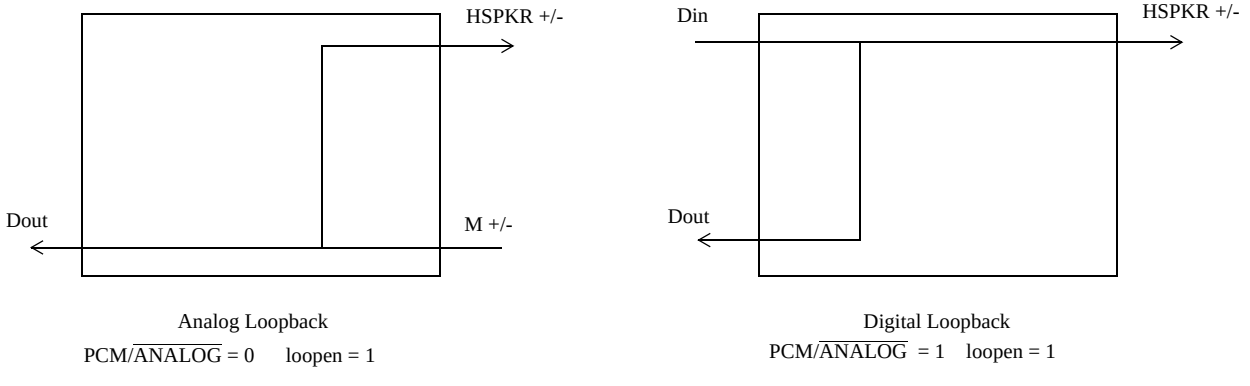


Figure 10 - Loopback Signal Flow

Absolute Maximum Ratings†

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	V_{DD} - V_{SS}	- 0.3	5	V
2	Voltage on any I/O pin	V_I/V_O	V_{SS} - 0.3	V_{DD} + 0.3	V
3	Current on any I/O pin (transducers excluded)	I_I/I_O		± 20	mA
4	Storage Temperature	T_S	- 65	+ 150	°C
5	Power Dissipation (package)	P_D		750	mW

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{SS} unless otherwise stated

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Supply Voltage	V_{DD}	2.7	3	3.6	V	
2	CMOS Input Voltage (high)	V_{IHC}	0.9*V_{DD}		V_{DD}	V	
3	CMOS Input Voltage (low)	V_{ILC}	V_{SS}		0.1*V_{DD}	V	
4	Operating Temperature	T_A	- 40		+ 85	°C	

Power Characteristics

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Static Supply Current (clock disabled, all functions off, PDFDI/PDDR=1, PWRST=0)	I_{DDC1}		2	20	µA	Outputs unloaded, Input signals static, not loaded
2	Dynamic Supply Current: Total all functions enabled	I_{DDFT}		6	10	mA	See Note 1.

Note 1: Power delivered to the load is in addition to the bias current requirements.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Input HIGH Voltage CMOS inputs	V_{IHC}	0.7*Vdd			V	
2	Input LOW Voltage CMOS inputs	V_{ILC}			0.3*Vdd	V	
3	VBias Voltage Output	V_{Bias}		$V_{DD}/2$		V	Max. Load = 20kΩ
4	VRef Voltage Output	V_{Ref}		$V_{DD}/2$-1.1		V	No Load
5	Input Leakage Current	I_{IZ}		0.1	10	mA	$V_{IN}=V_{DD}$ to V_{SS}
6	Positive Going Threshold Voltage ($\overline{PWRST}$ only) Negative Going Threshold Voltage ($\overline{PWRST}$ only) Hysteresis	V_{T+} V_{T-}	2.2	 0.65	 0.7	V V V	Vdd = 3V
7	Output HIGH Current	I_{OH}	1.0			mA	$V_{OH} = 0.9*V_{DD}$ See Note 1
8	Output LOW Current	I_{OL}	2.5			mA	$V_{OL} = 0.1*V_{DD}$ See Note 1
9	Output Leakage Current	I_{OZ}		0.01	10	mA	$V_{OUT} = V_{DD}$ and V_{SS}
10	Output Capacitance	C_o		15		pF	
11	Input Capacitance	C_i		10		pF	

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

* Note 1 - Magnitude measurement, ignore signs.

Clockin Tolerance Characteristics† **(ST-BUS Mode)**

	Characteristics	Min.	Typ.‡	Max.	Units	Test Conditions
1	$\overline{C4i}$ Frequency	4095.6	4096	4096.4	kHz	(i.e., 100 ppm)

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

AC Characteristics† for A/D (Transmit) Path - **0 dBm0 = $A_{Lo3.17}$ - 3.17 dB** = **1.027 V_{rms}** for μ-Law and **0 dBm0 = $A_{Lo3.14}$ - 3.14 dB** =**1.067 V_{rms}** for A-Law, at the Codec. (V_{Ref} = 0.4 V and V_{Bias}=1.5 volts.)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Analog input equivalent to overload decision	$A_{Li3.17}$ $A_{Li3.14}$		4.246 4.4		Vp-p Vp-p	μ-Law A-Law Both at Codec
2	Absolute half-channel gain M ± to Dout	 G_{AX1} G_{AX2}	 5.4 14.7	 6.0 15.3	 6.6 15.9	 dB dB	Transmit filter gain=0 dB setting. TxINC = 0* TxINC = 1* @1020 Hz
	Tolerance at all other transmit filter settings (1 to 7 dB)		-0.2	±0.1	+0.2	dB	
3	Gain tracking vs. input level ITU-T G.714 Method 2	G_{TX}	-0.3 -0.6 -1.6		0.3 0.6 1.6	dB dB dB	3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0
4	Signal to total Distortion vs. input level. ITU-T G.714 Method 2	D_{QX}	35 29 24			dB dB dB	0 to -30 dBm0 -40 dBm0 -45 dBm0
5	Transmit Idle Channel Noise	N_{CX} N_{PX}		13 -70.5	16 -69	dBrnC0 dBm0p	μ-Law A-Law
6	Gain relative to gain at 1020 Hz <50 Hz 60 Hz 200 Hz 300 - 3000 Hz 3000-3300 Hz 3300 Hz 3400 Hz 4000 Hz 4600 Hz >4600 Hz	G_{RX}	 -0.25 -0.9 -0.9 -1.2	 -45 -0.2 -0.6 -23 -41	 -25 -30 0.0 0.25 0.25 0.25 0.25 -12.5 -25 -25	 dB dB dB dB dB dB dB dB dB dB	
7	Absolute Delay	D_{AX}		360		ms	at frequency of minimum delay
8	Group Delay relative to D_{AX}	D_{DX}		750 380 130 750		ms ms ms ms	500-600 Hz 600 - 1000 Hz 1000 - 2600 Hz 2600 - 2800 Hz
9	Power Supply Rejection f=1020 Hz	 PSSR	 30	 50		 dB	±100 mV peak signal on V_{DD} μ-law

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.
* Note: TxINC, refer to Control Register 1, address 00h.

AC Characteristics† for D/A (Receive) Path - 0 dBm0 = $A_{Lo3.17}$ - 3.17 dB = 1.027 V_{rms} for μ-Law and **0 dBm0 = $A_{Lo3.14}$ - 3.14 dB =1.067 V_{rms}** for A-Law, at the Codec. (V_{Ref} = 0.4 V and V_{Bias}=1.5 volts.)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Analog output at the Codec full scale	$A_{Lo3.17}$ $A_{Lo3.14}$		4.183 4.331		Vp-p Vp-p	μ-Law A-Law
2	Absolute half-channel gain. Din to HSPKR±	G_{AR1} G_{AR2} G_{AR3} G_{AR4}	-0.6 -6.6 -6.6 -12.6	0 -6 -6 -12	0.6 -5.4 -5.4 -11.4	dB dB dB dB	DrGain=0, RxINC =1* DrGain=0, RxINC =0* DrGain=1, RxINC =1* DrGain=1, RxINC =0* @ 1020 Hz
	Tolerance at all other receive filter settings (-1 to -7 dB)		-0.2	±0.1	+0.2	dB	
3	Gain tracking vs. input level ITU-T G.714 Method 2	G_{TR}	-0.3 -0.6 -1.6		0.3 0.6 1.6	dB dB dB	3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0
4	Signal to total distortion vs. input level. ITU-T G.714 Method 2	G_{QR}	35 29 24			dB dB dB	0 to -30 dBm0 -40 dBm0 -45 dBm0
5	Receive Idle Channel Noise	N_{CR} N_{PR}		11.5 -80	14 -77	dBrnC0 dBm0p	μ-Law A-Law
6	Gain relative to gain at 1020 Hz 200 Hz 300 - 3000 Hz 3000 - 3300 Hz 3300 Hz 3400 Hz 4000 Hz 4600 Hz >4600 Hz	G_{RR}	 -0.25 -0.90 -0.9 -0.9	 -0.1 -0.5 -23 -41	 0.25 0.25 0.25 0.25 0.25 -12.5 -25 -25	 dB dB dB dB dB dB dB dB	
7	Absolute Delay	D_{AR}		240		ms	at frequency of min. delay
8	Group Delay relative to D_{AR}	D_{DR}		750 380 130 750		ms ms ms ms	500-600 Hz 600 - 1000 Hz 1000 - 2600 Hz 2600 - 2800 Hz
9	Crosstalk D/A to A/D A/D to D/A	CT_{RT} CT_{TR}		-90 -90	-74 -80	dB dB	ITU-T G.714.16

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.
* Note: RxINC, refer to Control Register 1, address 00h.

AC Electrical Characteristics† for Side-tone Path

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Absolute path gain gain adjust = 0 dB	G_{AS1} G_{AS2}	-17.1 -11.1	-16.5 -10.5	-15.9 -9.9	dB dB	RxINC = 0* RxINC = 1* M± inputs to HSPKR± outputs 1000 Hz at STG2=1
2	Tolerance of other side-tone settings (-9.96 to 9.96 dB) relative to output at 0 dB setting		-0.5	+/-0.2	+0.5	dB	

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.
* Note: RxINC, refer to Control Register 1, address 00h.

Electrical Characteristics† for Analog Outputs

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Earpiece load impedance	E_{ZL}	260	300		ohms	across HSPKR±
2	Allowable earpiece capacitive load	E_{CL}		300		pF	each pin: HSPKR+, HSPKR-
3	Earpiece harmonic distortion	E_D		0.5		%	300 ohms load across HSPKR± (tol-15%), VO≤693mV_{RMS}, RxINC=1*, Rx gain=0 dB

† Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.
* Note: RxINC, refer to Control Register 1, address 00h.

Electrical Characteristics† for Analog Inputs

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Maximum input voltage without overloading Codec across M+/M-	V_{IOLH}		2.128 0.756		Vp-p Vp-p	TxINC = 0, A/$\overline{\mu}$ = 0* TxINC = 1, A/μ = 1* Tx filter gain=0 dB setting
2	Input Impedance	Z_I	50			kW	M+/M- to V_{SSA}

† Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.
* Note: TxINC, refer to Control Register 1, address 00h.

AC Electrical Characteristics† - ST-BUS Timing (See Figure 11)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	$\overline{C4i}$ Clock Period	t_{C4P}		244		ns	
2	$\overline{C4i}$ Clock High period	t_{C4H}		122		ns	
3	$\overline{C4i}$ Clock Low period	t_{C4L}		122		ns	
4	$\overline{C4i}$ Clock Transition Time	t_T		20		ns	
5	$\overline{F0i}$ Frame Pulse Setup Time	t_{F0iS}	50			ns	
6	$\overline{F0i}$ Frame Pulse Hold Time	t_{F0iH}	50			ns	
7	Delayed Frame Pulse delay after C4i rising	t_{F0odS}			55	ns	
8	Delayed Frame Pulse hold time from C4i rising	t_{F0odH}			50	ns	
9	DSTo Delay	t_{DSToD}			125	ns	C_L = 30 pF, 1 kΩ load.*
10	DSTi Setup Time	t_{DSTiS}	20			ns	
11	DSTi Hold Time	t_{DSTiH}	50			ns	

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.
* Note: All conditions → data-data, data-HiZ, HiZ-data.

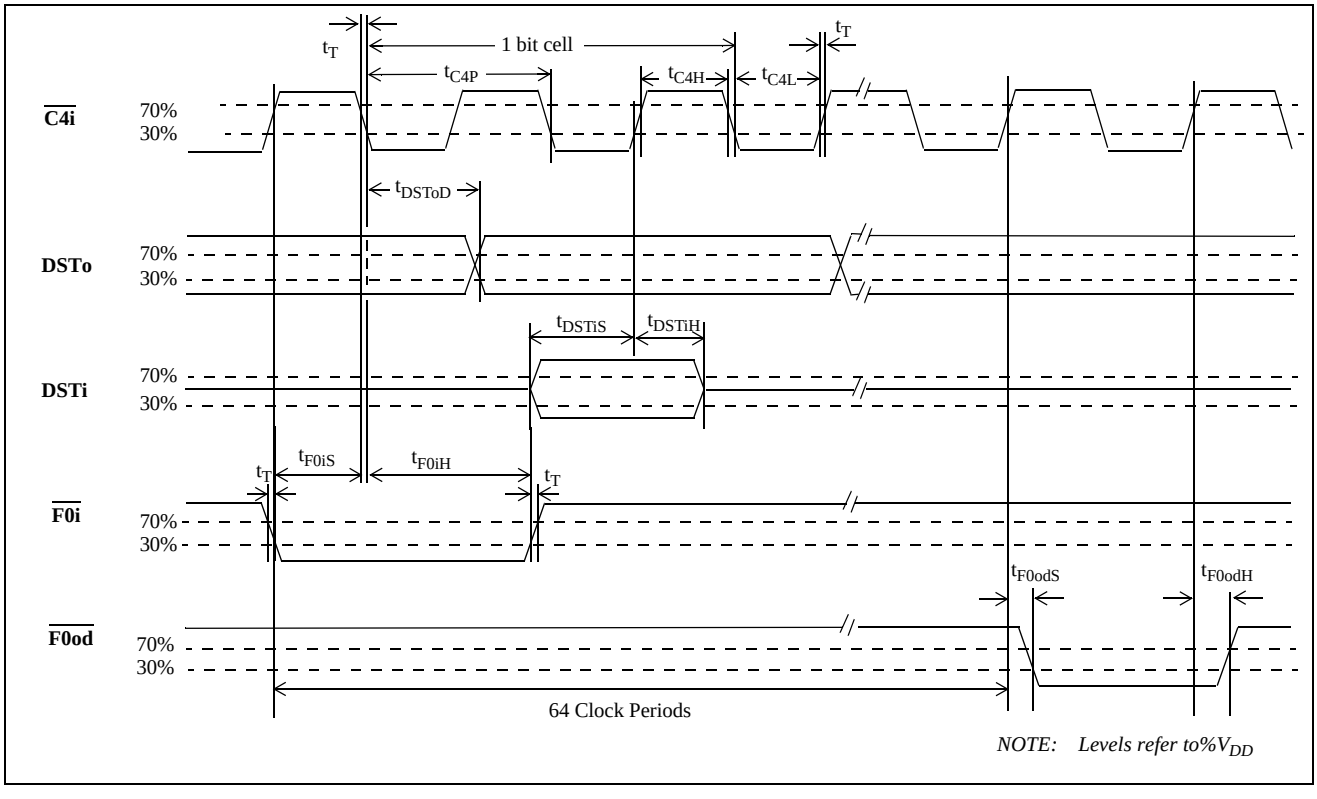


Figure 11 - ST-BUS Timing Diagram

AC Electrical Characteristics† - SSI BUS Synchronous Timing (see Figure 12)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	BCL Clock Period	t_{BCL}	244		1953	ns	BCL=4096 kHz to 512 kHz
2	BCL Pulse Width High	t_{BCLH}	115	122		ns	BCL=4096 kHz
3	BCL Pulse Width Low	t_{BCLL}		122		ns	BCL=4096 kHz
4	BCL Rise/Fall Time	t_R/t_F		20		ns	Note 1
5	Strobe Pulse Width	t_{ENW}		8 x t_{BCL}		ns	Note 1
6	Delayed Strobe Pulse Width	t_{ENWD}		8 x t_{BCL}		ns	Note 1
7	Strobe setup time before BCL falling	t_{SSS}	70		t_{BCL}-80	ns	
8	Strobe hold time after BCL falling	t_{SSH}	80		t_{BCL}-80	ns	
9	Delayed Strobe Pulse delay after BCL rising	t_{DSTBR}			55	ns	Note 1
10	Delayed Strobe Pulse hold time after BCL rising	t_{DSTBF}			55	ns	Note 1
11	Dout High Impedance to Active Low from Strobe rising	t_{DOZL}			55	ns	C_L=50 pF, R_L=1 K
12	Dout High Impedance to Active High from Strobe rising	t_{DOZH}			55	ns	C_L=50 pF, R_L=1 K
13	Dout Active Low to High Impedance from Strobe falling	t_{DOLZ}			90	ns	C_L=50 pF, R_L=1 K
14	Dout Active High to High Impedance from Strobe falling	t_{DOHZ}			90	ns	C_L=50 pF, R_L=1 K
15	Dout Delay (high and low) from BCL rising	t_{DD}			80	ns	C_L=50 pF, R_L=1 K
16	Din Setup time before BCL falling	t_{DIS}	10			ns	
17	Din Hold Time from BCL falling	t_{DIH}	50			ns	

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Note 1: Not production tested, guaranteed by design.

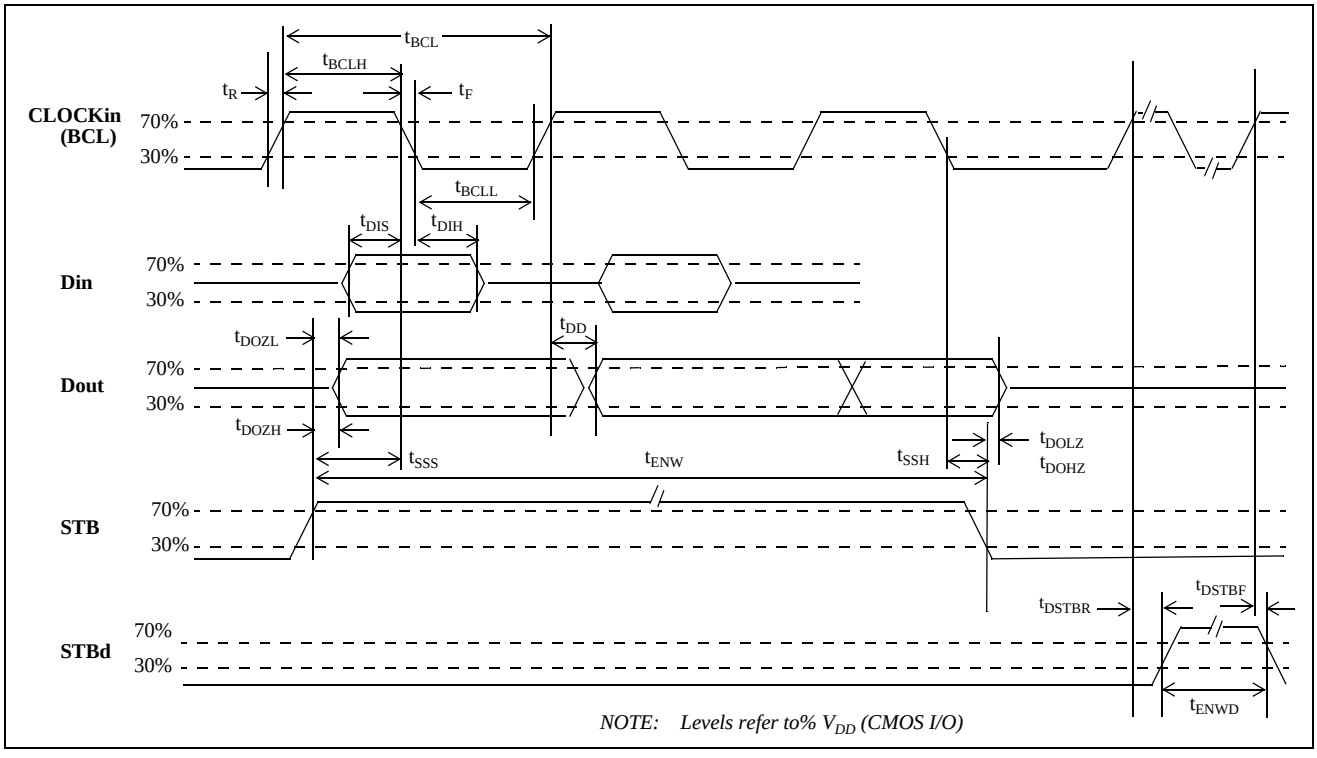


Figure 12 - SSI Synchronous Timing Diagram

AC Electrical Characteristics† - SSI BUS Asynchronous Timing (note 1) (see Figure 13)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Bit Cell Period	T_{DATA}		7812 3906		ns ns	BCL=128 kHz BCL=256 kHz
2	Frame Jitter	T_j			600	ns	
3	Bit 1 Dout Delay from STB going high	t_{dda1}			T_j+600	ns	C_L=50 pF, R_L=1 K
4	Bit 2 Dout Delay from STB going high	t_{dda2}	600+ T_{DATA}-T_j	600+ T_{DATA}	600 + T_{DATA}+T_j	ns	C_L=50 pF, R_L=1 K
5	Bit n Dout Delay from STB going high	t_{ddan}	600 + (n-1) x T_{DATA}-T_j	600 + (n-1) x T_{DATA}	600 + (n-1) x T_{DATA}+T_j	ns	C_L=50 pF, R_L=1 K n=3 to 8
6	Bit 1 Data Boundary	T_{DATA1}	T_{DATA}-T_j		T_{DATA}+T_j	ns	
7	Din Bit n Data Setup time from STB rising	t_{SU}	T_{DATA}\2 +500ns-T_j +(n-1) x T_{DATA}			ns	n=1-8
8	Din Data Hold time from STB rising	t_{ho}	T_{DATA}\2 +500ns+T_j +(n-1) x T_{DATA}			ns	

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Note 1: Not production tested, guaranteed by design.

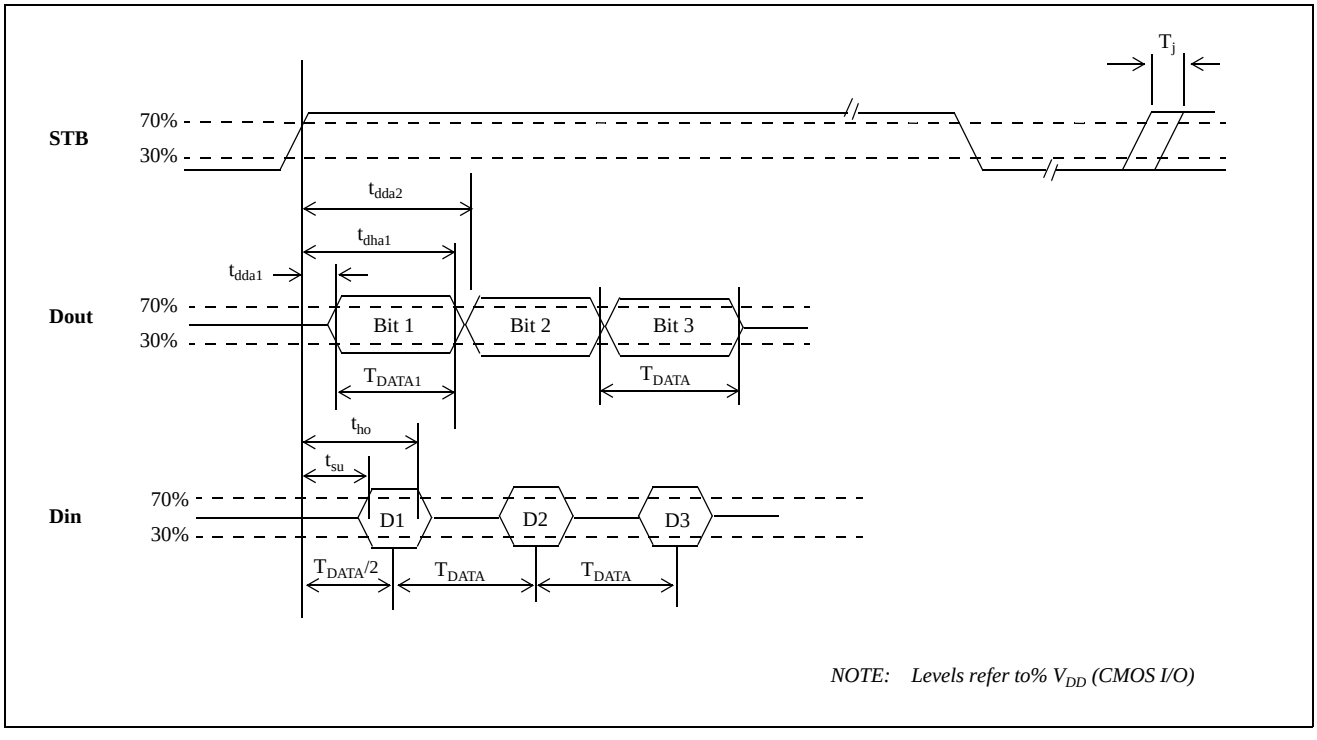


Figure 13 - SSI Asynchronous Timing Diagram

AC Electrical Characteristics† - Microport Timing (see Figure 14)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Input data setup	t_{IDS}	100			ns	
2	Input data hold	t_{IDH}	30			ns	
3	Output data delay	t_{ODD}			120	ns	C_L = 50pF, R_L = 1 K *
4	Serial clock period	t_{CYC}	500	1000		ns	
5	SCLK pulse width high	t_{CH}	250	500		ns	
6	SCLK pulse width low	t_{CL}	250	500		ns	
7	$\overline{CS}$ setup-Intel	t_{CSSI}	200			ns	
8	$\overline{CS}$ setup-Motorola	t_{CSSM}	100			ns	
9	$\overline{CS}$ hold	t_{CSH}	100			ns	
10	$\overline{CS}$ to output high impedance	t_{OHZ}			120	ns	C_L = 50pF, R_L = 1 K

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Note: All conditions → data-data, data-HiZ, HiZ-data.

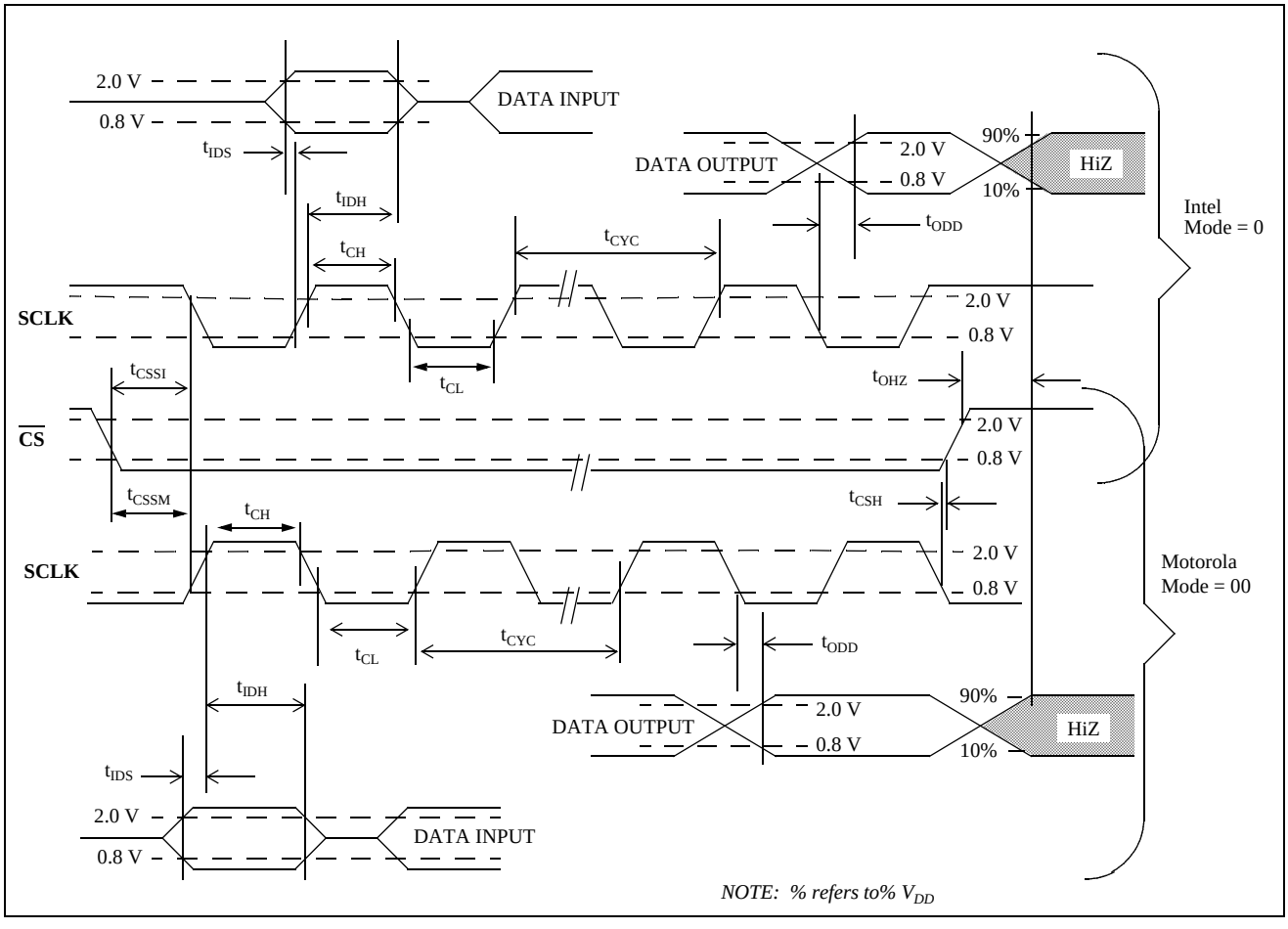
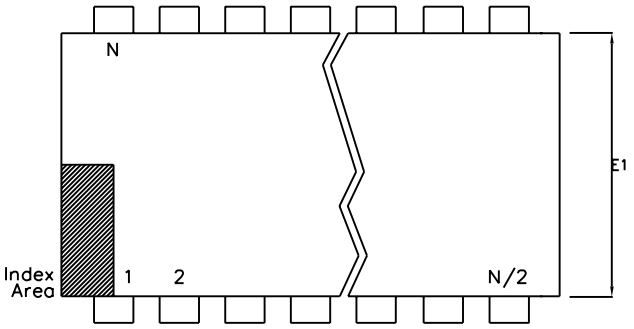
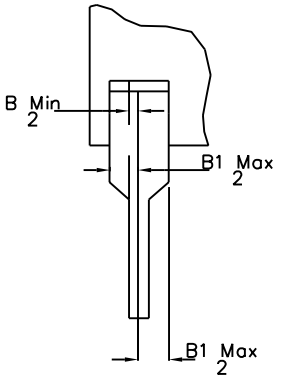
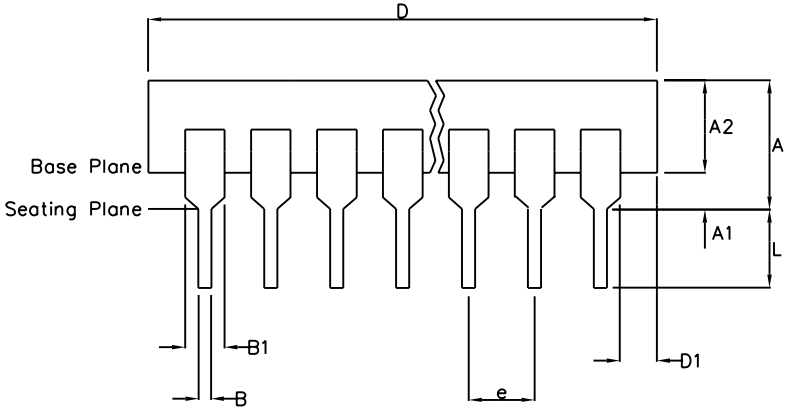
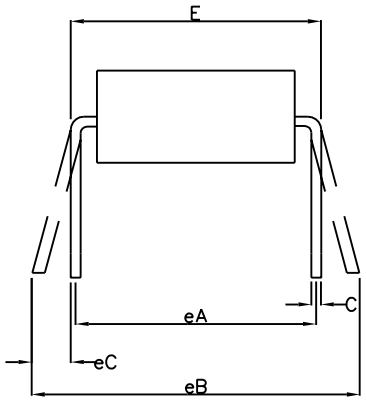


Figure 14 - Microport Timing









	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	29.21	32.77	1.150	1.290
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	24		24	
Conforms to Jedec MS-011AA ISS.B				

Notes:
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

ISSUE	1	2	3	
ACN	7010	203400	213101	
DATE	20Apr95	4Nov97	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

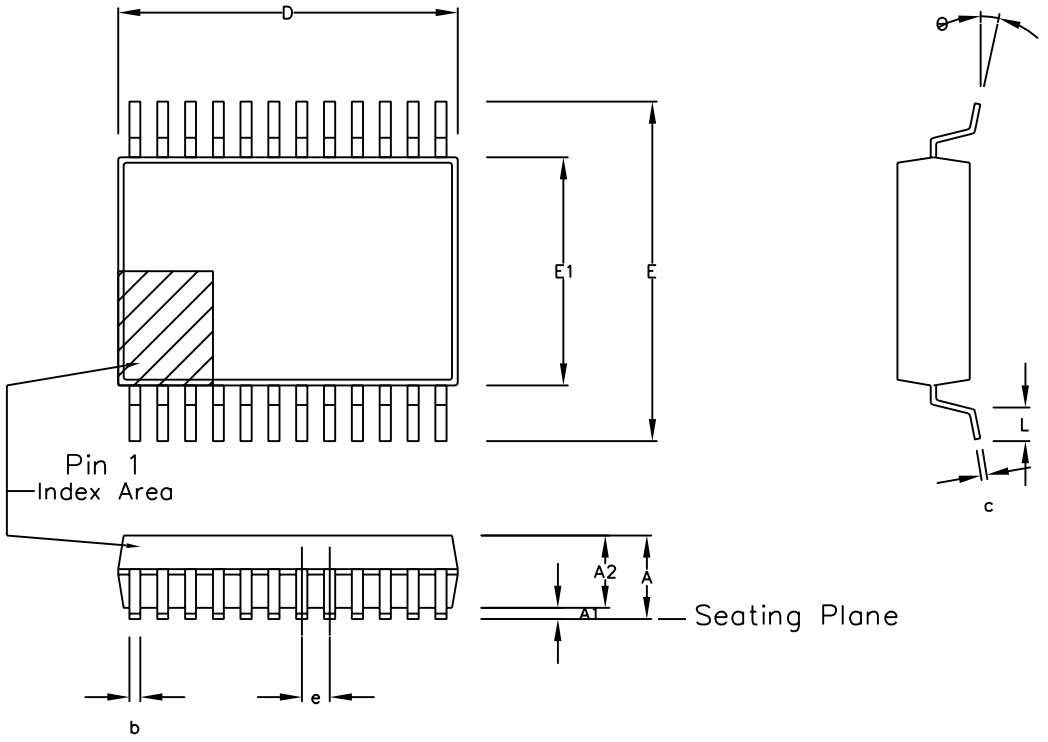
Previous package codes

DP / E

Package Code DA

Package Outline for 24 lead PDIP

GPD00071



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	1.70		2.00		0.067		0.079
A1	0.05		0.20		0.002		0.008
A2	1.65		1.85		0.065		0.073
D	7.90		8.50		0.311		0.335
E	7.40		8.20		0.291		0.323
E1	5.00		5.60		0.197		0.220
L	0.55		0.95		0.022		0.037
e	0.65 BSC.				0.026 BSC.		
b	0.22		0.38		0.009		0.015
c	0.09		0.25		0.004		0.010
θ	0°		8°		0°		8°
	Pin features						
N	24						
Conforms to JEDEC MO-150 AG Iss. B							

This drawing supersedes:-
418/ED/51481/003 (UK)

Notes:
1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protrusion. Mould flash or protrusion shall not exceed 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

ISSUE	1	2	3	
ACN	201934	205233	213104	
DATE	27Feb97	25Sep98	15Jul02	
APPRD.				

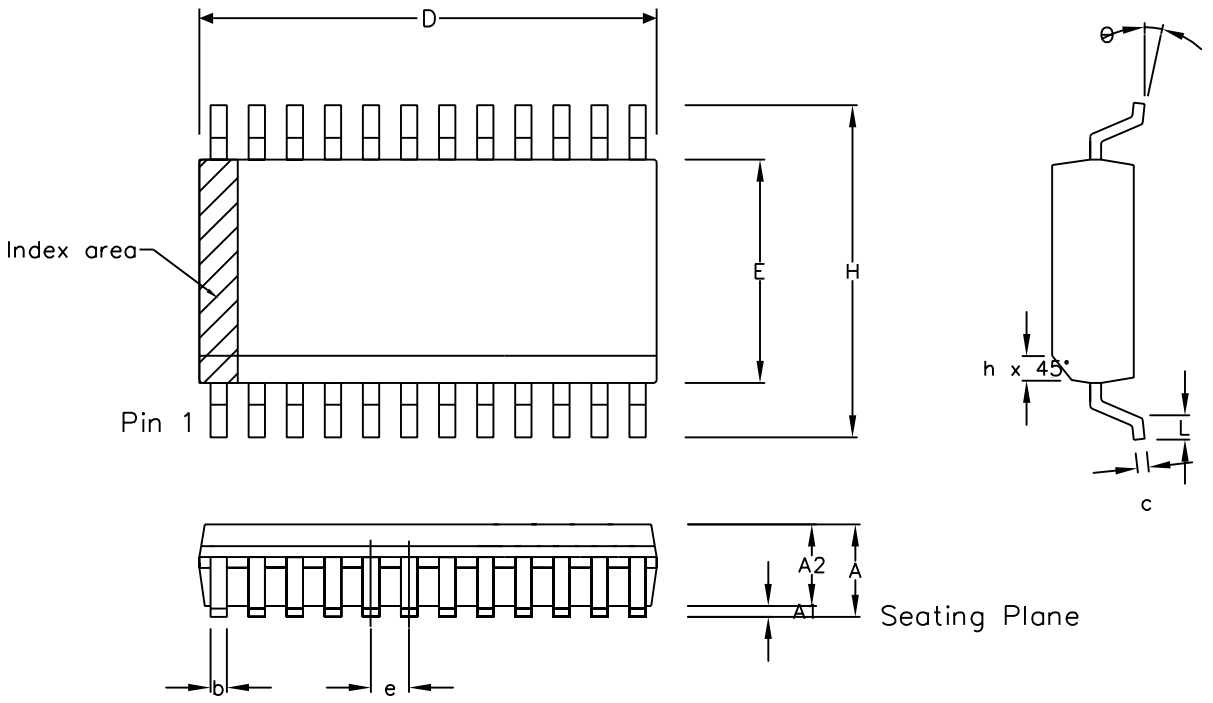
ZARLINK SEMICONDUCTOR

Previous package codes
NP / N

Package Code DD

Package Outline for
24 lead SSOP
(5.3mm Body Width)

GPD00295



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.35		2.65		0.093		0.104
A1	0.10		0.30		0.004		0.012
A2	2.25		2.35		0.089		0.092
D	15.20		15.60		0.599		0.614
H	10.00		10.65		0.394		0.419
E	7.40		7.60		0.291		0.299
L	0.40		1.27		0.016		0.050
e	1.27 BSC.				0.050 BSC.		
b	0.33		0.51		0.013		0.020
c	0.23		0.32		0.009		0.013
θ	0°		8°		0°		8°
h	0.25		0.75		0.010		0.029
	Pin features						
N	24						
Conforms to JEDEC MS-013AD Iss. C							

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	
ACN	6746	201942	213099	
DATE	7Apr95	27Feb97	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

MP / S

Package Code DC

Package Outline for 24 lead SOIC (0.300" Body Width)

GPD00016

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