

# MJW21192 (NPN), MJW21191 (PNP)

## Complementary Silicon Plastic Power Transistors

Specifically designed for power audio output, or high power drivers in audio amplifiers.

- DC Current Gain Specified up to 8.0 A at Temperature
- All On Characteristics at Temperature
- High SOA: 20 A, 18 V, 100 ms
- TO-247AE Package
- Pb-Free Packages are Available\*

### MAXIMUM RATINGS

Rating	Symbol	MJW21191 MJW21192	Unit
Collector-Emitter Voltage	$V_{CEO}$	150	Vdc
Collector-Base Voltage	$V_{CB}$	150	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current – Continuous – Peak	$I_C$	8.0 16	Adc
Base Current	$I_B$	2.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	125 0.65	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

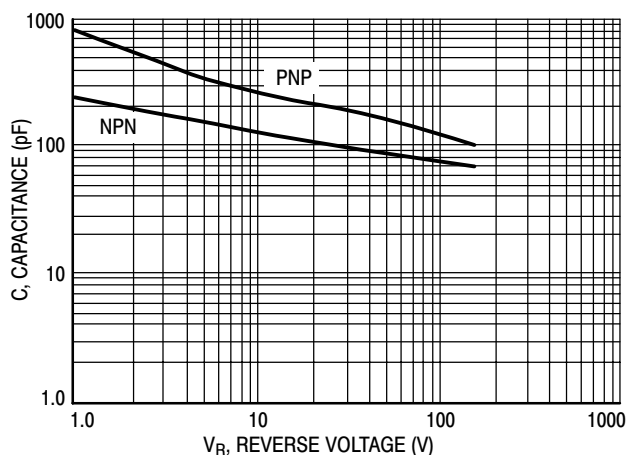


Figure 1. Typical Capacitance @  $25^\circ\text{C}$

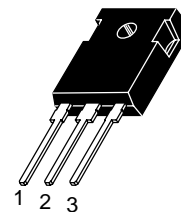
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

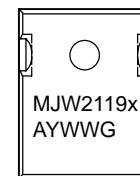
<http://onsemi.com>

## 8.0 A POWER TRANSISTORS COMPLEMENTARY SILICON 150 V, 125 W



TO-247  
CASE 340L  
STYLE 3

### MARKING DIAGRAM



1 BASE  
2 COLLECTOR  
3 EMITTER

x = 1 or 2  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping
MJW21191	TO-247	30 Units/Rail
MJW21191G	TO-247 (Pb-Free)	30 Units/Rail
MJW21192	TO-247	30 Units/Rail
MJW21192G	TO-247 (Pb-Free)	30 Units/Rail

# MJW21192 (NPN), MJW21191 (PNP)

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (Note 1) ( $I_C = 10\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	150	–	Vdc
Collector Cutoff Current ( $V_{CB} = 250\text{ Vdc}$ , $I_E = 0$ )	$I_{CES}$	–	10	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	10	$\mu\text{Adc}$
<b>ON CHARACTERISTICS (Note 1)</b>				
DC Current Gain ( $I_C = 4.0\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ ) ( $I_C = 8.0\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ )	$h_{FE}$	15 5.0	100 –	–
Collector–Emitter Saturation Voltage ( $I_C = 4.0\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ ) ( $I_C = 8.0\text{ Adc}$ , $I_B = 1.6\text{ Adc}$ )	$V_{CE(sat)}$	– –	1.0 2.0	Vdc
Base–Emitter On Voltage ( $I_C = 4.0\text{ Adc}$ , $V_{CE} = 2.0\text{ Vdc}$ )	$V_{BE(on)}$	–	2.0	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current Gain – Bandwidth Product (Note 2) ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$f_T$	4.0	–	MHz

1. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .
2.  $f_T = |h_{fe}| \cdot f_{test}$ .

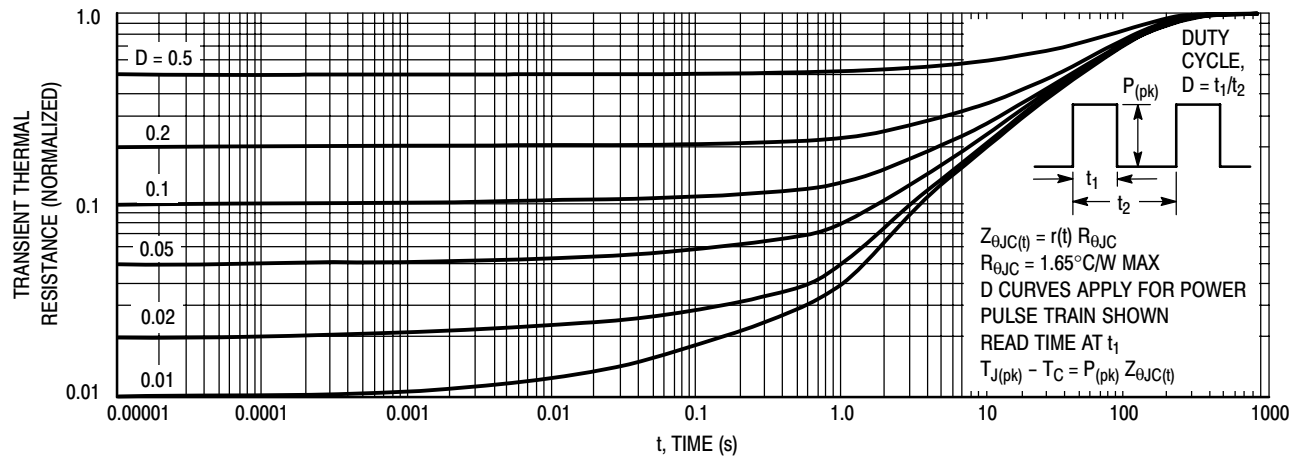


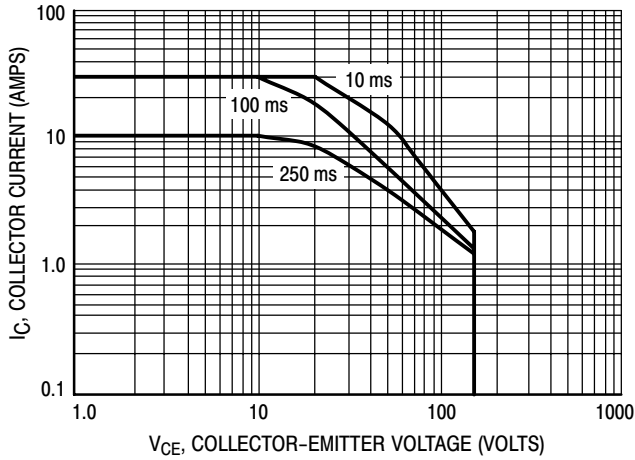
Figure 2. Thermal Response

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 3 and 4 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

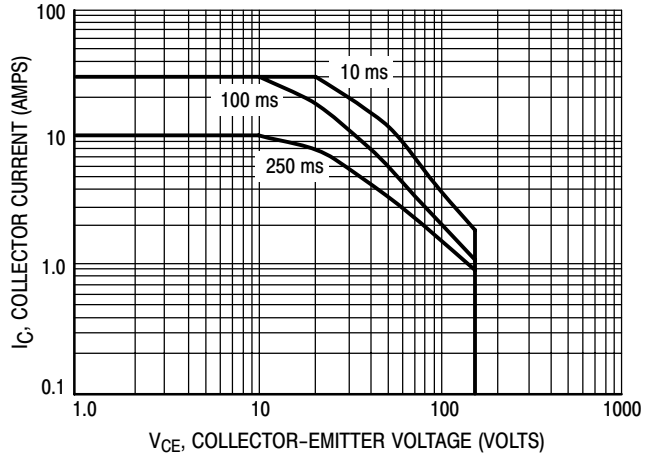
# MJW21192 (NPN), MJW21191 (PNP)

**NPN — MJW21192**



**Figure 3. NPN — MJW21192  
Safe Operating Area**

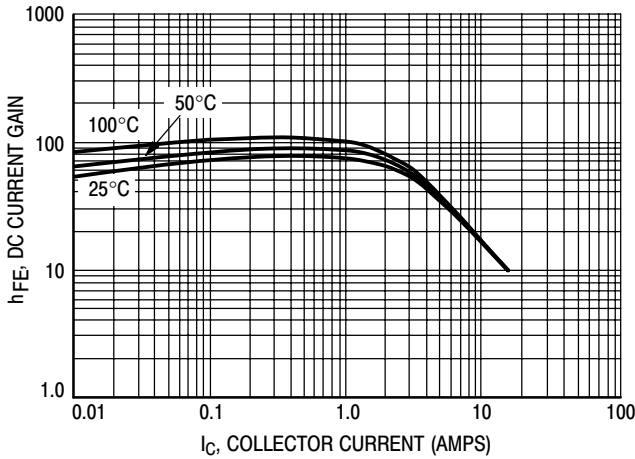
**PNP — MJW21191**



**Figure 4. PNP — MJW21191  
Safe Operating Area**

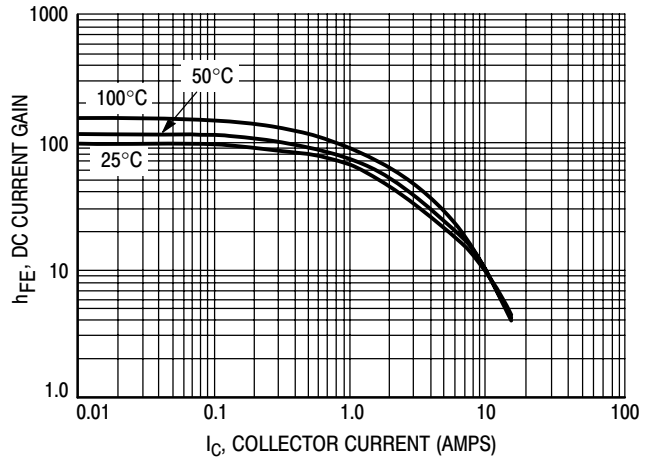
## TYPICAL CHARACTERISTICS

**NPN — MJW21192**



**Figure 5. NPN — MJW21192  
 $V_{CE} = 2.0$  V DC Current Gain**

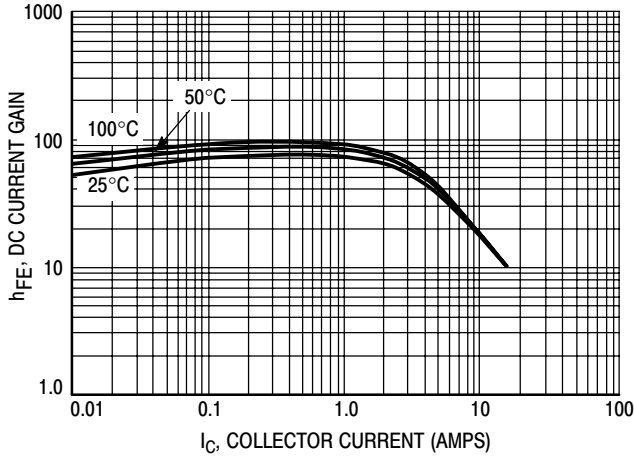
**PNP — MJW21191**



**Figure 6. PNP — MJW21191  
 $V_{CE} = 2.0$  V DC Current Gain**

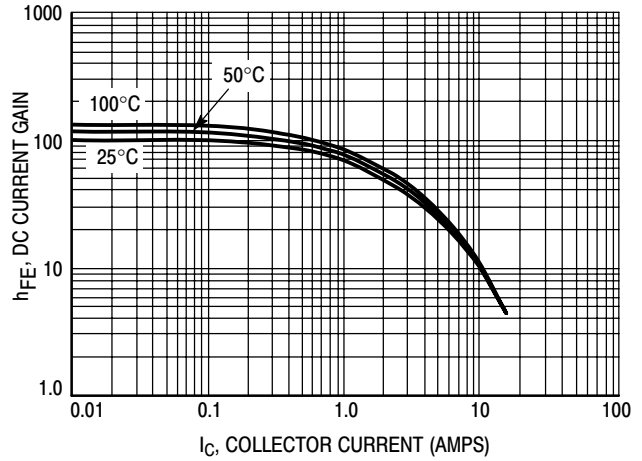
# MJW21192 (NPN), MJW21191 (PNP)

**NPN — MJW21192**

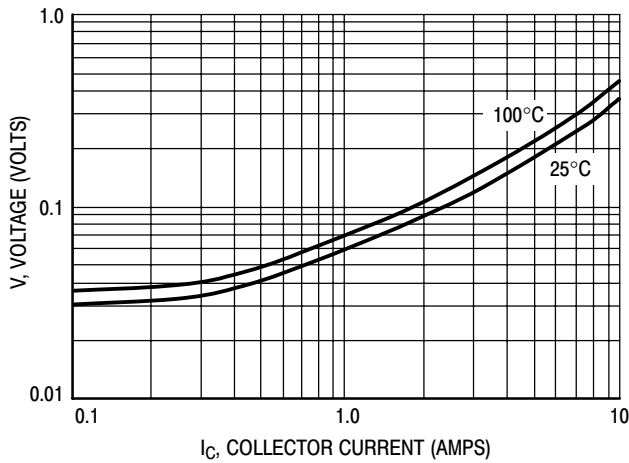


**Figure 7. NPN — MJW21192**  
 $V_{CE} = 5.0 \text{ V DC Current Gain}$

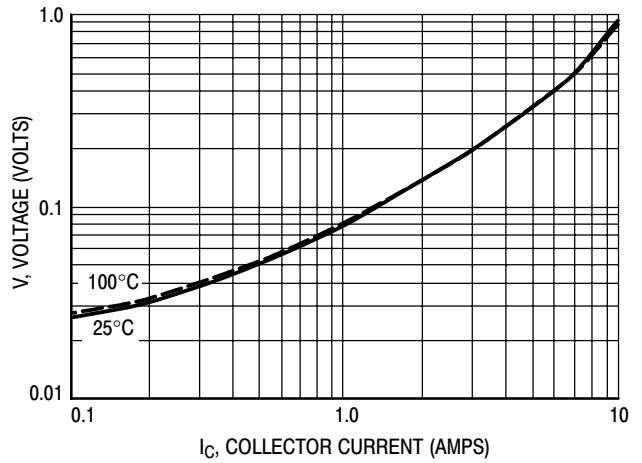
**PNP — MJW21191**



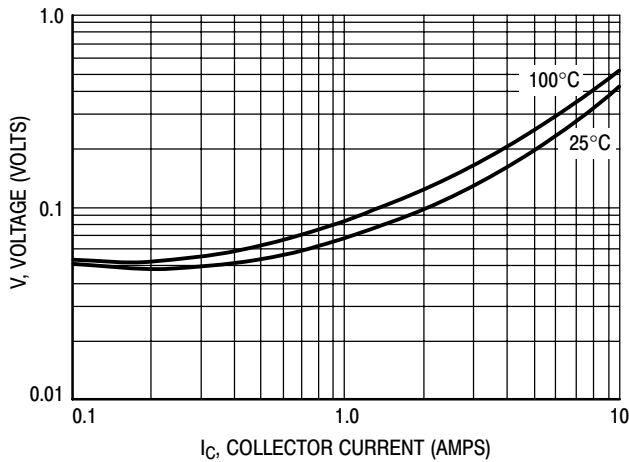
**Figure 8. PNP — MJW21191**  
 $V_{CE} = 5.0 \text{ V DC Current Gain}$



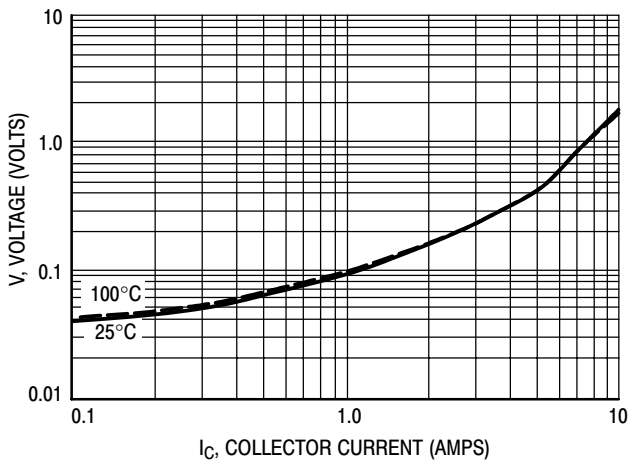
**Figure 9. NPN — MJW21192**  
 $V_{CE(sat)} I_C/I_B = 5.0$



**Figure 10. PNP — MJW21191**  
 $V_{CE(sat)} I_C/I_B = 5.0$



**Figure 11. NPN — MJW21192**  
 $V_{CE(sat)} I_C/I_B = 10$



**Figure 12. PNP — MJW21191**  
 $V_{CE(sat)} I_C/I_B = 10$

# MJW21192 (NPN), MJW21191 (PNP)

NPN — MJW21192

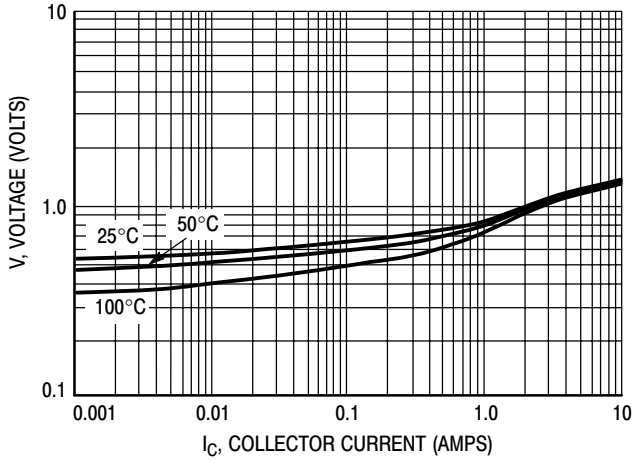


Figure 13. NPN — MJW21192  
 $V_{CE} = 2.0$  V  $V_{BE(on)}$  Curve

PNP — MJW21191

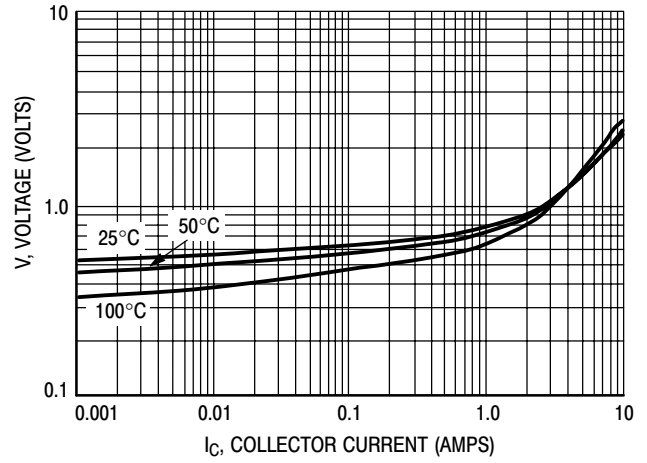
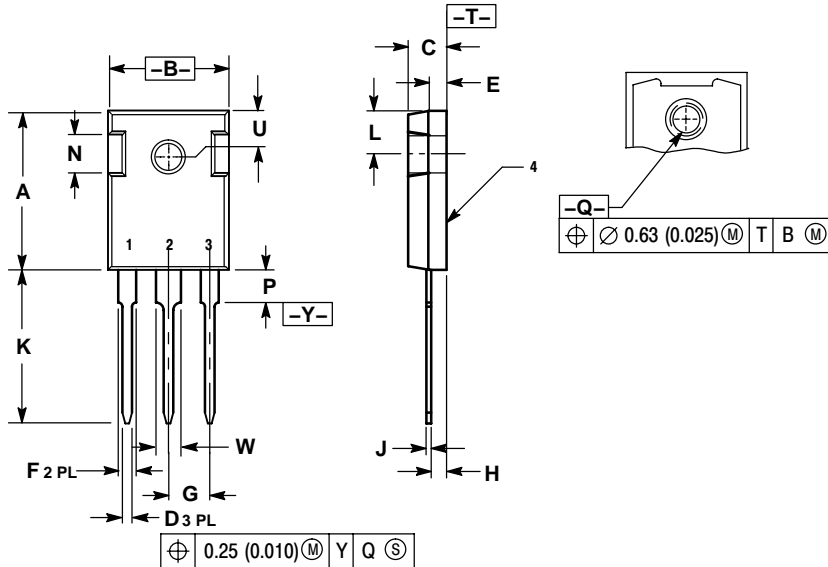


Figure 14. PNP — MJW21191  
 $V_{CE} = 2.0$  V  $V_{BE(on)}$  Curve

# MJW21192 (NPN), MJW21191 (PNP)

## PACKAGE DIMENSIONS

TO-247  
CASE 340L-02  
ISSUE D



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	2.20	2.60	0.087	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	20.06	20.83	0.790	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	---	4.50	---	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

- STYLE 3:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.