

# MJF15030 (NPN), MJF15031 (PNP)



ON Semiconductor®

<http://onsemi.com>

## Complementary Power Transistors For Isolated Package Applications

Designed for general-purpose amplifier and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

### Features

- Electrically Similar to the Popular MJE15030 and MJE15031
- 150 V<sub>CEO(sus)</sub>
- 8 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High Current Gain-Bandwidth Product –  
 $f_T = 30 \text{ MHz (Min) @ } I_C = 500 \text{ mA}$
- UL Recognized, File #E69369, to 3500 V<sub>RMS</sub> Isolation
- Pb-Free Packages are Available\*

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V <sub>CEO</sub>	150	Vdc
Collector-Base Voltage	V <sub>CB</sub>	150	Vdc
Emitter-Base Voltage	V <sub>EB</sub>	5	Vdc
RMS Isolation Voltage (Note 1) Test No. 1 Per Figure 11 Test No. 2 Per Figure 12 Test No. 3 Per Figure 13 (for 1 sec, R.H. < 30%, T <sub>A</sub> = 25°C)	V <sub>ISOL</sub>	4500 3500 1500	V <sub>RMS</sub>
Collector Current – Continuous – Peak	I <sub>C</sub>	8 16	Adc
Base Current	I <sub>B</sub>	2	Adc
Total Power Dissipation (Note 2) @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	36 0.016	W W/°C
Total Power Dissipation @ T <sub>A</sub> = 25°C Derate above 25°C	P <sub>D</sub>	2.0 0.016	W W/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-65 to +150	°C

### THERMAL CHARACTERISTICS

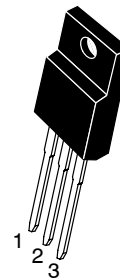
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	°C/W
Thermal Resistance, Junction-to-Case (Note 2)	R <sub>θJC</sub>	3.5	°C/W
Lead Temperature for Soldering Purposes	T <sub>L</sub>	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Proper strike and creepage distance must be provided.
2. Measurement made with thermocouple contacting the bottom insulated surface (in a location beneath the die), the devices mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.

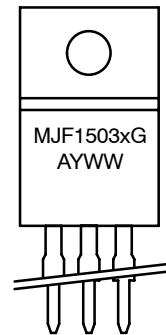
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## COMPLEMENTARY SILICON POWER TRANSISTORS 8 AMPERES 150 VOLTS, 36 WATTS



TO-220 FULLPACK  
CASE 221D  
STYLE 2

### MARKING DIAGRAM



MJF1503x = Specific Device Code  
 x = 0 or 1  
 G = Pb-Free Package  
 A = Assembly Location  
 Y = Year  
 WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MJF15030	TO-220 FULLPACK	50 Units/Rail
MJF15030G	TO-220 FULLPACK (Pb-Free)	50 Units/Rail
MJF15031	TO-220 FULLPACK	50 Units/Rail
MJF15031G	TO-220 FULLPACK (Pb-Free)	50 Units/Rail

# MJF15030 (NPN), MJF15031 (PNP)

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (Note 3) ( $I_C = 10\text{ mA}$ , $I_B = 0$ )	$V_{CE(sus)}$	150	–	Vdc
Collector Cutoff Current ( $V_{CE} = 150\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	–	10	$\mu\text{A}$
Collector Cutoff Current ( $V_{CB} = 150\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	–	10	$\mu\text{A}$
Emitter Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	10	$\mu\text{A}$
<b>ON CHARACTERISTICS (Note 3)</b>				
DC Current Gain ( $I_C = 0.1\text{ A}$ , $V_{CE} = 2\text{ Vdc}$ ) ( $I_C = 2\text{ A}$ , $V_{CE} = 2\text{ Vdc}$ ) ( $I_C = 3\text{ A}$ , $V_{CE} = 2\text{ Vdc}$ ) ( $I_C = 4\text{ A}$ , $V_{CE} = 2\text{ Vdc}$ )	$h_{FE}$	40	–	–
		40	–	–
		40	–	–
		20	–	–
DC Current Gain Linearity ( $V_{CE}$ from 2 V to 20 V, $I_C$ from 0.1 A to 3 A) (NPN to PNP)	$h_{FE}$	<b>Typ</b>		
		2 3		
Collector–Emitter Saturation Voltage ( $I_C = 1\text{ A}$ , $I_B = 0.1\text{ A}$ )	$V_{CE(sat)}$	–	0.5	Vdc
Base–Emitter On Voltage ( $I_C = 1\text{ A}$ , $V_{CE} = 2\text{ Vdc}$ )	$V_{BE(on)}$	–	1	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current Gain – Bandwidth Product (Note 4) ( $I_C = 500\text{ mA}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 10\text{ MHz}$ )	$f_T$	30	–	MHz

3. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

4.  $f_T = |h_{fe}| \cdot f_{test}$ .

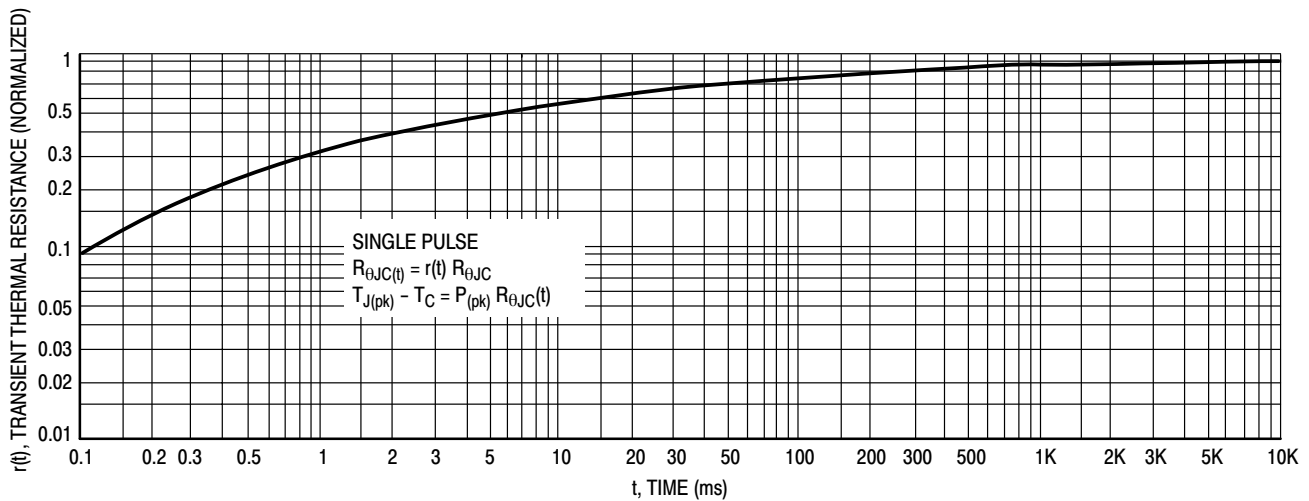


Figure 1. Thermal Response

# MJF15030 (NPN), MJF15031 (PNP)

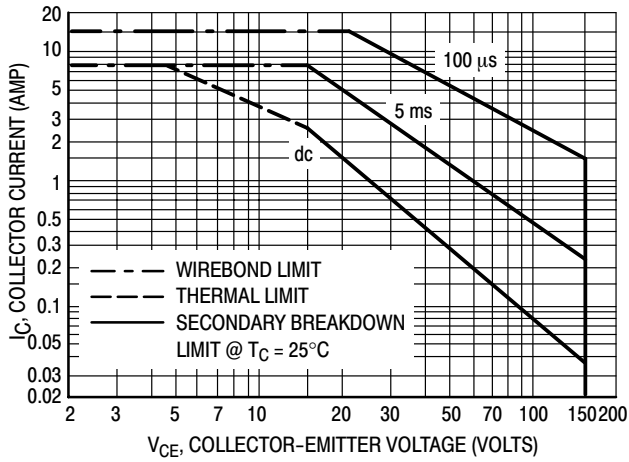


Figure 2. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 2 and 3 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

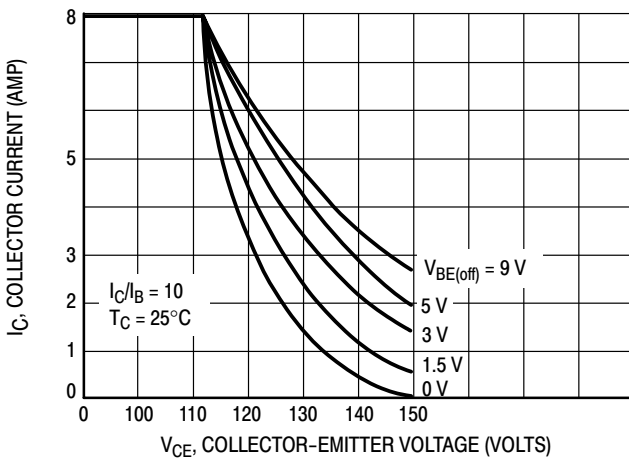


Figure 3. Reverse Bias Switching Safe Operating Area

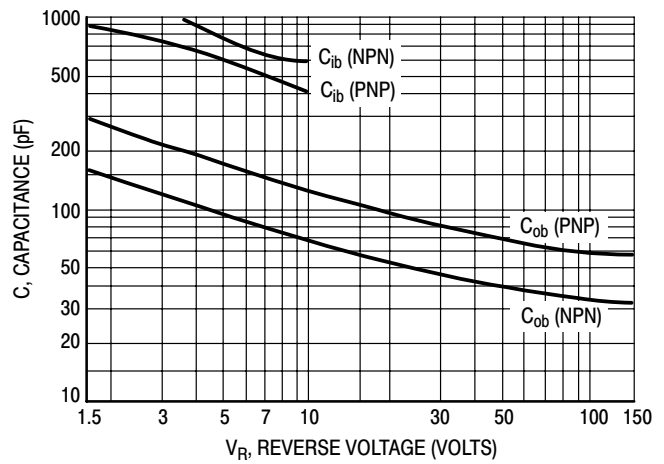


Figure 4. Capacitances

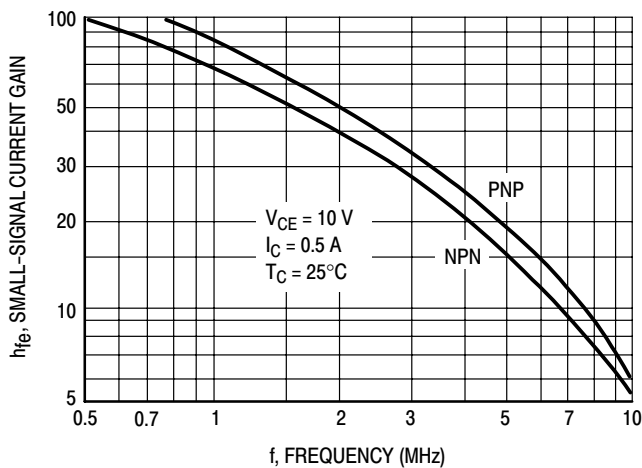


Figure 5. Small-Signal Current Gain

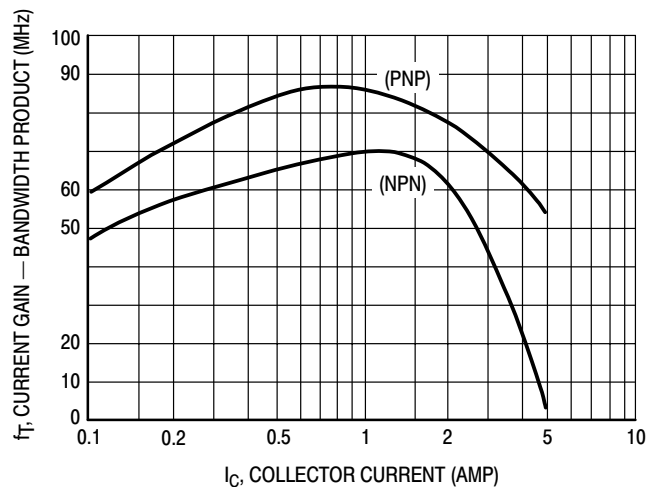


Figure 6. Current Gain — Bandwidth Product

# MJF15030 (NPN), MJF15031 (PNP)

## DC CURRENT GAIN

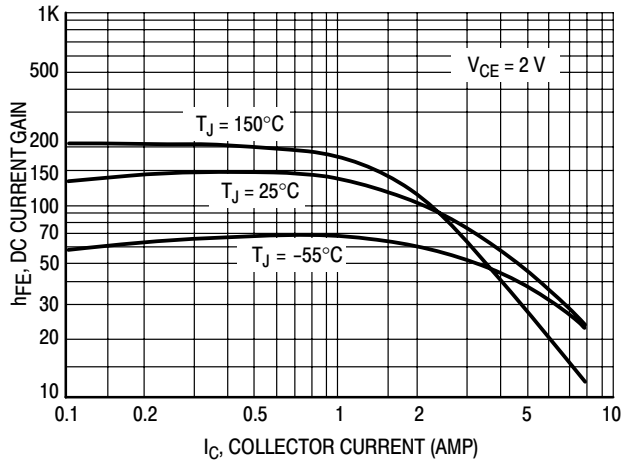


Figure 7a. MJF15030 NPN

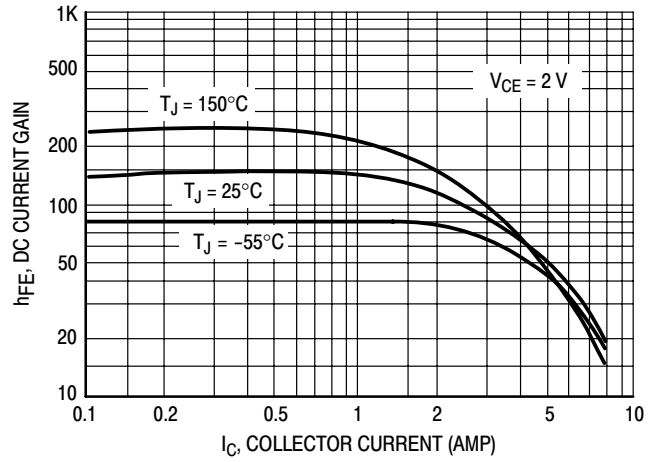


Figure 7b. MJF15031 PNP

## “ON” VOLTAGE

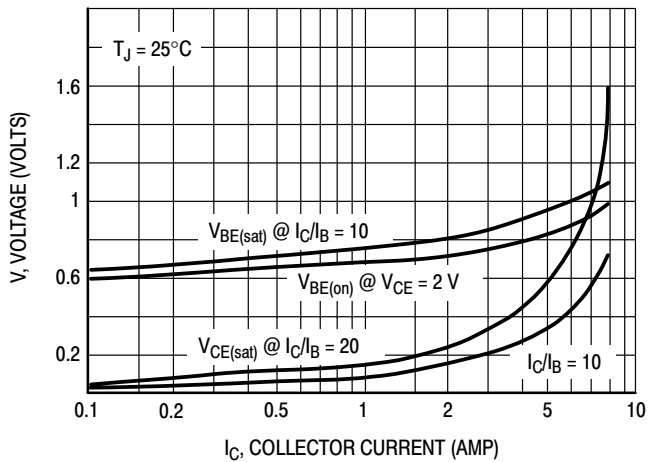


Figure 8a. MJF15030 NPN

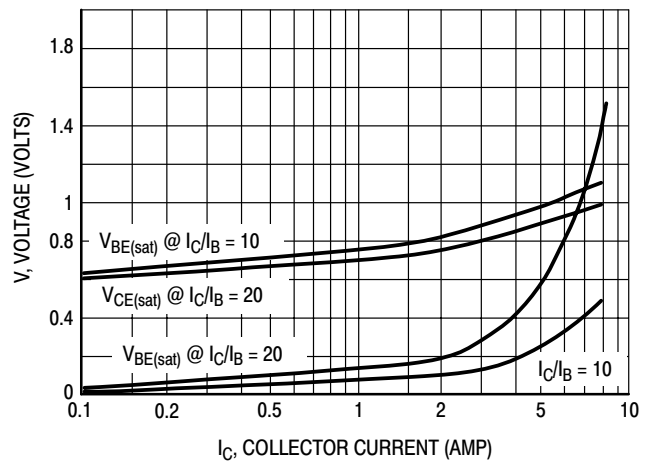


Figure 8b. MJF15031 PNP

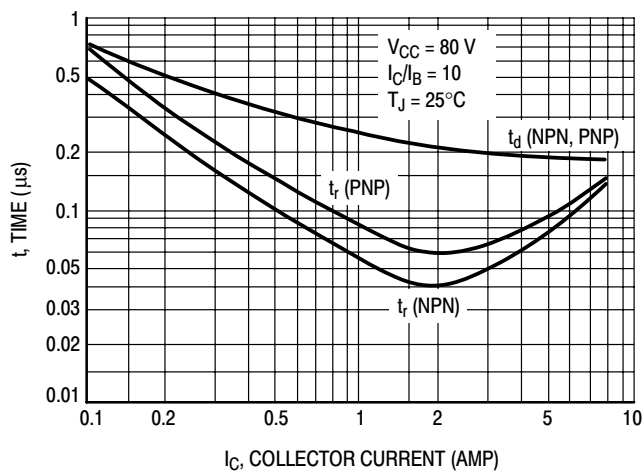


Figure 9. Turn-On Times

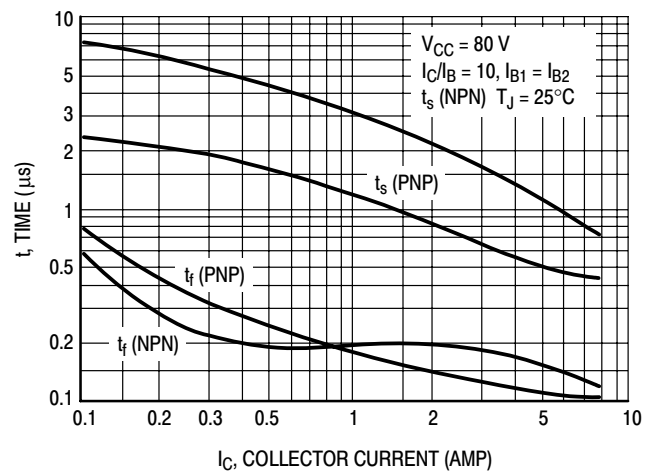
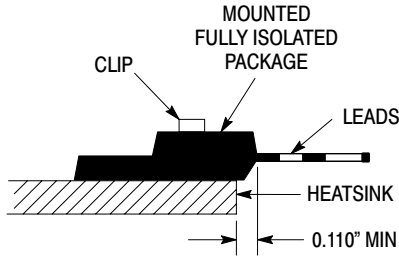


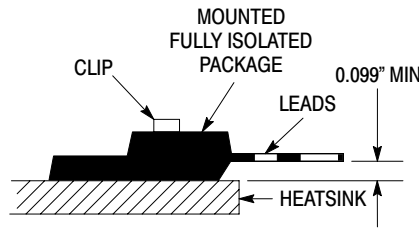
Figure 10. Turn-Off Times

# MJF15030 (NPN), MJF15031 (PNP)

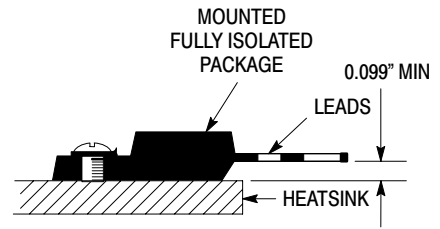
## TEST CONDITIONS FOR ISOLATION TESTS\*



**Figure 11. Clip Mounting Position for Isolation Test Number 1**



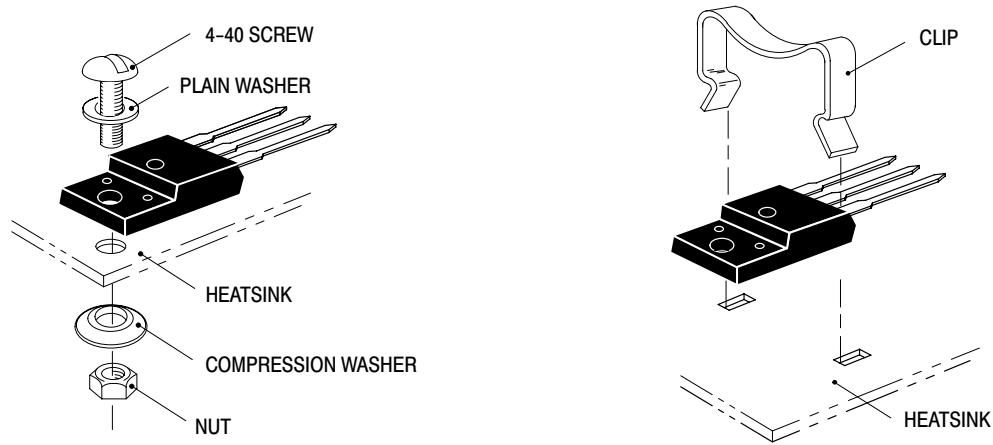
**Figure 12. Clip Mounting Position for Isolation Test Number 2**



**Figure 13. Screw Mounting Position for Isolation Test Number 3**

\*Measurement made between leads and heatsink with all leads shorted together

## MOUNTING INFORMATION



**Figure 14. Typical Mounting Techniques\***

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

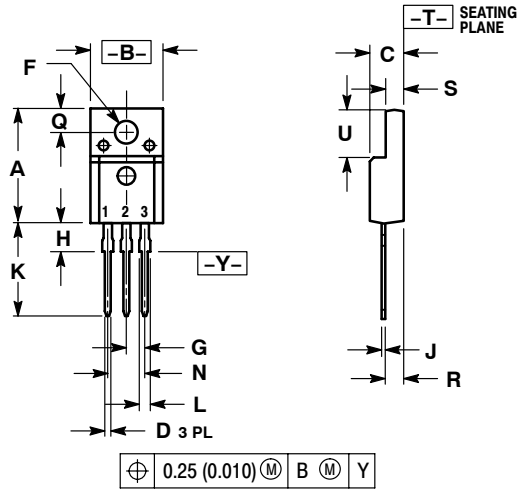
Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

\*\* For more information about mounting power semiconductors see Application Note AN1040.

# MJF15030 (NPN), MJF15031 (PNP)

## PACKAGE DIMENSIONS

TO-220 FULLPAK  
CASE 221D-03  
ISSUE G



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.625	0.635	15.88	16.12
B	0.408	0.418	10.37	10.63
C	0.180	0.190	4.57	4.83
D	0.026	0.031	0.65	0.78
F	0.116	0.119	2.95	3.02
G	0.100 BSC		2.54 BSC	
H	0.125	0.135	3.18	3.43
J	0.018	0.025	0.45	0.63
K	0.530	0.540	13.47	13.73
L	0.048	0.053	1.23	1.36
N	0.200 BSC		5.08 BSC	
Q	0.124	0.128	3.15	3.25
R	0.099	0.103	2.51	2.62
S	0.101	0.113	2.57	2.87
U	0.238	0.258	6.06	6.56

### STYLE 2:

1. BASE
2. COLLECTOR
3. EMITTER

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.