

# MC100EPT24

## LVTTL/LVCMOS to Differential LVECL Translator

The MC100EPT24 is a LVTTL/LVCMOS to differential LVECL translator. Because LVECL levels and LVTTL/LVCMOS levels are used, a -3.3V, +3.3V and ground are required. The small outline 8-lead SOIC package and the single gate of the EPT24 makes it ideal for those applications where space, performance, and low power are at a premium.

The EPT24 is available in the 100E standard and is compatible with ECL 100K logic levels.

- 350ps Typical Propagation Delay
- Maximum Frequency > 1.0GHz
- Differential ECL Outputs
- Small Outline SOIC Package
- PNP LVTTL Inputs for Minimal Loading
- Flow Through Pinouts
- Q Output will default HIGH with inputs open
- ESD Protection: 4000 KV HBM, 200 V MM
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack.  
For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8",  
Oxygen Index 28 to 34
- Transistor Count = 181 devices

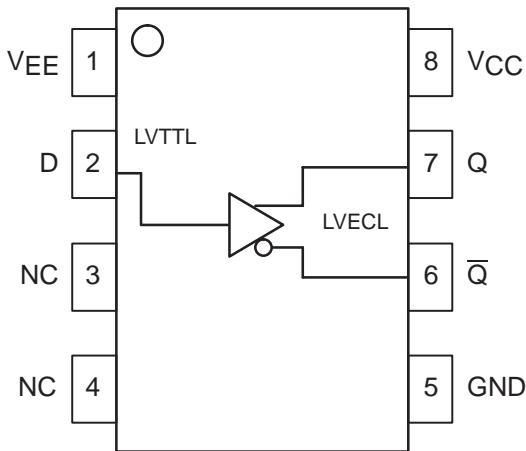
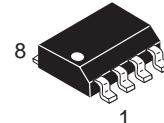


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

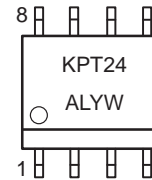


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**SO-8**  
**D SUFFIX**  
**CASE 751**

### MARKING DIAGRAM



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

\*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	FUNCTION
Q, Q̄	Differential LVECL Outputs
D	LVTTL Input
VCC	Positive Supply
GND	Ground
VEE	Negative Supply

### ORDERING INFORMATION

Device	Package	Shipping
MC100EPT24D	SOIC	98 Units/Rail
MC100EPT24DR2	SOIC	2500 Tape & Reel

# MC100EPT24

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{EE}$	Power Supply ( $V_{CC} = 0V$ )	-3.8 to 0	VDC
$V_{CC}$	Power Supply ( $V_{EE} = 0V$ )	3.8 to 0	VDC
$V_I$	Input Voltage ( $V_{CC} = 0V$ , $V_I$ not more negative than $V_{EE}$ )	-3.8 to 0	VDC
$V_I$	Input Voltage ( $V_{EE} = 0V$ , $V_I$ not more positive than $V_{CC}$ )	3.8 to 0	VDC
$I_{out}$	Output Current Continuous Surge	50 100	mA
$T_A$	Operating Temperature Range	-40 to +85	°C
$T_{stg}$	Storage Temperature	-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) Still Air 500lfpm	190 130	°C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	41 to 44 ± 5%	°C/W
$T_{sol}$	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

## LVTTTL INPUT DC CHARACTERISTICS ( $V_{CC} = 3.3V \pm 0.3V$ ; GND = 0V; $T_A = -40^\circ C$ to $+85^\circ C$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$I_{IH}$	Input HIGH Current ( $V_{in} = 2.7V$ )			20	$\mu A$
$I_{IHH}$	Input HIGH Current MAX ( $V_{in} = 6.0V$ )			100	$\mu A$
$I_{IL}$	Input LOW Current ( $V_{in} = 0.5V$ )			-0.6	mA
$V_{IK}$	Input Clamp Voltage ( $I_{in} = -18mA$ )			-1.2	V
$V_{IH}$	Input HIGH Voltage	2.0			V
$V_{IL}$	Input LOW Voltage			0.8	V

## LVECL OUTPUT DC CHARACTERISTICS ( $V_{CC} = 3.3V \pm 0.3V$ ; $V_{EE} = -3.3V \pm 0.3V$ ; GND = 0V)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output HIGH Voltage (Note 1.)	-1135	-1020	-885	-1135	-1020	-885	-1135	-1030	-885	mV
$V_{OL}$	Output LOW Voltage (Note 1.)	-1935	-1750	-1685	-1935	-1770	-1685	-1925	-1790	-1685	mV
$I_{CC}$	Power Supply Current		2.0	4.0		2.0	4.0		2.0	4.0	mA
$I_{EE}$	Power Supply Current	20	30	38	20	30	38	20	30	38	mA

1. Output levels will vary 1:1 with GND; Outputs loaded through 50 $\Omega$  to GND - 2.0V.

## AC CHARACTERISTICS ( $V_{CC} = 3.3V \pm 0.3V$ ; $V_{EE} = -3.3V \pm 0.3V$ ; GND = 0V)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency (Note 2.)	1.0			1.0			1.0			GHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential (Note 3.)	300	500	800	300	530	800	300	560	800	ps
$t_{JITTER}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
$t_r$ $t_f$	Output Rise/Fall Times (20% - 80%)	70	125	170	80	130	180	100	150	200	ps

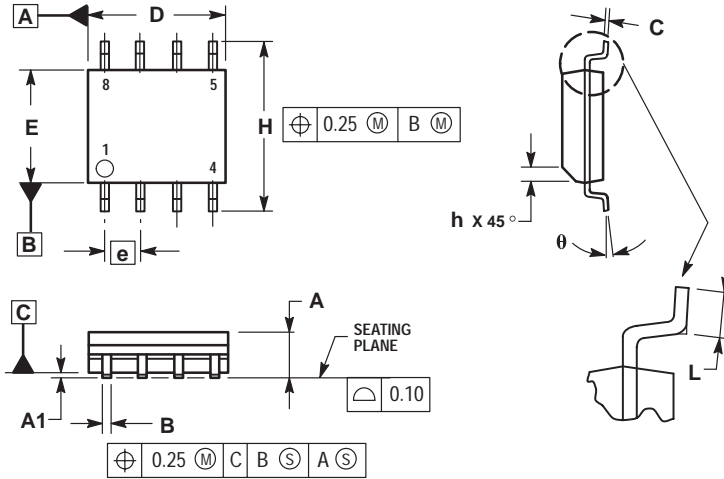
2.  $F_{max}$  guaranteed for functionality only.  $V_{OL}$  and  $V_{OH}$  levels are guaranteed at DC only.

3. TTL input of 0V to 3V.

# MC100EPT24

## PACKAGE DIMENSIONS


SO-8  
D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751-06  
ISSUE T



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
theta	0°	7°

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