MC74VHCT540A

Octal Bus Buffer

Inverting

The MC74VHCT540A is an advanced high speed CMOS inverting octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHCT540A features inputs and outputs on opposite sides of the package and two AND−ed active−low output enables. When either $\overline{OE1}$ or $\overline{OE2}$ are high, the terminal outputs are in the high impedance state.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT540A input and output (when disabled) structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

- High Speed: t_{PD} = 3.7 ns (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 4.0 μA (Max) at T_A = 25°C
- TTL−Compatible Inputs: V_{IL} = 0.8 V; V_{IH} = 2.0 V
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 1.2 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 124 FETs or 31 Equivalent Gates
- **These devices are available in Pb−free package(s). Specifications herein apply to both standard and Pb−free devices. Please see our website at www.onsemi.com for specific Pb−free orderable part numbers, or contact your local ON Semiconductor sales office or representative.**

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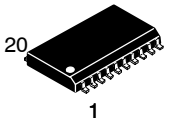
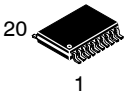
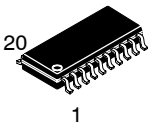
MARKING DIAGRAMS



SOIC
DW SUFFIX
CASE 751D



TSSOP
DT SUFFIX
CASE 948E



SOIC EIAJ
M SUFFIX
CASE 967

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

FUNCTION TABLE

Inputs			Output $\overline{Y}$
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

ORDERING INFORMATION

Device	Package	Shipping
MC74VHCT540ADW	SOIC	38 Units/Rail
MC74VHCT540ADT	TSSOP	75 Units/Rail
MC74VHCT540AM	SOIC	50 Units/Rail

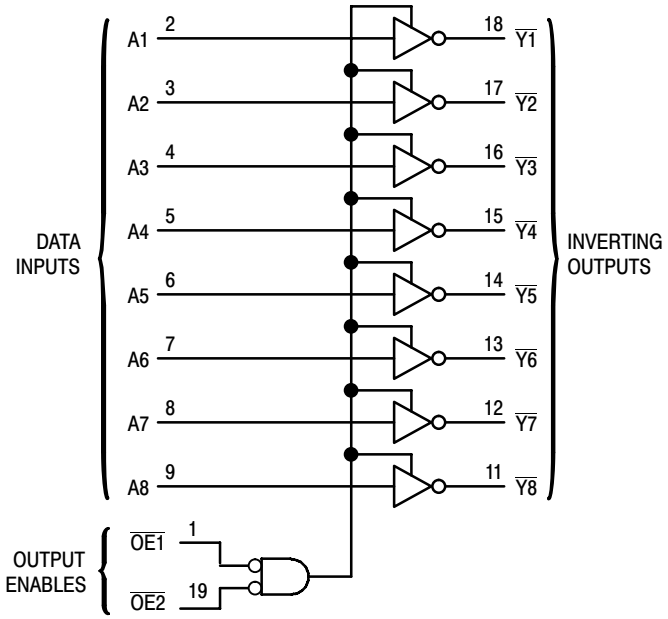


Figure 1. Logic Diagram

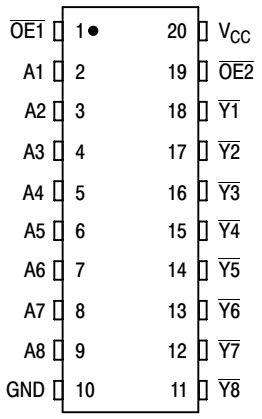


Figure 2. Pin Assignment

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	− 0.5 to + 7.0	V
V_{in}	DC Input Voltage	− 0.5 to + 7.0	V
V_{out}	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	− 20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation in Still Air (Note 2) SOIC Packages TSSOP Package	 500 450	mW
T_{stg}	Storage Temperature	− 65 to + 150	°C

1. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum−rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
2. Derating − SOIC Packages: − 7.0 mW/°C from 65° to 125°C
   TSSOP Package: − 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		4.5	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage	Outputs in 3−State High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature		−55	125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 5.0 V ±0.5 V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			$T_A \le$ 85°C		$T_A \le$ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High−Level Input Voltage		3.0 4.5 5.5	1.2 2.0 2.0			1.2 2.0 2.0		1.2 2.0 2.0		V
V_{IL}	Maximum Low−Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	Minimum High−Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OH} = − 50 μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = − 4.0 mA I_{OH} = − 8.0 mA	 3.0 4.5	 2.58 3.94			 2.48 3.80		 2.34 3.66		
V_{OL}	Maximum Low−Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 4.0 mA I_{OL} = 8.0 mA	 3.0 4.5			 0.36 0.36		 0.44 0.44		 0.52 0.52	
I_{IN}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Input: V_{IN} = 3.4 V	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5 V	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$			$T_A = -40$ to $85°C$		$T_A \le 125°C$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to $\overline{Y}$ (Figures 1 and 3)	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF		4.8	7.0	1.0	8.5		10.5	ns
		$C_L = 50$ pF		7.3	10.5	1.0	12.0		14.0	
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF		3.7	5.0	1.0	6.0		8.0	
		$C_L = 50$ pF		5.2	7.0	1.0	8.0		10.0	
t_{PZL}, t_{PZH}	Output Enable TIme, $\overline{OEn}$ to $\overline{Y}$ (Figures 2 and 4)	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $R_L = 1.0$ kΩ		6.8	10.5	1.0	12.5		15.0	ns
		$C_L = 50$ pF		9.3	14.0	1.0	16.0		19.0	
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $R_L = 1.0$ kΩ		4.7	7.2	1.0	8.5		10.5	
		$C_L = 50$ pF		6.2	9.2	1.0	10.5		13.0	
t_{PLZ}, t_{PHZ}	Output Disable Time, $\overline{OEn}$ to $\overline{Y}$ (Figures 2 and 4)	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 50$ pF $R_L = 1.0$ kΩ		11.2	15.4	1.0	17.5		20.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF $R_L = 1.0$ kΩ		6.0	8.8	1.0	10.0		11.5	
t_{OSLH}, t_{OSHL}	Output to Output Skew	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 50$ pF (Note 3)			1.5		1.5		2.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF (Note 3)			1.0		1.0		1.5	ns
C_{in}	Maximum Input Capacitance			4.0	10		10		10	pF
C_{out}	Maximum Three−State Output Capacitance (Output in High Impedance State)			6.0						pF

		Typical @ 25°C, $V_{CC} = 5.0$V	
C_{PD}	Power Dissipation Capacitance (Note 4)	17	pF

3. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

Symbol	Parameter	$T_A = 25°C$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.9	1.2	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	− 0.9	−1.2	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

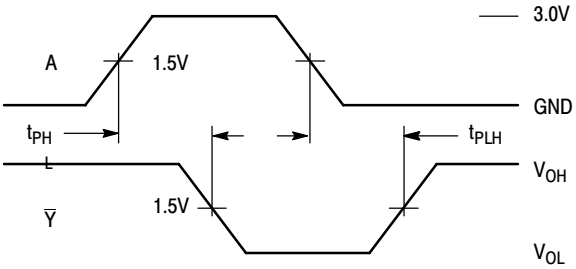


Figure 3. Switching Waveform

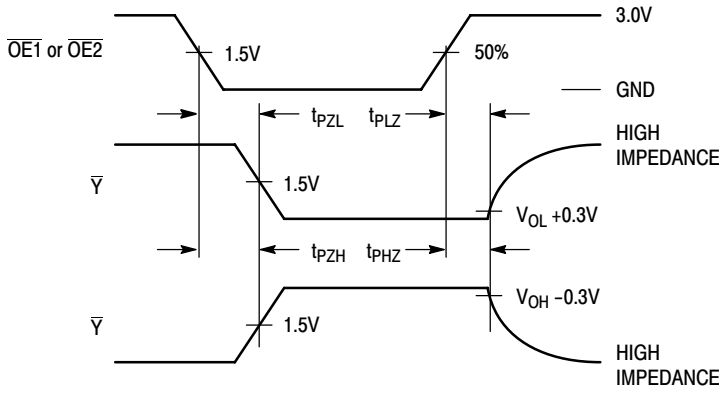
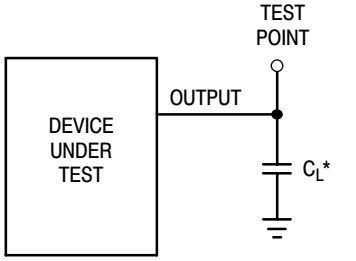
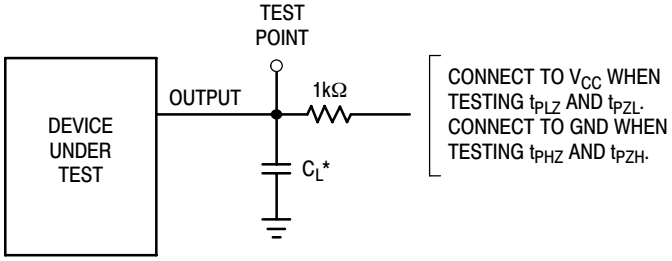


Figure 4. Switching Waveform



*Includes all probe and jig capacitance

Figure 5. Test Circuit

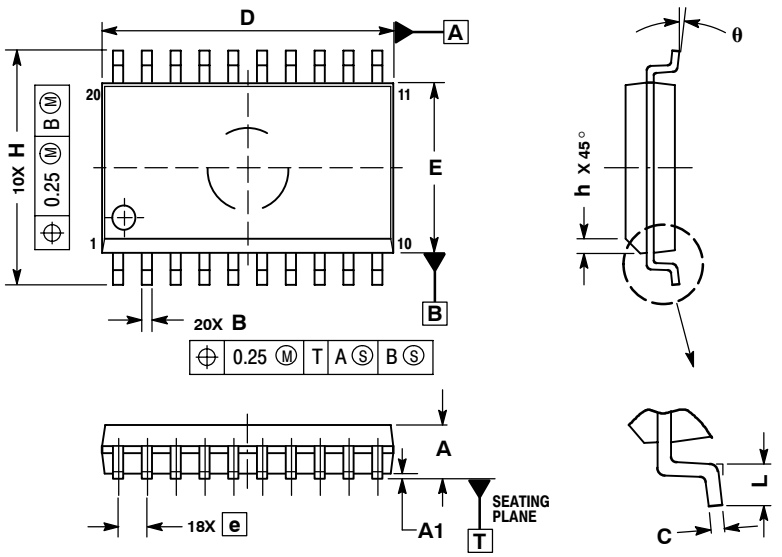


*Includes all probe and jig capacitance

Figure 6. Test Circuit

PACKAGE DIMENSIONS

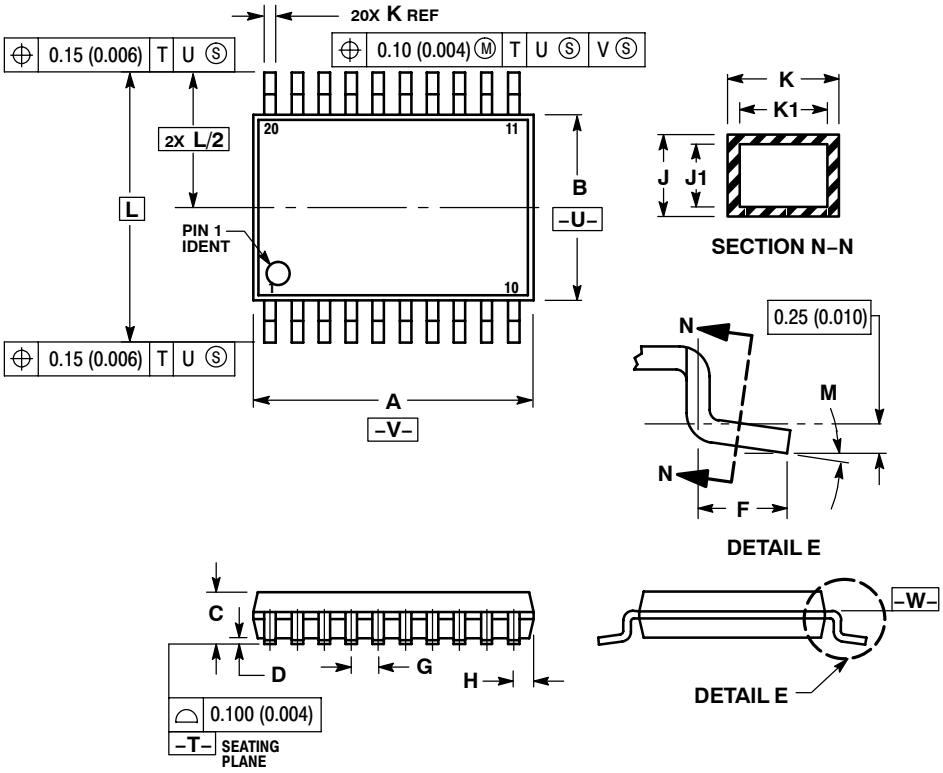
SOIC
DW SUFFIX
CASE 751D–05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

TSSOP
DT SUFFIX
CASE 948E–02
ISSUE A

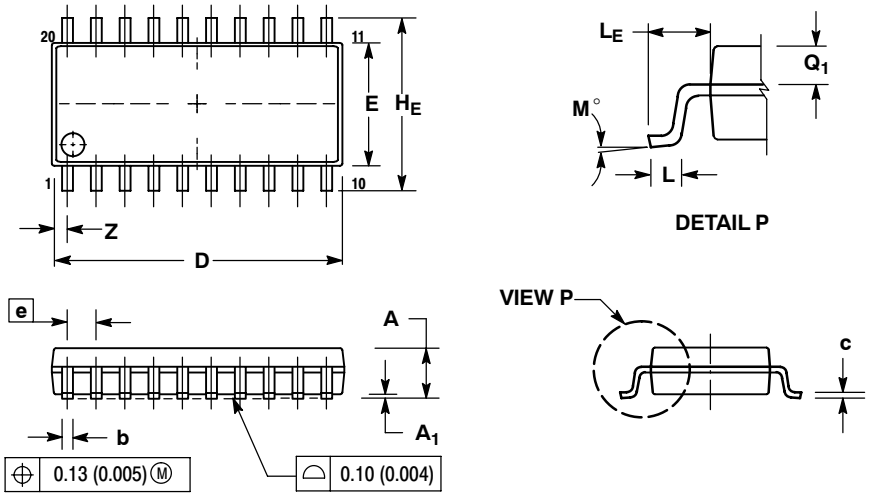


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OF PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

SOIC EIAJ
M SUFFIX
CASE 967−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

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