FAIRCHILD SEMICONDUCTOR®

RMPA2458
2.4–2.5 GHz InGaP HBT Low Current Linear Power Amplifier

Features

- 31.5dB small signal gain
- 27dBm output power @ 1dB compression
- 103mA total current at 19dBm modulated power out
- 2.5% EVM at 19 dBm modulated power out
- 3.3V collector supply operation
- 2.9V mirror supply operation
- Power saving shutdown options (bias control)
- Integrated power detector with 20dB dynamic range
- Lead-free RoHS compliant 3 x 3 x 0.9mm leadless package
- Internally matched to 50 Ohms and DC blocked RF input/output
- Optimized for use in 802.11b/g applications

General Description

The RMPA2458 power amplifier is designed for high performance WLAN applications in the 2.4–2.5 GHz frequency band. The low profile 16 pin 3 x 3 x 0.9 mm package with internal matching on both input and output to 50 Ohms minimizes next level PCB space and allows for simplified integration. The on-chip detector provides power sensing capability while the bias control provides power saving shutdown capability. The PA's industry leading low power consumption and excellent linearity are achieved using our InGaP Heterojunction Bipolar Transistor (HBT) technology.

Device

Electrical Characteristics[1] 802.11g OFDM Modulation

(176 μs burst time, 100 μs idle time) 54 Mbps Data Rate, 16.7 MHz Bandwidth

Parameter	Min	Typ	Max	Units
Frequency	2.4		2.5	GHz
Collector Supply Voltage	3.0	3.3	3.6	V
Mirror Supply Voltage		2.9		V
Mirror Supply Current		3.3		mA
Gain		31.5		dB
Total Current @ 19dBm P_{OUT}		103		mA
EVM @ 19dBm P_{OUT}[2]		2.5		%
Detector Output @ 19dBm P_{OUT}		340		mV
Detector Threshold[3]		5		dBm

Notes:

1. VC1, VC2, VC3 = 3.3V, VM123 = 2.9V, T_A = 25°C, PA is constantly biased, 50Ω system.
2. Percentage includes system noise floor of EVM = 0.8%.
3. P_{OUT} measured at P_{IN} corresponding to power detection threshold.

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Electrical Characteristics[1] 802.11b CCK Modulation (RF not framed) 11 Mbps Data Rate 22.0 MHz Bandwidth

Parameter	Min	Typ	Max	Units
Frequency	2.4		2.5	GHz
Collector Supply Voltage	3.0	3.3	3.6	V
Mirror Supply Voltage		2.9		V
Mirror Supply Current		3.3		mA
Gain		32		dB
Total Current @ 19dBm Pout		130		mA
First Side Lobe Power @ 19dBm Pout		-36		dBm
Second Side Lobe Power @ 19dBm Pout		-60		dBm
Max Pout Spectral Mask Compliance[2]		24		dBm
Detector Output @ 19dBm Pout		1.15		V
Detector Pout Threshold[3]		5		dBm

Electrical Characteristics[1] Single Tone

Parameter	Min	Typ	Max	Units
Frequency	2.4		2.5	GHz
Collector Supply Voltage	3.0	3.3	3.6	V
Mirror Supply Voltage (VM123)	2.6	2.9	3.1	V
Gain		31.5		dB
Total Quiescent Current		49		mA
Bias Current at pin VM123[4]		3.2		mA
P1dB Compression		27		dBm
Current @ P1dB Compression		600		mA
Shutdown Current (VM123 = 0V)		<1.0		µA
Input Return Loss		12		dB
Output Return Loss		9		dB
Detector Output at P1dB Compression		2.4		V
Detector Pout Threshold[3]		5		V
Turn-on Time[5]		<1.0		µS
Spurious (Stability)[6]		-65		dBc

Notes:

1. VC1, VC2, VC3 = 3.3V, VM123 = 2.9 Volts, Ta = 25°C, P_A is constantly biased, 50Ω system.
2. P_{IN} is adjusted to point where performance approaches spectral mask requirements.
3. P_{OUT} measured at P_{IN} corresponding to power detection threshold.
4. Mirror bias current is included in the total quiescent current.
5. Measured from Device On signal turn on to the point where RF P_{OUT} stabilizes to 0.5dB.
6. Load VSWR is set to 8:1 and the angle is varied 360 degrees. P_{OUT} = -30dBm to P1dB.

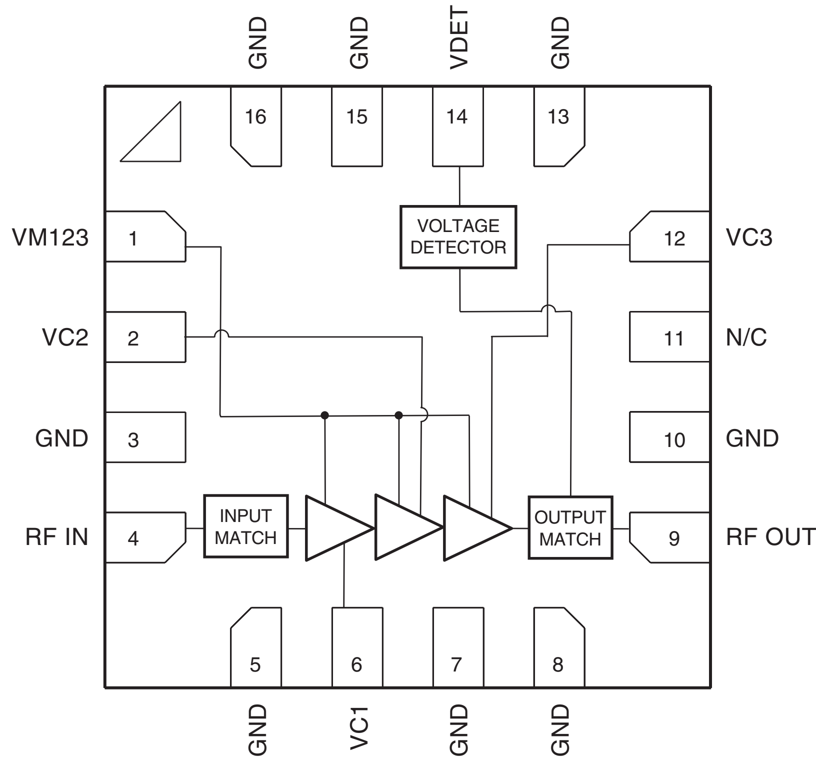
Absolute Ratings[1]

Symbol	Parameter	Ratings	Units
VC1, VC2, VC3	Positive Supply Voltage	5	V
IC1, IC2, IC3	Supply Current IC1 IC2 IC3	 50 150 700	 mA mA mA
VM123	Positive Bias Voltage	3.6	V
P_{IN}	RF Input Power	+5	dBm
T_{CASE}	Case Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C

Note:

1. No permanent damage with one parameter set at extreme limit. Other parameters set to typical values.

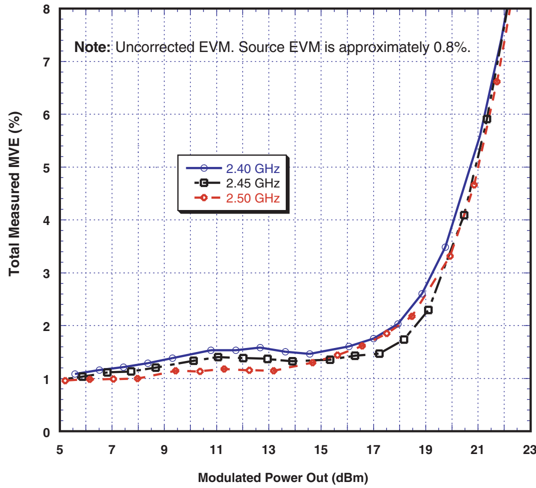
Functional Block Diagram

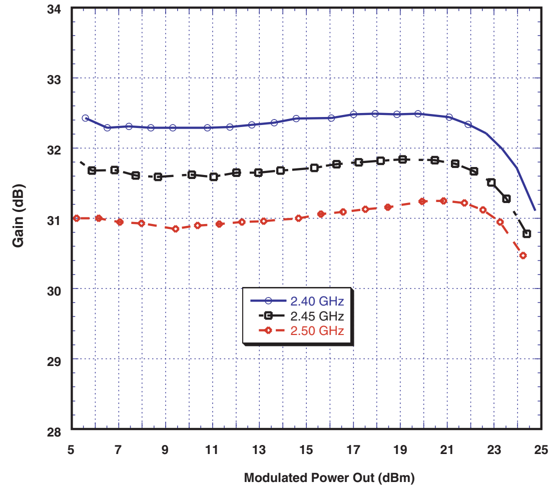


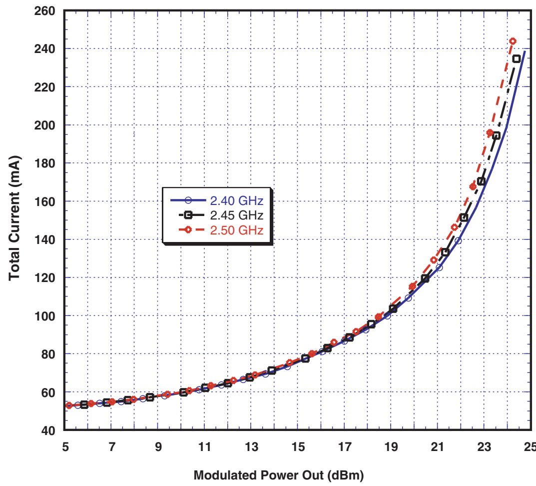
Pin	Description
1	VM123
2	VC2
3	GND
4	RF IN
5	GND
6	VC1
7	GND
8	GND
9	RF OUT
10	GND
11	N/C
12	VC3
13	GND
14	VDET
15	GND
16	GND

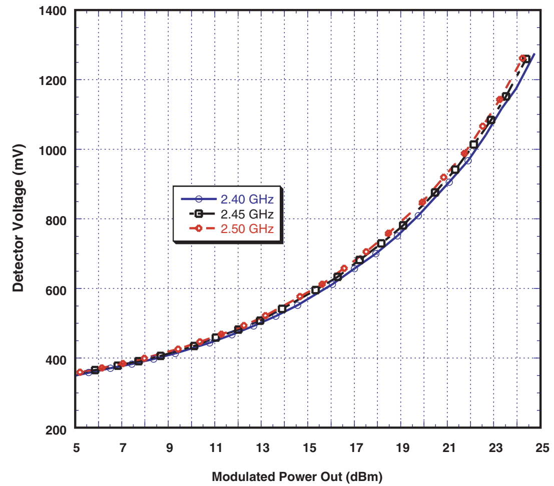
Performance Data 802.11g OFDM Modulation

(176 µs burst time, 100 µs idle time) 54 Mbps Data Rate, 16.7 MHz Bandwidth

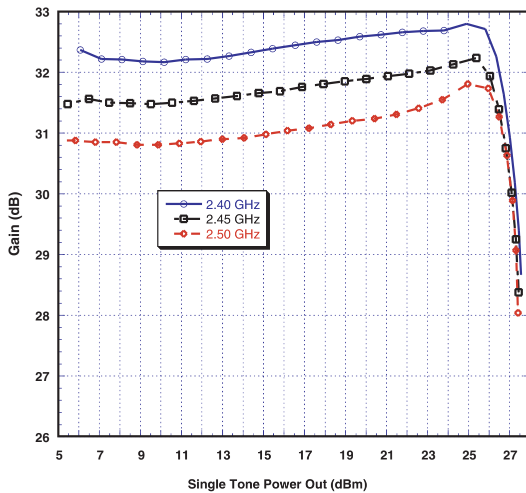


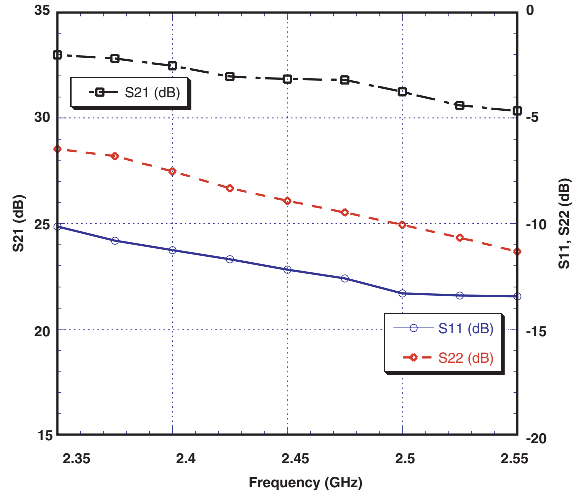




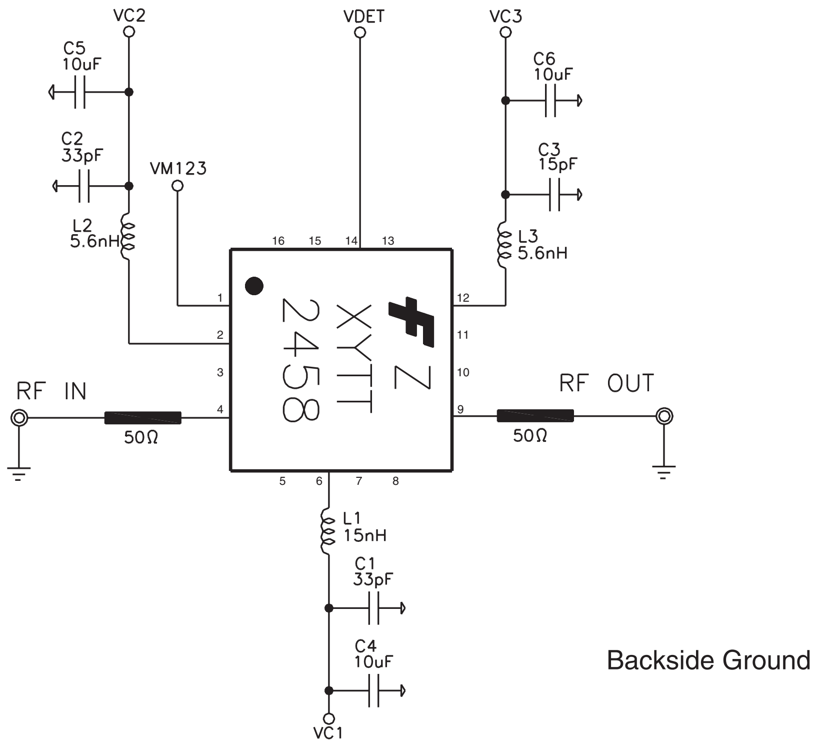


Single Tone

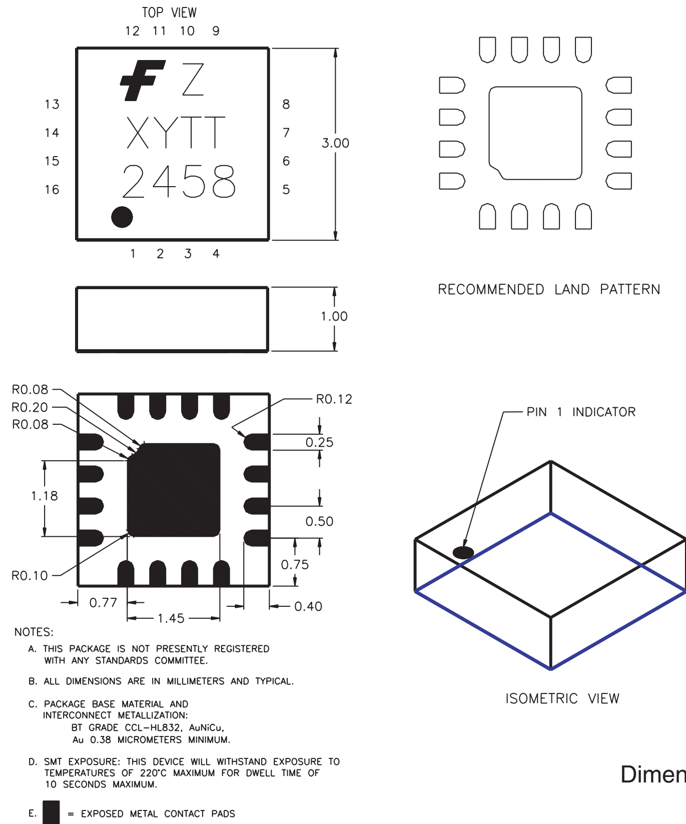




Evaluation Board Schematic



Package Outline



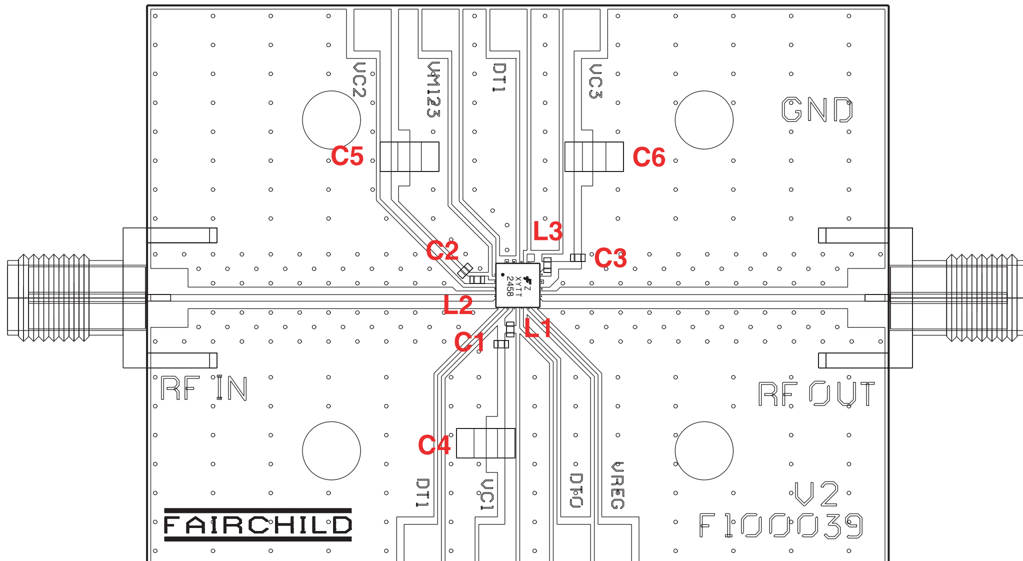
Dimensions in mm

Note: Dimensions do not include protrusions or mold flash. These are not to exceed 0.006" (.155mm) on any side.

Evaluation Board Bill of Materials

Qty	Item No.	Part Number	Description	Vendor
1	1	F100039	PC Board	Fairchild
2	2	#142-0701-841	SMA Connector	Johnson
7	3	#S1322-XX-ND	RT Angle Sgl M Header	Digikey
Ref	4	F1XXXXX	Assembly, RMPA2458	Fairchild
1	5 (C3)	06035A150J	15pF Capacitor	AVX
2	6 (C1, C2)	GRM39C0G330J50D500	33pF Capacitor	Murata
3	7 (C4, C5, C6)	CC1206JX5R106M	10μF Capacitor	TDK
2	8 (L2, L3)	LLV1005FB5N6S	5.6nH Inductor	Toko
1	9 (L1)	LLV1005FH15NK	15nH Inductor	Toko
A/R	10	SN63	Solder Paste	Indium Corp.
A/R	11	SN96	Solder Paste	Indium Corp.

Evaluation Board Layout



Actual Board Size = 2.0" X 1.5"

Evaluation Board Turn-On Sequence[1]

Recommended turn-on sequence:

1) Connect common ground terminal to the Ground (GND) pin on the board.

2) Connect voltmeter to pin DT1 (VDET, voltage detector).

3) Apply positive supply voltage VC1 (=3.3 V) to pin VC1 (first stage collector).

4) Apply positive supply voltage VC2 (=3.3 V) to pin VC2 (second stage collector).

5) Apply positive supply voltage VC3 (=3.3 V) to pin VC3 (third stage collector).

6) Apply positive bias voltage VM123 (=2.9 V) to pin VM123 (bias networks).

7) At this point, you should expect to observe the following positive currents flowing into the pins:

Pin	Current
VM123	1.0 – 5.0 mA
VC1	1.0 – 9.0 mA
VC2	5.0 – 25.0 mA
VC3	22.0 – 42.0 mA

8) Apply input RF power to SMA connector pin RFIN. Currents in pins VC1, VC2 and VC3 will vary depending on the input drive level.

9) Vary positive voltage on pin VM123 from +2.9 V to +0 V to shut down the amplifier or alter the power level. Shut down current flow into the pins:

Pin	Current
VC1	<1 nA
VC2	<1 nA
VC3	<1 nA

Recommended turn-off sequence:

Use reverse order described in the turn-on sequence above.

Note:

1. Turn on sequence is not critical and it is not necessary to sequence power supplies in actual system level design

Applications Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Precautions to Avoid Permanent Device Damage:

- Cleanliness: Observe proper handling procedures to ensure clean devices and PCBs. Devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC and ground contact areas.
- Device Cleaning: Standard board cleaning techniques should not present device problems provided that the boards are properly dried to remove solvents or water residues.
- Static Sensitivity: Follow ESD precautions to protect against ESD damage:
  - A properly grounded static-dissipative surface on which to place devices.
  - Static-dissipative floor or mat.
  - A properly grounded conductive wrist strap for each person to wear while handling devices.
- General Handling: Handle the package on the top with a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoiding damaging the RF, DC, and ground contacts on the package bottom. Do not apply excessive pressure to the top of the lid.
- Device Storage: Devices are supplied in heat-sealed, moisture-barrier bags. In this condition, devices are protected and require no special storage conditions. Once the sealed bag has been opened, devices should be stored in a dry nitrogen environment.

Device Usage:
Fairchild recommends the following procedures prior to assembly.

- Assemble the devices within one year of removal from the dry pack.
- During the one year period, the devices must be stored in an environment of less than 60% relative humidity and a maximum temperature of 30°C
- If the one year period or the environmental conditions have been exceeded, then the dry-bake procedure, at 125°C for 24 hours minimum, must be performed.

Solder Materials & Temperature Profile:
Reflow soldering is the preferred method of SMT attachment. Hand soldering is not recommended.

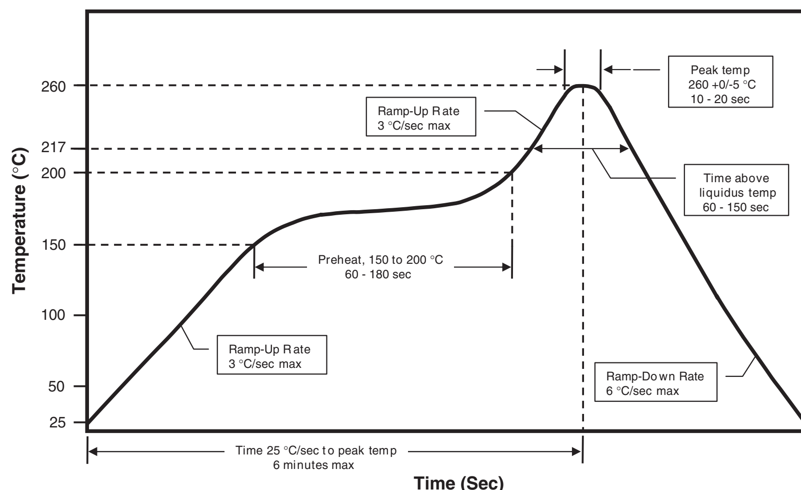
Reflow Profile

- Ramp-up: During this stage the solvents are evaporated from the solder paste. Care should be taken to prevent rapid oxidation (or paste slump) and solder bursts caused by violent solvent out-gassing. A maximum heating rate is 3°C/sec.
- Pre-heat/soak: The soak temperature stage serves two purposes; the flux is activated and the board and devices achieve a uniform temperature. The recommended soak condition is: 60-180 seconds at 150-200°C.
- Reflow Zone: If the temperature is too high, then devices may be damaged by mechanical stress due to thermal mismatch or there may be problems due to excessive solder oxidation. Excessive time at temperature can enhance the formation of inter-metallic compounds at the lead/board interface and may lead to early mechanical failure of the joint. Reflow must occur prior to the flux being completely driven off. The duration of peak reflow temperature should not exceed 20 seconds. Soldering temperatures should be in the range 255–260°C, with a maximum limit of 260°C.
- Cooling Zone: Steep thermal gradients may give rise to excessive thermal shock. However, rapid cooling promotes a finer grain structure and a more crack-resistant solder joint. The illustration below indicates the recommended soldering profile.

Solder Joint Characteristics:
Proper operation of this device depends on a reliable void-free attachment of the heat sink to the PWB. The solder joint should be 95% void-free and be a consistent thickness.

Rework Considerations:
Rework of a device attached to a board is limited to reflow of the solder with a heat gun. The device should be subjected to no more than 15°C above the solder melting temperature for no more than 5 seconds. No more than 2 rework operations should be performed.

Recommended Solder Reflow Profile



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Rev. I16