## APPLICATIONS

$\checkmark$ Ethernet-10 Base T
$\checkmark$ Cellular Phones
$\checkmark$ Handheld Electronics
$\checkmark$ FireWire \& USB Interfaces
$\boldsymbol{\checkmark}$ Multiple I/O Ports or Power Supplies

## IEC COMPATIBILITY (ENG1DOD-4)

$\checkmark$ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
$\checkmark$ 61000-4-4 (EFT): 40A - 5/50ns
$\checkmark$ 61000-4-5 (Surge): 12A, 8/20 $\mu$ s Level 1(Line-Gnd) \& Level 2(Line-Line)


## FEATURES

, 200 Watts Peak Pulse Power per Line ( $\mathrm{tp}=8 / 20 \mu \mathrm{~s}$ )
$\checkmark$ Monolithic Design
$\checkmark$ Available in Multiple Voltage Types Ranging From 5V to 24 V
$\checkmark$ Protect 4 Bidirectional Lines \& 5 Unidirectional Lines
$\checkmark$ ESD Protection $>25$ kilovolts
$\checkmark$ Low Clamping Voltage
$\checkmark$ Unidirectional \& Bidirectional Configurations
$\checkmark$ Low Leakage Current
$\checkmark$ RoHS Compliant in Lead-Free Versions

## MECHANICAL CHARACTERISTICS

$\checkmark$ Molded JEDEC SOT-23-6 Package
$\checkmark$ Weight 16 milligrams (Approximate)
$\checkmark$ Available in Tin-Lead or Lead-Free Pure-Tin Plating(Annealed)
$\checkmark$ Solder Reflow Temperature:
Tin-Lead - Sn/Pb, 85/15: 240-245 ${ }^{\circ} \mathrm{C}$
Pure-Tin - Sn, 100: $260-270^{\circ} \mathrm{C}$
Flammability rating UL 94V-0
$\checkmark 8 \mathrm{~mm}$ Tape and Reel Per EIA Standard 481
$\checkmark$ Marking: Marking Code \& Pin One Defined By DOT on Package

## PIN CONFIGURATIONS

UNIDIRECTIONAL


BIDIRECTIONAL


## DEVICE CHARACTERISTICS

| MAXIMUM RATINGS @ $25^{\circ} \mathrm{C}$ Unless Otherwise Specified |  |  |  |
| :--- | :---: | :---: | :---: |
| PARAMETER | SYMBOL | VALUE | UNITS |
| Peak Pulse Power $\left(\mathrm{t}_{\mathrm{p}}=8 / 20 \mu \mathrm{~s}\right)-$ See Figure 1 | $\mathrm{P}_{\mathrm{PP}}$ | 200 | Watts |
| OperatingTemperature | $\mathrm{T}_{J}$ | $-55^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {STG }}$ | $-55^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$ | ${ }^{\circ} \mathrm{C}$ |


| ELECTRICAL CHARACTERISTICS PER LINE @ $25^{\circ} \mathrm{C}$ Unless Otherwise Specified |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PART NUMBER (See Notes 1-3) | DEVICE <br> MARKING | RATED STAND-OFF VOLTAGE | MINIMUM BREAKDOWN VOLTAGE | MAXIMUM CLAMPING VOLTAGE (See Fig. 2) | MAXIMUM CLAMPING VOLTAGE (See Fig. 2) | MAXIMUM LEAKAGE CURRENT | TYPICAL CAPACITANCE |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{wn}} \\ & \text { voLTS } \end{aligned}$ | @ 1mA $\mathrm{V}_{\text {(BRI }}$ VOLTS | $\begin{gathered} @ \mathrm{I}_{\mathrm{p}}=1 \mathrm{~A} \\ \mathrm{~V}_{\mathrm{c}} \\ \text { VOLTS } \end{gathered}$ | $\begin{aligned} & @ 8 / 20 \mu \mathrm{~s} \\ & \mathrm{~V}_{\mathrm{c}} @ \mathrm{l}_{\mathrm{pp}} \\ & \hline \end{aligned}$ |  | $\begin{gathered} @ 0 \mathrm{~V}, 1 \mathrm{MHz} \\ \mathrm{C}_{\mathrm{j}} \\ \mathrm{pF} \\ \hline \end{gathered}$ |
| CP05 | QRH | 5.0 | 6.0 | 9.8 | 11.8V @ 17.0A | 20 | 70 |
| CP05C | QRL | 5.0 | 6.0 | 9.8 | 11.8V @ 17.0A | 20 | 70 |
| CP12 | QRI | 12.0 | 13.3 | 19 | 28.3V @ 7.0A | 1 | 50 |
| CP12C | QRM | 12.0 | 13.3 | 19 | 28.3V @ 7.0A | 1 | 50 |
| CP15 | QRJ | 15.0 | 16.7 | 24 | 45.0V @ 5.0A | 1 | 30 |
| CP15C | QRN | 15.0 | 16.7 | 24 | 45.0V @ 5.0A | 1 | 30 |
| CP24 | QRK | 24.0 | 26.7 | 43 | 65.0V @ 3.0A | 1 | 25 |
| CP24C | QRO | 24.0 | 26.7 | 43 | 65.0 V @ 3.0A | 1 | 25 |

Note 1: Part numbers with an additional "C" suffix are bidirectional devices, i.e., CP05C.
Note 2: Unidirectional Only: Test between pin 1, 3, 4 and 6 to pin 2 or 5.
Note 3: Bidirectional Only: Test between pin 5 to 1 or 3 or 4 or 6 . Electrical characteristics apply in both directions.

FIGURE 1
PEAK PULSE POWER VS PULSE TIME


FIGURE 2


GRAPHS


FIGURE 4 OVERSHOOT \& CLAMPING VOLTAGE FOR CP05


ESD Test Pulse: 25 kilovolt, $1 / 30 \mathrm{~ns}$ (waveshape)

FIGURE 5


FIGURE 6
TYPICAL REVERSE VOLTAGE VS CAPACITANCE FOR CP05C


# CPO5 <br> thru <br> CP24C 

## APPLICATION NDTE

The CP Series are TVS arrays designed to protect I/O or data lines from the damaging effects of ESD or EFT. This product series provides both unidirectional and bidirectional protection, with a surge capability of 200 Watts $P_{p P}$ per line for an $8 / 20 \mu \mathrm{~s}$ waveform and ESD protection $>25$ kilovolts.

## UNIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 1)

The CP Series provides up to four (4) lines of protection in a common-mode configuration as depicted in Figure 1.

Circuit connectivity is as follows:
$\checkmark$ Line 1 is connected to Pin 1
$\checkmark$ Line 2 is connected to Pin 3 .
$\checkmark \quad$ Line 3 is connected to Pin 4.
$\checkmark$ Line 4 is connected to Pin 6
$\checkmark \quad$ Pin 5 is connected to ground.
$\checkmark \quad$ Pin 2 is not connected.

## BIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 2)

The CPxxC Series provides up to four (4) lines of protection in a common-mode configuration as depicted in Figure 2.

Circuit connectivity is as follows:
v Line 1 is connected to Pin 1.
$\checkmark \quad$ Line 2 is connected to Pin 3.
$\checkmark$ Line 3 is connected to Pin 4
$\checkmark$ Line 4 is connected to Pin 5 .
$\checkmark$ Pin 6 is connected to ground.
$\checkmark$ Pin 2 is not connected.
Figure 1 - Unidirectional Configuration Common-Mode I/O Port Protection


## CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:
$\checkmark$ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
$\checkmark$ The path length between the TVS device and the protected line should be minimized.
$\checkmark$ All conductive loops including power and ground loops should be minimized.
$\checkmark$ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
$\checkmark$ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Figure 2 - Bidirectional Configuration Common-Mode I/O Port Protection


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## ProTek Devices

2929 South Fair Lane, Tempe, AZ 85282
Tel: 602-431-8101 Fax: 602-431-2288
E-Mail: sales@protekdevices.com Web Site: www.protekdevices.com

