AKD4631-VN
AK4631-VN Evaluation board Rev.0

GENERAL DESCRIPTION

AKD4631-VN is an evaluation board for the AK4631VN, 16bit mono CODEC with MIC/SPK amplifier. The AKD4631-VN can evaluate A/D converter and D/A converter separately in addition to loopback mode (A/D → D/A). AKD4631-VN also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4631-VN --- Evaluation board for AK4631VN
(Cable for connecting with printer port of IBM-AT, compatible PC and control software are packed with this. This control software does not support Windows NT.)

FUNCTION

- **DIT/DIR with optical input/output**
- **BNC connector for an external clock input**
- **10pin Header for serial control mode**

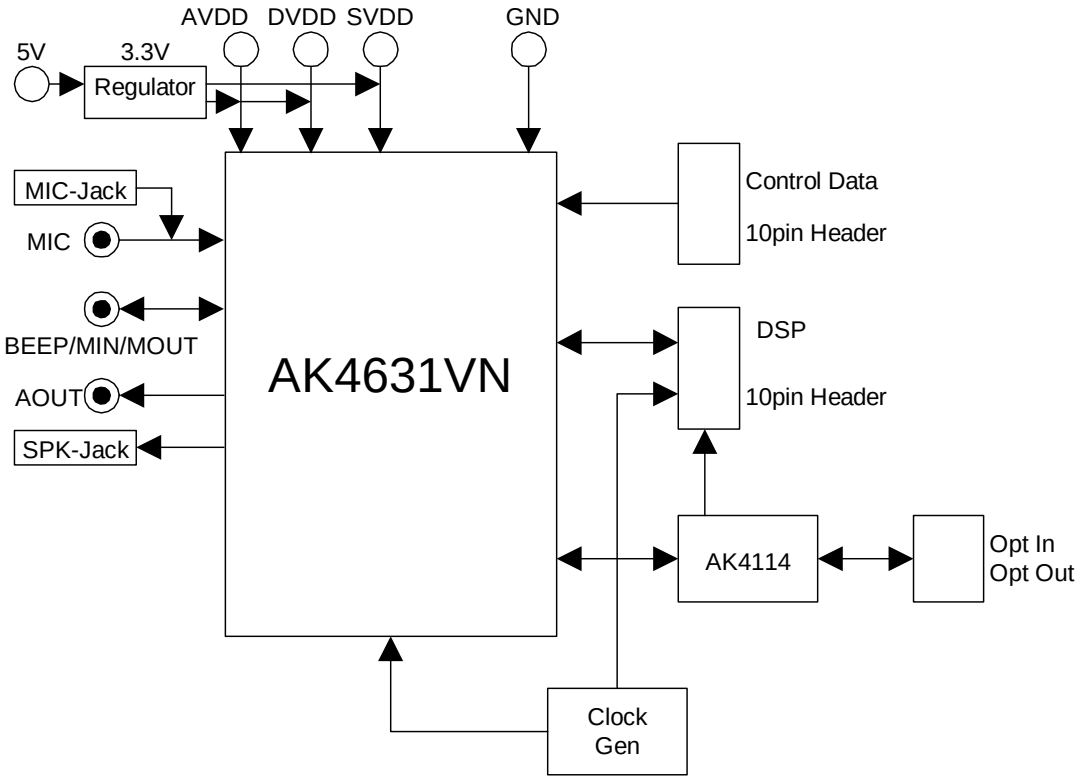


Figure 1. AKD4631-VN Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

Evaluation Board Manual

■ Operation sequence

1) Set up the power supply lines.

1-1) When AVDD, DVDD, SVDD, and VCC are supplied from the regulator. (AVDD, DVDD, SVDD, and VCC jack should be open.). See "**Other jumper pins set up** (page 10)". <default>

[REG]	(red)	= 5V	
[AVDD]	(orange)	= open	: 3.3V is supplied to AVDD of AK4631-VN from regulator.
[DVDD]	(orange)	= open	: 3.3V is supplied to DVDD of AK4631-VN from regulator.
[SVDD]	(blue)	= open	: 3.3V is supplied to SVDD of AK4631-VN from regulator.
[VCC]	(orenge)	= open	: 3.3V is supplied to logic block from regulator.
[AVSS]	(black)	= 0V	: for analog ground
[AGND]	(black)	= 0V	: for analog ground
[DGND]	(black)	= 0V	: for logic ground

1-2) When AVDD, DVDD, SVDD, and VCC are not supplied from the regulator. (AVDD, DVDD, SVDD, and VCC jack should be junction.) See "**Other jumper pins set up** (page 10)".

[REG]	(red)	= "REG" jack should be open.
[AVDD]	(orange)	= 2.6 ~ 3.6V : for AVDD of AK4631-VN (typ. 3.3V)
[DVDD]	(orange)	= 2.6 ~ 3.6V : for DVDD of AK4631-VN (typ. 3.3V)
[SVDD]	(blue)	= 2.6 ~ 5.25V: for SVDD of AK4631-VN (typ. 3.3V, 5.0V)
[VCC]	(orenge)	= 2.6 ~ 3.6V : for logic (typ. 3.3V)
[AVSS]	(black)	= 0V : for analog ground
[AGND]	(black)	= 0V : for analog ground
[DGND]	(black)	= 0V : for logic ground

Each supply line should be distributed from the power supply unit.
AVDD and DVDD must be same voltage level.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.
The AK4631VN and AK4114 should be reset once bringing SW1, 2 "L" upon power-up.

■ Evaluation mode

In case of AK4631VN evaluation using AK4114, it is necessary to correspond to audio interface format for AK4631VN and AK4114. About AK4631VN's audio interface format, refer to datasheet of AK4631VN. About AK4114's audio interface format, refer to Table 2 in this manual.

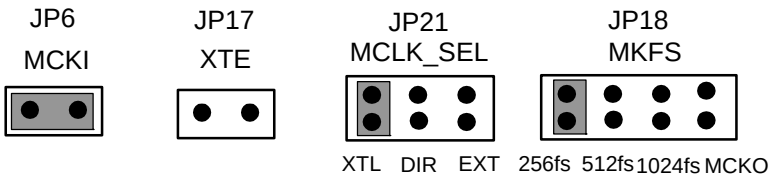
Applicable Evaluation Mode

(1) Evaluation of loop-back mode (A/D → D/A) : PLL, Master Mode (Default)
(2) Evaluation of loop-back mode (A/D → D/A) : PLL, Slave Mode (PLL Reference CLOCK: MCKI pin)
(3) Evaluation of loop-back mode (A/D → D/A) : PLL, Slave Mode (PLL Reference CLOCK: BICK or FCK pin)
(4) Evaluation of using DIR of AK4114 (opt-connector) : EXT, Slave Mode
(5) Evaluation of using DIT of AK4114 (opt-connector) : EXT, Slave Mode

(1) Evaluation of loop-back mode (A/D → D/A) : PLL, Master Mode (Default)

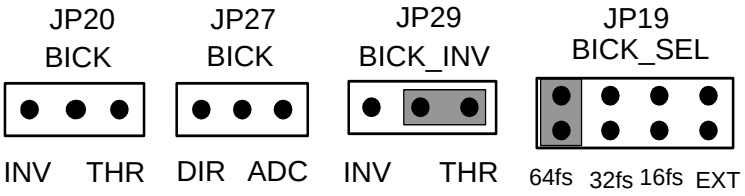
a) Set up jumper pins of MCKI clock

"MCKPD bit" in the AK4631-VN should be set to "0".
X'tal of 11.2896MHz, 12MHz, 12.288MHz, 13MHz, 24MHz or 27MHz can be set in X2. X'tal of 11.2896MHz (Default) is set on the AKD4631-VN. Set "No.8 of SW3" to "H".
When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 24MHz or 27MHz) through a RCA connector (J8: EXT/BICK) is supplied, select EXT on JP21 (MCLK_SEL) and short JP17 (XTE). JP23 (EXT1) and R26 should be properly selected in order to much the output impedance of the clock generator.

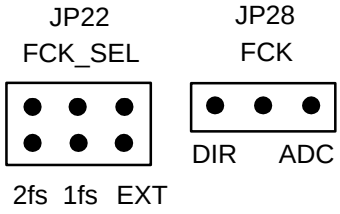


b) Set up jumper pins of BICK clock

Output frequency (16fs/32fs/64fs) of BICK should be set by "BCKO1-0 bit" in the AK4631-VN.
There is no necessity for set up JP19.

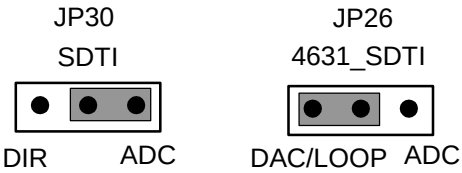


c) Set up jumper pins of FCK clock



d) Set up jumper pins of DATA

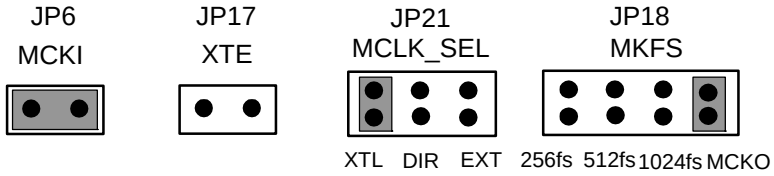
When the AK4631VN is evaluated by loop-back mode (A/D → D/A), the jumper pins should be set to the following.



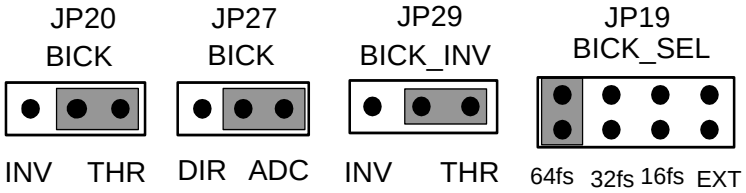
(2) Evaluation of loop-back mode (A/D → D/A) : PLL, Slave Mode (PLL Reference CLOCK: MCKI pin)

a) Set up jumper pins of MCKI clock

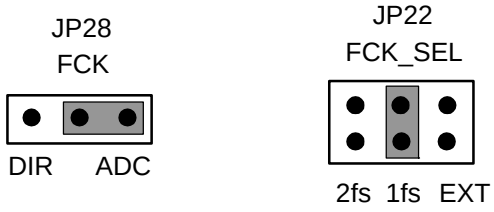
"MCKPD bit" in the AK4631VN should be set to "0".
X'tal of 11.2896MHz (Default) is set on the AKD4631-VN. In this case, the AK4631VN corresponds to PLL reference clock of 12.2896MHz. In this evaluation mode, the output clock from MCKO-pin of the AK4631VN is supplied to a divider (U3: 74VHC4040), BICK and FCK clocks are generated by the divider. Then "MCKO bit" in the AK4631VN should be set to "1". When an external clock through a RCA connector (J8: EXT/BICK) is supplied, select EXT on JP21 (MCLK_SEL) and short JP17 (XTE). JP23 (EXT1) and R26 should be properly selected in order to match the output impedance of the clock generator.



b) Set up jumper pins of BICK clock



c) Set up jumper pins of FCK clock



d) Set up jumper pins of DATA

When the AK4631-VN is evaluated by loop-back mode (A/D → D/A), the jumper pins should be set to the following.

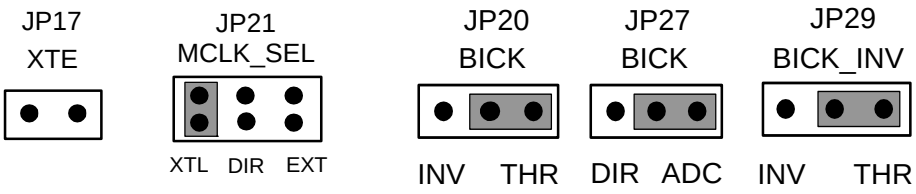
(3) Evaluation of loop-back mode (A/D → D/A) : PLL, Slave Mode (PLL Reference CLOCK: BICK or FCK pin)

a) Set up jumper pins of MCKI clock

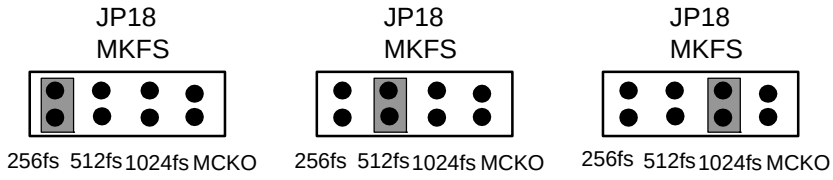
"MCKPD bit" in the AK4631VN should be set to "1". JP6 (MCKI) should be open.

b) Set up jumper pins of BICK clock

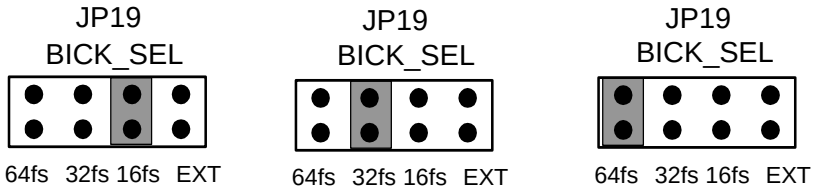
When an external clock through a RCA connector J8 (EXT/BICK) is supplied, select EXT on JP19 (MCLK_SEL) and short JP17 (XTE). JP23 (EXT1) and R26 should be properly selected in order to match the output impedance of the clock generator.



In this evaluation mode, the selected clock from JP21 (MCLK_SEL) is supplied to a divider (U3: 74VHC4040), BICK and FCK clocks are generated by the divider. Input frequency of master clock is set up in turn "256fs", "512fs", "1024fs" from left.

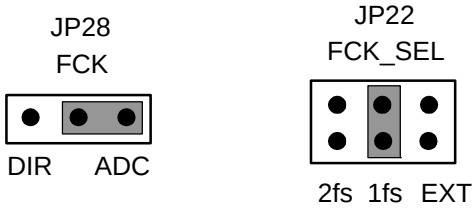


And input frequency of BICK is set up in turn "16fs", "32fs", "64fs" from left.



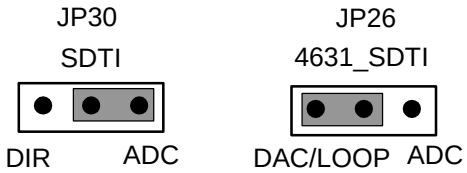
c) Set up jumper pins of FCK clock

When an external clock through a RCA connector J9 (FCK) is supplied, select EXT on JP22 (FCK_SEL). JP24 (EXT2) and R27 should be properly selected in order to match the output impedance of the clock generator.



d) Set up jumper pins of DATA

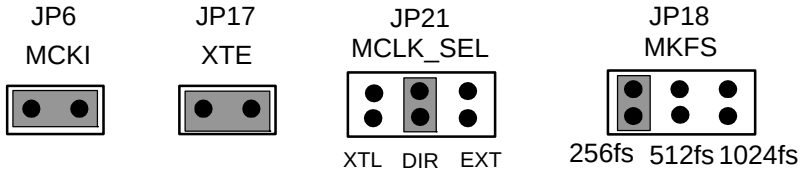
When the AK4631VN is evaluated by loop-back mode (A/D → D/A), the jumper pins should be set to the following.



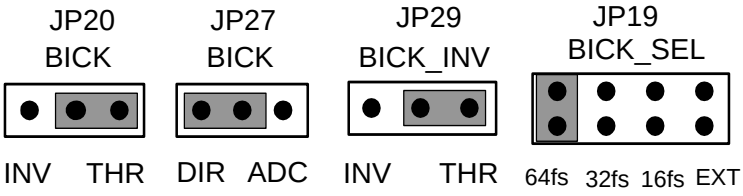
(4) Evaluation of using DIR of AK4114 (opt-connector) : EXT, Slave Mode

a) Set up jumper pins of MCKI clock

"MCKPD bit" in the AK4631VN should be set to "0".

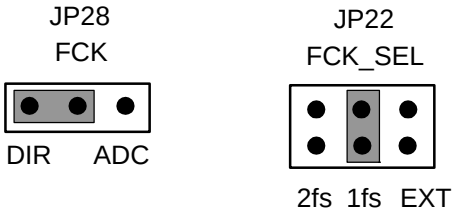


b) Set up jumper pins of BICK clock



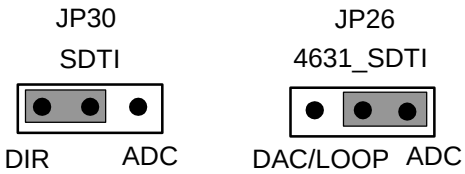
c) Set up jumper pins of FCK clock

JP24 (EXT2) and R27 should be properly selected in order to match the output impedance of the clock generator.



d) Set up jumper pins of DATA

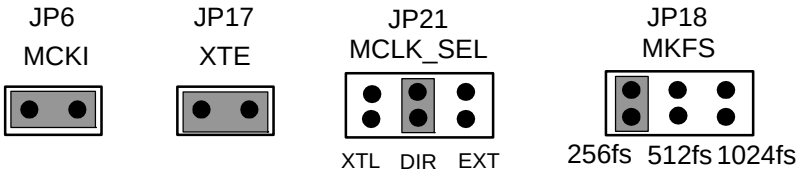
When D/A converter of the AK4631-VN is evaluated by using DIR of AK4114, the jumper pins should be set to the following.



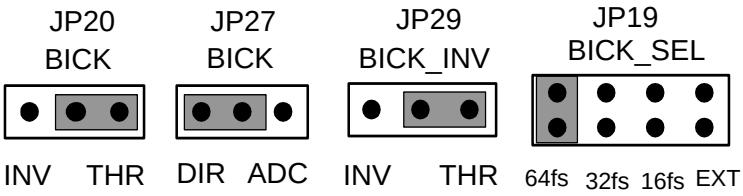
(5) Evaluation of using DIT of AK4114 (opt-connector) : EXT, Slave Mode

a) Set up jumper pins of MCKI clock

"MCKPD bit" in the AK4631-VN should be set to "0".

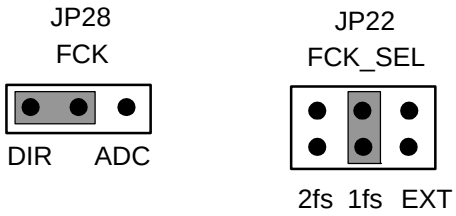


b) Set up jumper pins of BICK clock



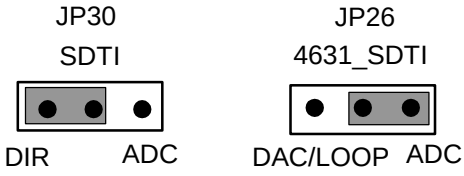
c) Set up jumper pins of FCK clock

JP24 (EXT2) and R27 should be properly selected in order to match the output impedance of the clock generator.



d) Set up jumper pins of DATA

When A/D converter of the AK4631-VN is evaluated by using DIR of AK4114, the jumper pins should be set to the following.



■ DIP Switch set up

[SW3] (MODE) : Mode Setting of AK4631-VN and AK4114
ON is "H", OFF is "L".

No.	Name	ON ("H")	OFF ("L")
1	DIF0	AK4114 Audio Format Setting See Table 2	
2	DIF1		
3	CM2		
4	CM0	Clock Operation Mode select See Table 3	
5	CM1		
6	OCKS0	Master Clock Frequency Select See Table 4	
7	OCKS1		
8	M/S	Master mode	Slave mode

Note. When the AK4631-VN is evaluated Master mode, "No.8 of SW3" is set to "H".
Table 1. Mode Setting for AK4631-VN and AK4114

Resistor setting for AK4631-VN Audio Interface Format		Setting for AK4114 Audio Interface Format					
DIF1 bit	DIF0 bit	DIF0	DIF1	DIF2	DAUX	SDTO	
0	1	L	L	L	24bit, Left justified	16bit, Right justified	
1	0	L	L	H	24bit, Left justified	24bit, Left justified	Default
1	1	H	L	H	24bit, I^2S	24bit, I^2S	

Note. When the AK4631-VN is evaluated by using DIR/DIT of AK4114, "No.8 of SW3" is set to "L".
Table 2. Setting for AK4114 Audio Interface Format

Mode	CM1	CM0	UNLOCK	PLL	X'tal	Clock source	SDTO	
0	0	0	-	ON	ON(Note)	PLL	RX	
1	0	1	-	OFF	ON	X'tal	DAUX	
2	1	0	0	ON	ON	PLL	RX	Default
			1	ON	ON	X'tal	DAUX	
3	1	1	-	ON	ON	X'tal	DAUX	

ON: Oscillation (Power-up), OFF: STOP (Power-down)
Note : When the X'tal is not used as clock comparison for fs detection (i.e. XTL1,0= "1,1"), the X'tal is off. Default setting is recommended.

Table 3. Clock Operation Mode select

No.	OCKS1	MCKO1	MCKO2	X'tal	
0	0	256fs	256fs	256fs	Default
2	1	512fs	256fs	512fs	

Table 4. Master Clock Frequency Select (Stereo mode)

■ Other jumper pins set up

1. JP1 (GND) : Analog ground and Digital ground
   - OPEN : Separated.
   - SHORT : Common. (The connector “DGND” can be open.) <Default>

2. JP2 (AIN) : Connection between MICOUT pin and AIN pin of the AK4631VN.
   - OPEN : No connection.
   - SHORT : Connection. <Default>

3. JP3 (AVDD_SEL) : AVDD of the AK4631VN
   - REG : AVDD is supplied from the regulator (“AVDD” jack should be open). < Default >
   - AVDD : AVDD is supplied from “AVDD ” jack.

4. JP9 (DVDD_SEL) : DVDD of the AK4631VN
   - AVDD : DVDD is supplied from “AVDD”. < Default >
   - DVDD : DVDD is supplied from “DVDD ” jack.

5. JP10 (LVC_SEL) : Logic block of LVC is selected supply line.
   - DVDD : Logic block of LVC is supplied from “DVDD”. < Default >
   - VCC : Logic block of LVC is supplied from “VCC ” jack.

6. JP11 (VCC_SEL) : Logic block is selected supply line.
   - LVC : Logic is supplied from supply line of LVC. < Default >
   - VCC : Logic block of LVC is supplied from “VCC ” jack.

7. JP4 (SVDD_SEL) : SVDD of the AK4631VN
   - REG : SVDD is supplied from the regulator (“SVDD” jack should be open). < Default >
   - SVDD : SVDD is supplied from “SVDD ” jack.

8. JP8 (MCKO_SEL) : Master Clock Frequency is selected clock from MCKO1 or MCKO2 of the AK4114.
   - MCKO1 : The check from MCKO1 of AK4114 is provided to MCKI of the AK4631VN. < Default >
   - MCKO2 : The check from MCKO2 of AK4114 is provided to MCKI of the AK4631VN.

■ The function of the toggle SW

[SW1] (DIR) : Power control of AK4114. Keep “H” during normal operation.
Keep “L” when AK4114 is not used.

[SW2] (PDN) : Power control of AK4631VN. Keep “H” during normal operation.

■ Indication for LED

[LED1] (ERF): Monitor INT0 pin of the AK4114. LED turns on when some error has occurred to AK4114.

■ Serial Control

The AK4631-VN can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT2 (CTRL) with PC by 10 wire flat cable packed with the AKD4631-VN

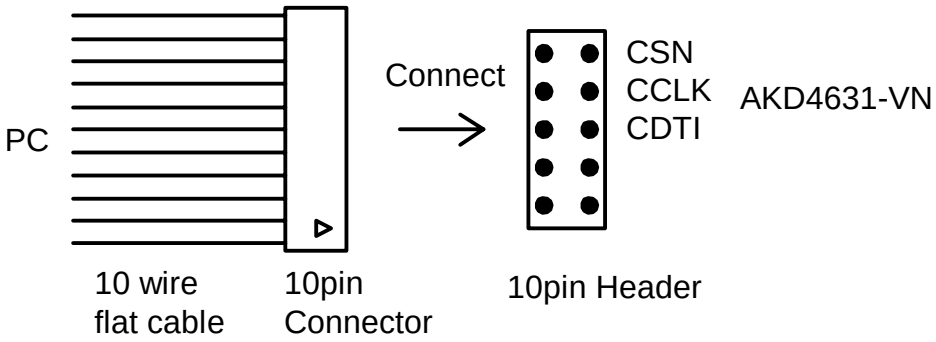


Figure 2. Connect of 10 wire flat cable

■ Analog Input / Output Circuits

(1) Input Circuits

a) MIC Input Circuit

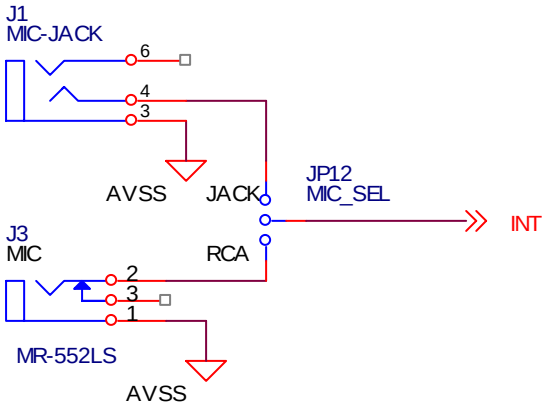
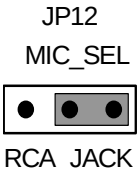
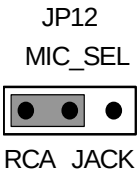


Figure 3. MIC Input Circuit

(a-1) Analog signal is input to MIC pin via J1 connector.



(a-2) Analog signal is input to MIC pin via J3 connector.



(2) Output Circuits

a) AOUT Output Circuit

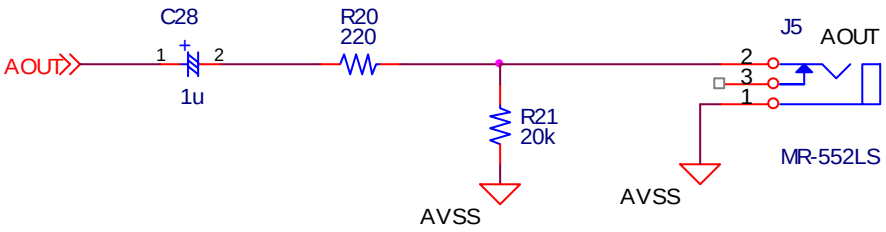


Figure 4. AOUT Output Circuit

b) SPK Output Circuit

Note. When mini-jack is inserted or pulled out J2 (SPK-JACK) connector, JP13 (SPP_SEL) and JP14 (SPN_SEL) should be open, or “PMSPK bit” in the AK4631-VN should be set to “0”.

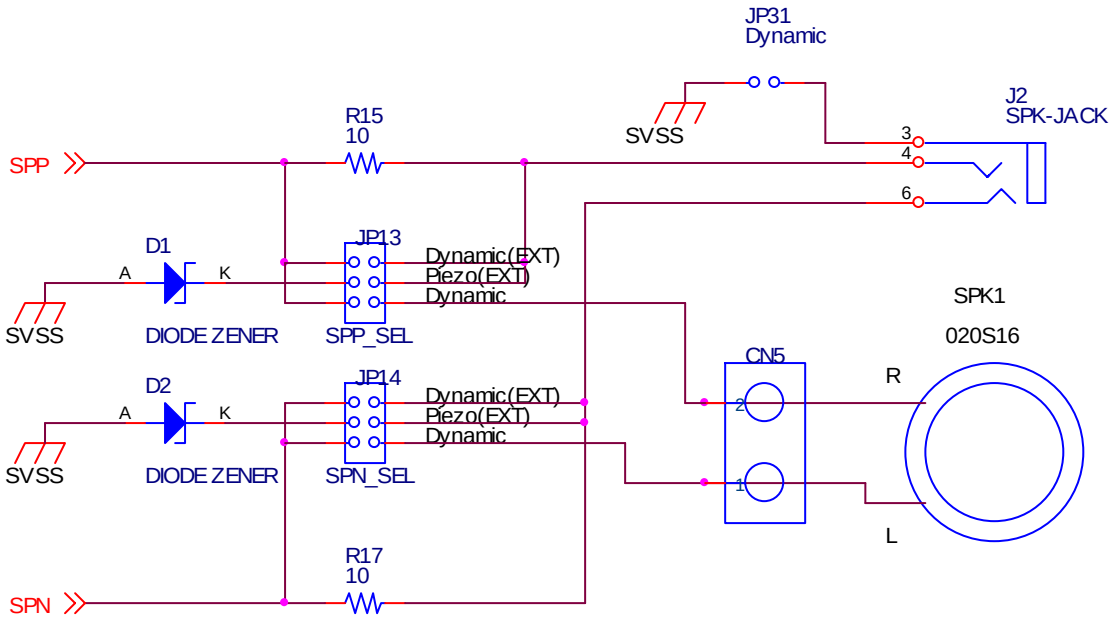
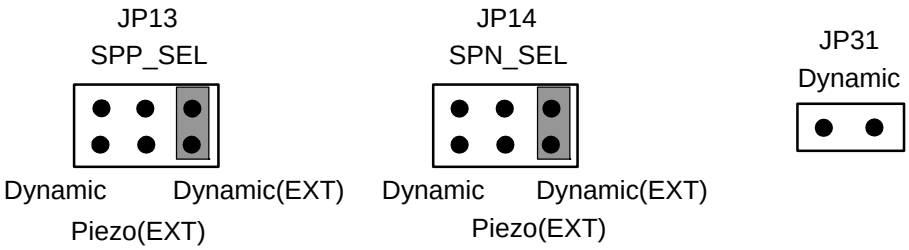
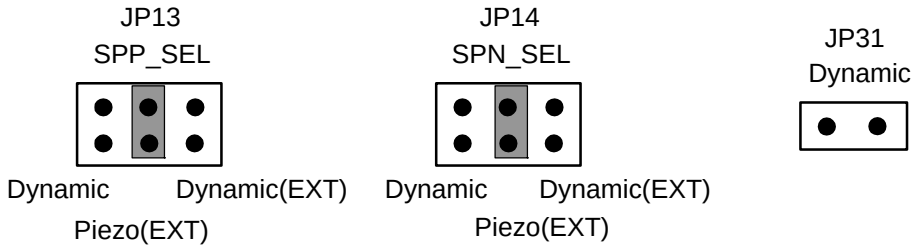


Figure 5. SPK Output Circuit

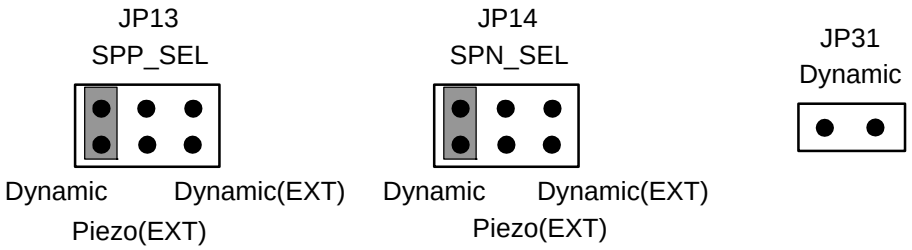
(b-1) An external dynamic speaker is evaluated by using J2 (SPK-JACK) connector.



(b-2) An external Piezo speaker is evaluated by using J2 (SPK-JACK) connector.



(b-3) Analog signal of SPP/SPN pins are output from "Dynamic Speaker" on the evaluation (SPK1).



(3) BEEP/MIN/MOUT Input and Output Circuit

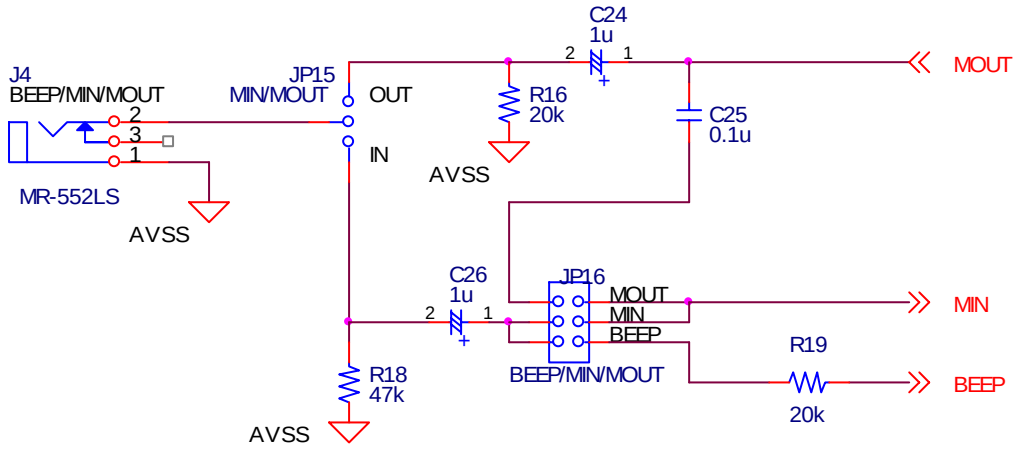
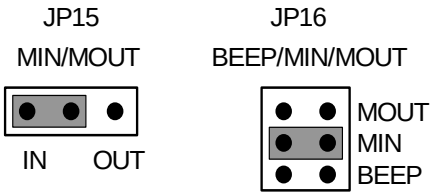
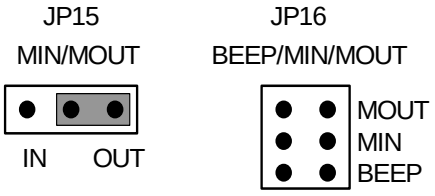


Figure 6. BEEP/MIN/MOUT Input and Output Circuit

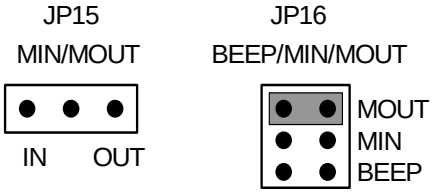
(3-1) Analog signal is input to MIN pin from J4 connector.



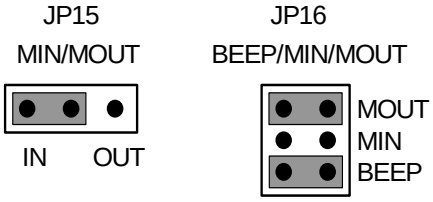
(3-2) Analog signal of MOUT pin is output from J4 connector.



(3-3) Analog signal of MOUT pin is input to MIN pin.



(3-4) Analog signal is input to BEEP pin from J4 connector.



∗ AKM assumes no responsibility for the trouble when using the above circuit examples.

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4631-VN according to previous term.

2. Connect IBM-AT compatible PC with AKD4631VN by 10-line type flat cable (packed with AKD4631-VN). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer “Installation Manual of Control Software Driver by AKM device control software”. In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled “AK4631VN Evaluation Kit” into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of “akd4631.exe” to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click “Write default” button.
3. Then set up the dialog and input data.

■ Explanation of each buttons

1. [Port Setup] : Set up the printer port.
2. [Write default] : Initialize the register of AK4631-VN.
3. [All Write] : Write all registers that is currently displayed.
4. [Function1] : Dialog to write data by keyboard operation.
5. [Function2] : Dialog to write data by keyboard operation.
6. [F3] : Dialog of sequential writing.
7. [SAVE] : Save the current register setting.
8. [OPEN] : Write the saved values to all register.
9. [Write] : Dialog to write data by mouse operation.

■ Explanation of each dialog

1. [Function1 Dialog] : Dialog to write data by keyboard operation

   Address Box: Input registers address in 2 figures of hexadecimal.
   Data Box: Input registers data in 2 figures of hexadecimal.

   If you want to write the input data to AK4631VN, click “OK” button. If not, click “Cancel” button.

2. [Function2 Dialog] : Dialog to evaluate IVOL

   Address Box: Input registers address in 2 figures of hexadecimal.
   Start Data Box: Input starts data in 2 figures of hexadecimal.
   End Data Box: Input end data in 2 figures of hexadecimal.
   Interval Box: Data is written to AK4631VN by this interval.
   Step Box: Data changes by this step.
   Mode Select Box:

   If you check this check box, data reaches end data, and returns to start data.
   [Example] Start Data = 00, End Data = 09
   Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

   If you do not check this check box, data reaches end data, but does not return to start data.
   [Example] Start Data = 00, End Data = 09
   Data flow: 00 01 02 03 04 05 06 07 08 09

   If you want to write the input data to AK4631VN, click “OK” button. If not, click “Cancel” button.

3. [Write Dialog] : Dialog to write data by mouse operation

   There are dialogs corresponding to each register.

   Click the “Write” button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

   If you want to write the input data to AK4631VN, click “OK” button. If not, click “Cancel” button.

■ Indication of data

Input data is indicated on the register map. Red letter indicates “H” or “1” and blue one indicates “L” or “0”. Blank is the part that is not defined in the datasheet.

■ Attention on the operation

If you set up Function1 or Function2 dialog, input data to all boxes. Attention dialog is indicated if you input data or address that is not specified in the datasheet or you click “OK” button before you input data. In that case set up the dialog and input data once more again. These operations does not need if you click “Cancel” button or check the check box.

MEASUREMENT RESULTS EXAMPLE

1.AK4631 Mode: EXT mode (Slave)

[Measurement condition]

- Measurement unit: ROHDE & SCHWARZ, UPD05
- MCKI: 256fs, 512fs
- BICK: 64fs
- Bit: 16bit
- Sampling Frequency: 8kHz & 16kHz
- Measurement Frequency: 20 ~ 3.4kHz (fs=8kHz), 20 ~ 8kHz (fs=16kHz)
- Power Supply: AVDD=DVDD=3.3V,SVDD=3.3V/5.0V
- Temperature: Room
- Input Frequency: 1kHz

[Measurement Results]

1.ADC characteristics (MIC Gain = +20dB, IPGA=0dB, ALC1 = OFF, MIC → IPGA → ADC)

	Result			
MCKI clock	512fs		256fs	
Sampling Frequency	8kHz	16kHz	8kHz	16kHz
S/(N+D) (-1dBFS)	84.6dB	84.1dB	85.2dB	84.1dB
D-Range (-60dBFS)	86.1dB	85.0dB	88.6dB	84.9dB
S/N	86.1dB	85.0dB	88.6dB	85.0dB

2. DAC characteristics (AOUT) (DAC → AOUT, DVOL = 0dB)

	Result			
MCKI clock	512fs		256fs	
Sampling Frequency	8kHz	16kHz	8kHz	16kHz
S/(N+D) (0dBFS)	89.7dB	89.0dB	86.0dB	91.9dB
D-Range (-60dBFS)	93.5dB	91.1dB	93.7dB	95.3dB
S/N	94.1dB	92.2dB	94.5dB	95.3dB

3. Speaker-Amp characteristics (DAC → MOUT → MIN → SPP/SPN, ALC2=OFF)

			Result
S/(N+D)	SVDD=3.3V RL=8Ω	SPKG1-0 = "00" (-0.5dBFS)	65.8dB
		SPKG1-0 = "01" (-0.5dBFS)	67.8dB
	SVDD=5.0V RL=50Ω	SPKG1-0 = "10" (-0.5dBFS)	74.5dB
		SPKG1-0 = "11" (-0.5dBFS)	78.1dB
S/N	SVDD=3.3V RL=8Ω	SPKG1-0 = "00"	90.2dB
		SPKG1-0 = "01"	90.4dB
	SVDD=5.0V RL=50Ω	SPKG1-0 = "10"	90.3dB
		SPKG1-0 = "11"	90.4dB

4. Loop-back (MIC → ADC → DAC → AOUT)

	Result			
MCKI clock	512fs		256fs	
Sampling Frequency	8kHz	16kHz	8kHz	16kHz
S/(N+D) (-1dBFS)	84.4dB	84.0dB	84.7dB	84.0dB
D-Range (-60dBFS)	85.9dB	84.8dB	87.8dB	84.5dB
S/N	86.0dB	84.8dB	87.9dB	84.6dB

2.AK4631 Mode: PLL SLAVE mode

[Measurement condition]

- Measurement unit: ROHDE & SCHWARZ, UPD05
- Bit: 16bit
- Sampling Frequency: 8kHz & 16kHz
- Measurement Frequency: 20 ~ 3.4kHz (fs=8kHz), 20 ~ 8kHz (fs=16kHz)
- Power Supply: AVDD=DVDD=SVDD=3.3V
- Temperature: Room
- Input Frequency: 1kHz

[Measurement Results]

2-1. PLL Reference clock : BICK or FCK pin

Loop-back (MIC → ADC → DAC → AOUT)

	Result			
PLL Reference clock	1fs (FCK pin)		16fs (BICK pin)	
Sampling Frequency	8kHz	16kHz	8kHz	16kHz
S/(N+D) (-1dBFS)	65.1dB	72.2dB	85.0dB	83.6dB
D-Range (-60dBFS)	86.3dB	85.0dB	87.8dB	85.0dB
S/N	86.4dB	85.0dB	87.9dB	85.0dB

2-2. PLL Reference clock : MCKI pin

Loop-back (MIC → ADC → DAC → AOUT)

	Result	
PLL Reference clock	12.288MHz	
Sampling Frequency	8kHz	16kHz
S/(N+D) (-1dBFS)	84.5dB	83.4dB
D-Range (-60dBFS)	86.3dB	85.1dB
S/N	86.6dB	85.2dB

3.AK4631 Mode: PLL MASTER mode

[Measurement condition]

- Measurement unit: ROHDE & SCHWARZ, UPD05
- MCKI: 12.288 MHz
- BICK: 16fs
- Bit: 16bit
- Sampling Frequency: 8kHz & 16kHz
- Measurement Frequency: 20 ~ 3.4kHz (fs=8kHz), 20 ~ 8kHz (fs=16kHz)
- Power Supply: AVDD=DVDD=SVDD=3.3V
- Temperature: Room
- Input Frequency:1kHz

[Measurement Results]

Loop-back (MIC → ADC → DAC → AOUT)

	Result	
	8kHz	16kHz
S/(N+D) (-1dBFS)	84.4dB	83.9dB
D-Range (-60dBFS)	86.1dB	85.3dB
S/N	86.4dB	85.3dB

4.PLOT DATA (EXT Slave mode)

4-1.ADC (MIC → ADC) PLOT DATA

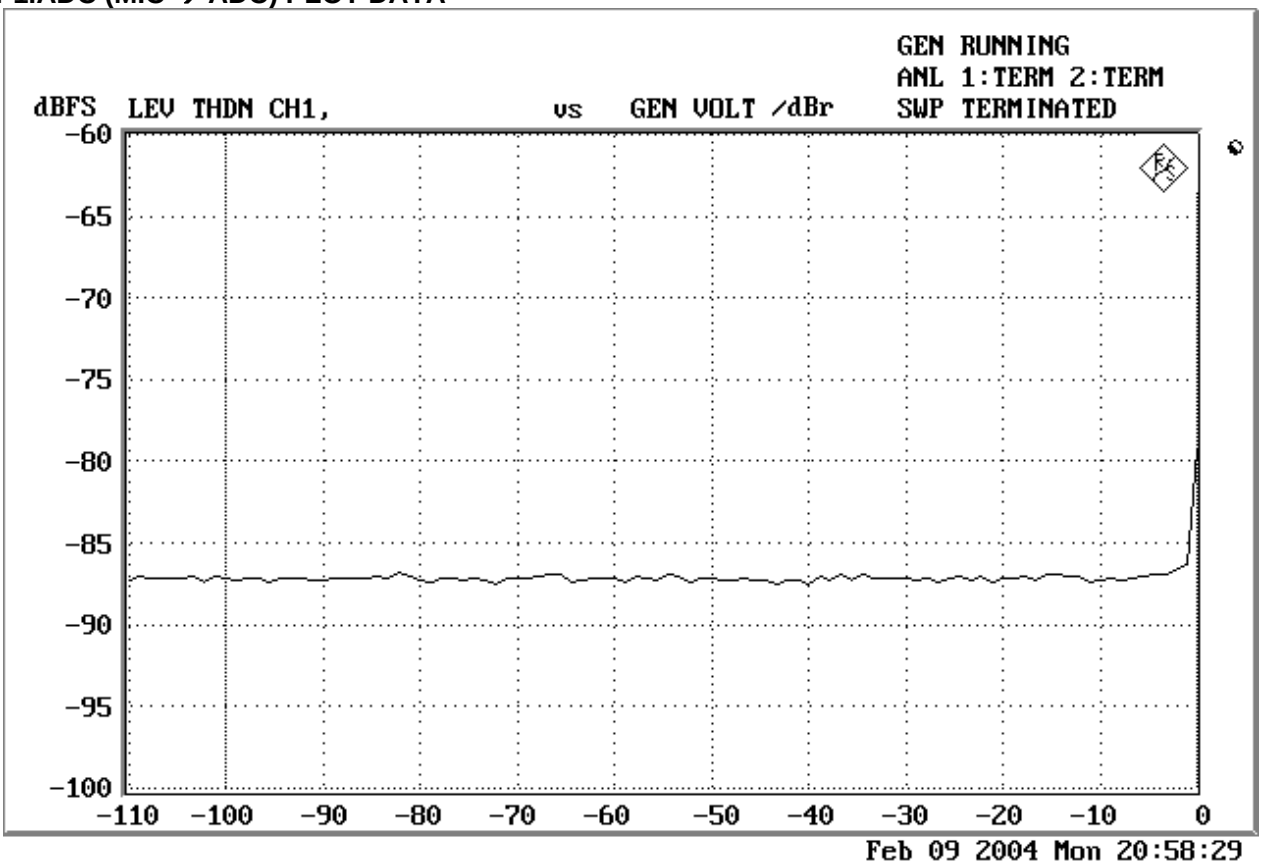


Figure 8. THD+N vs. Input Level

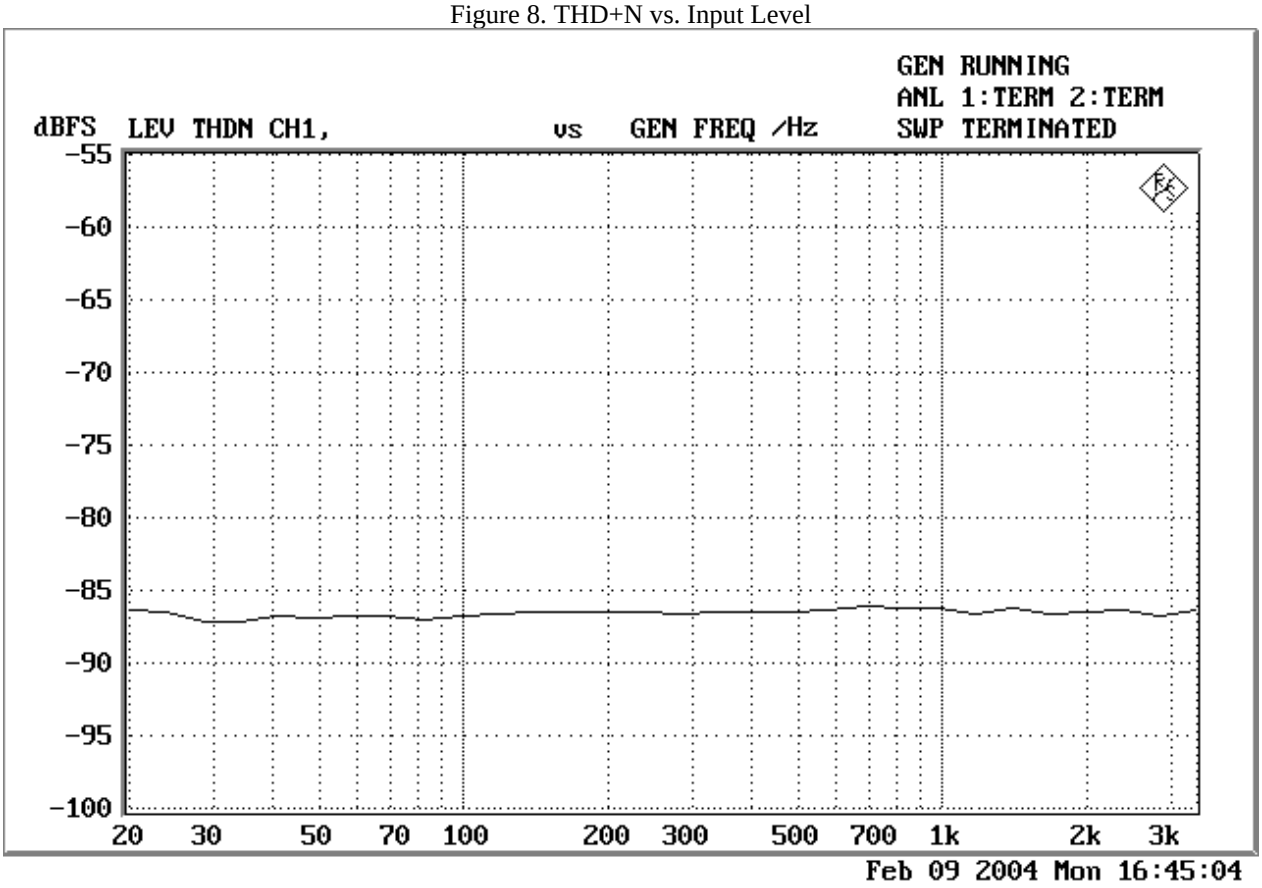


Figure 9. THD+N vs. Input Frequency (Input Level = -1dBFS)

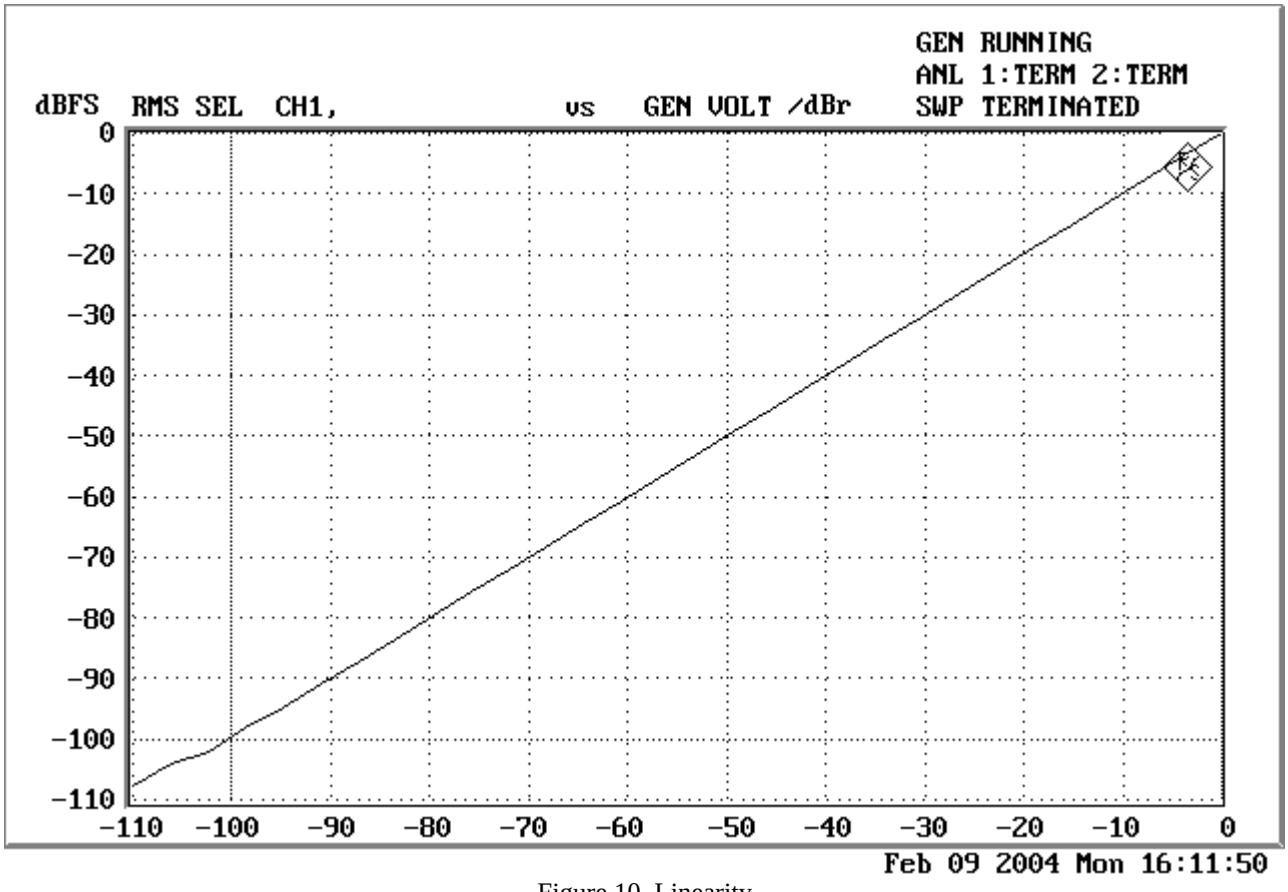


Figure 10. Linearity

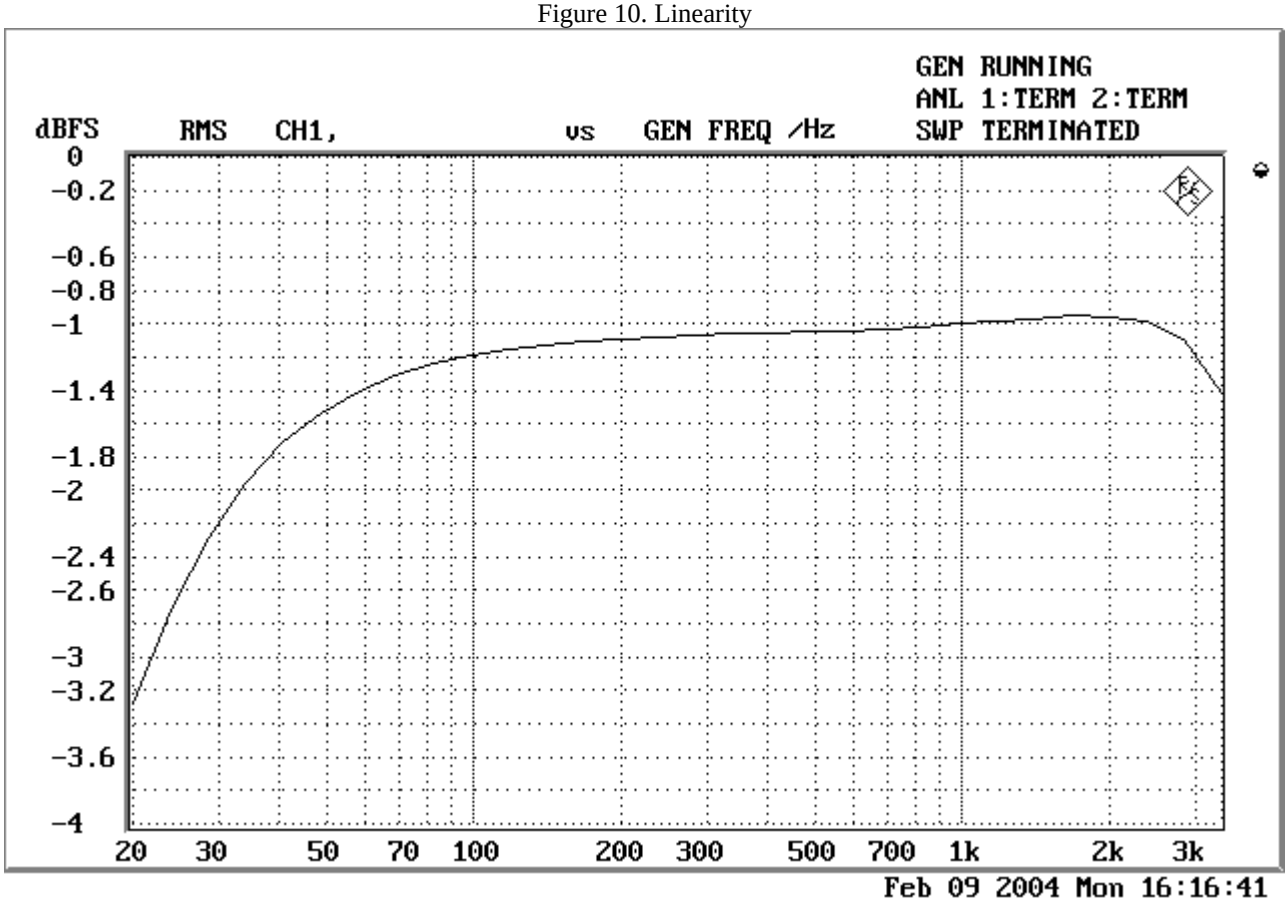


Figure 11. Frequency Response

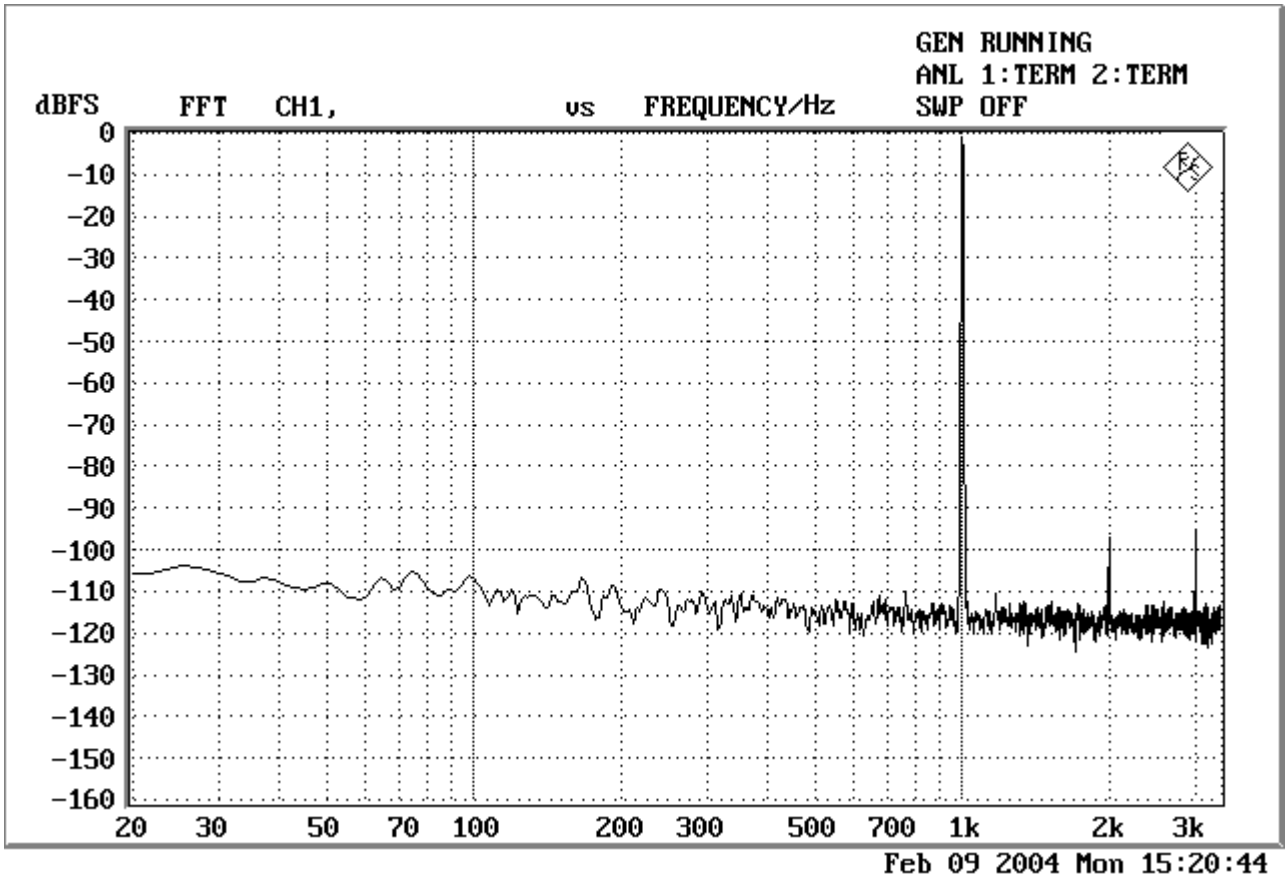


Figure 12. FFT Plot (Input level=-1.0dBFS)

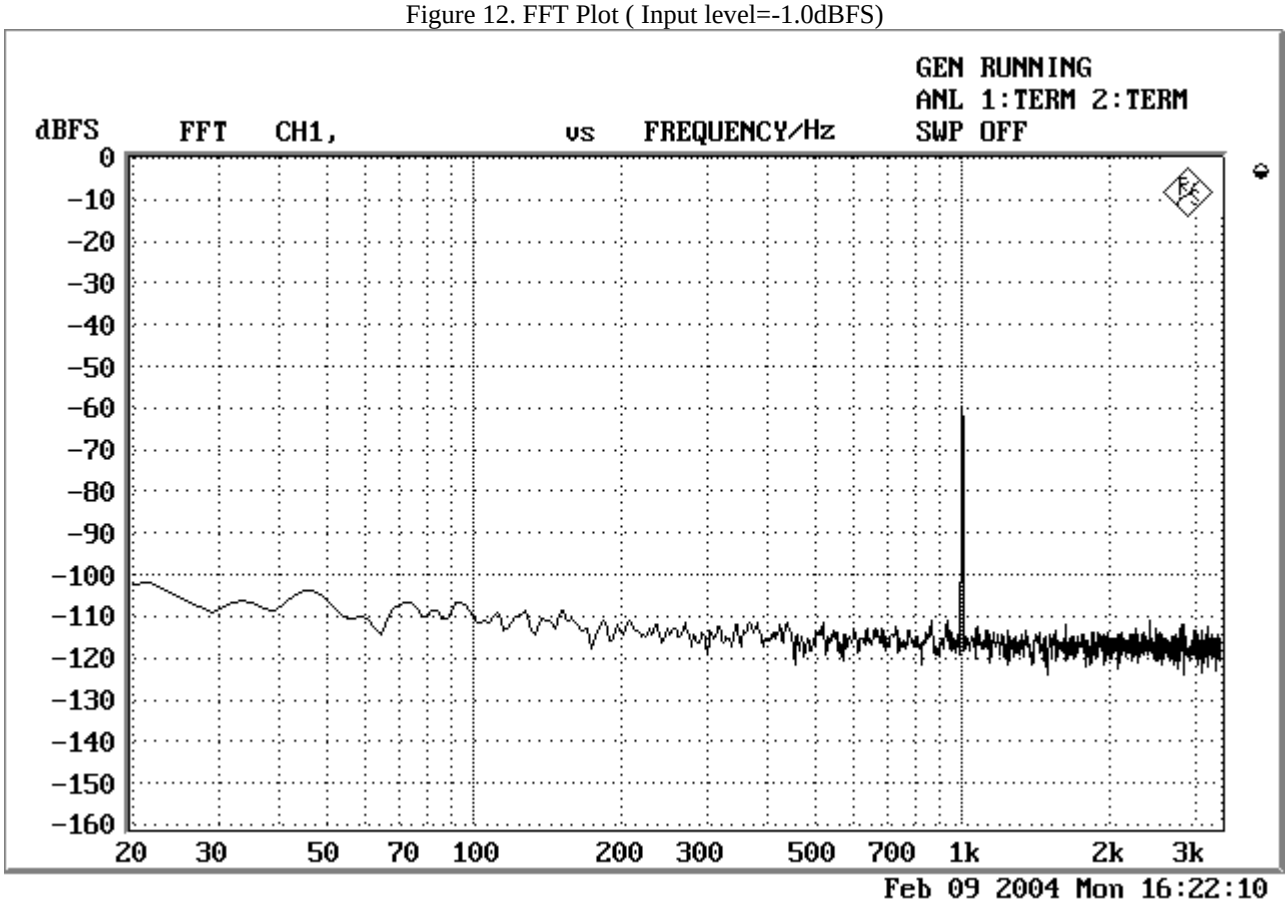


Figure 13. FFT Plot (Input level=-60.0dBFS)

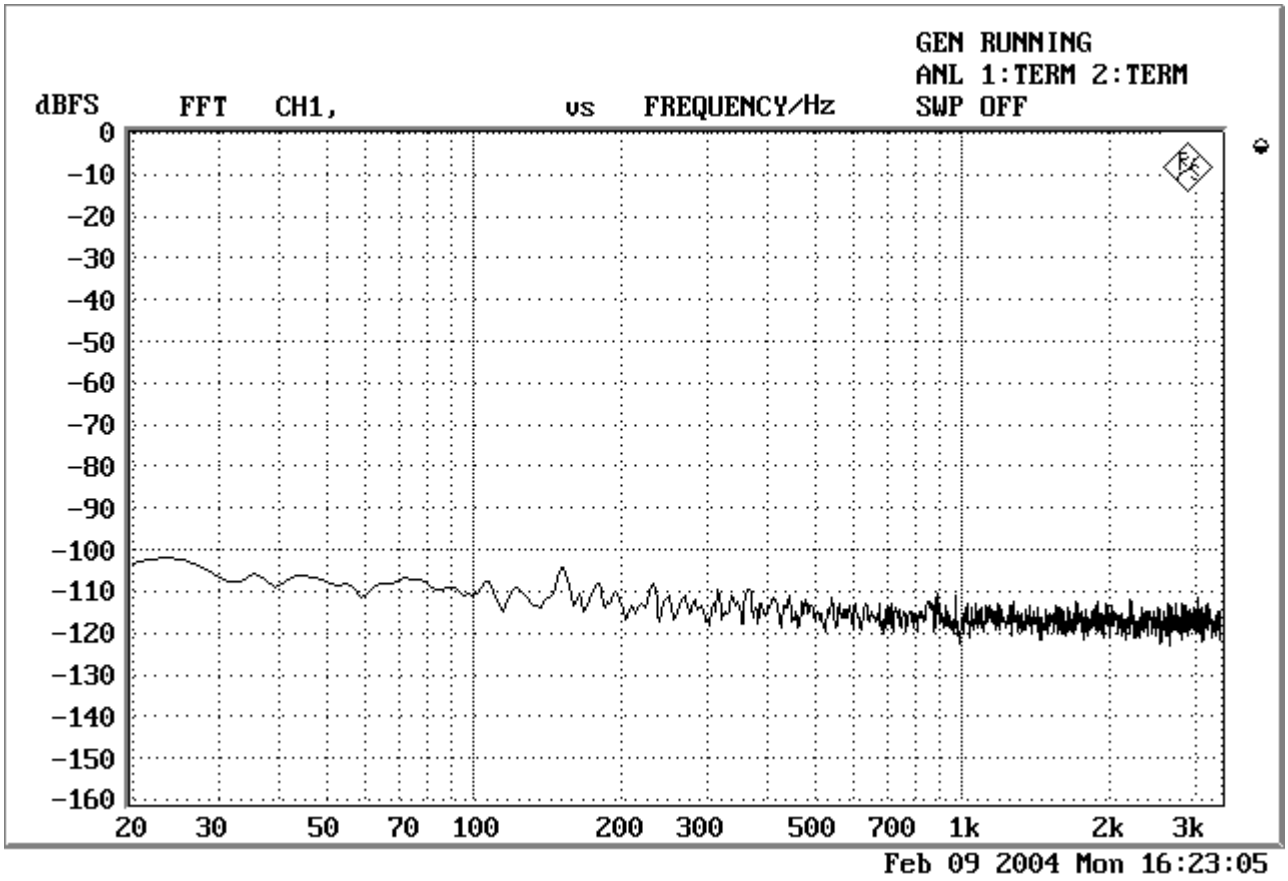


Figure 14. FFT Plot (“0” data input)

4-2. DAC (DAC → AOUT) PLOT DATA

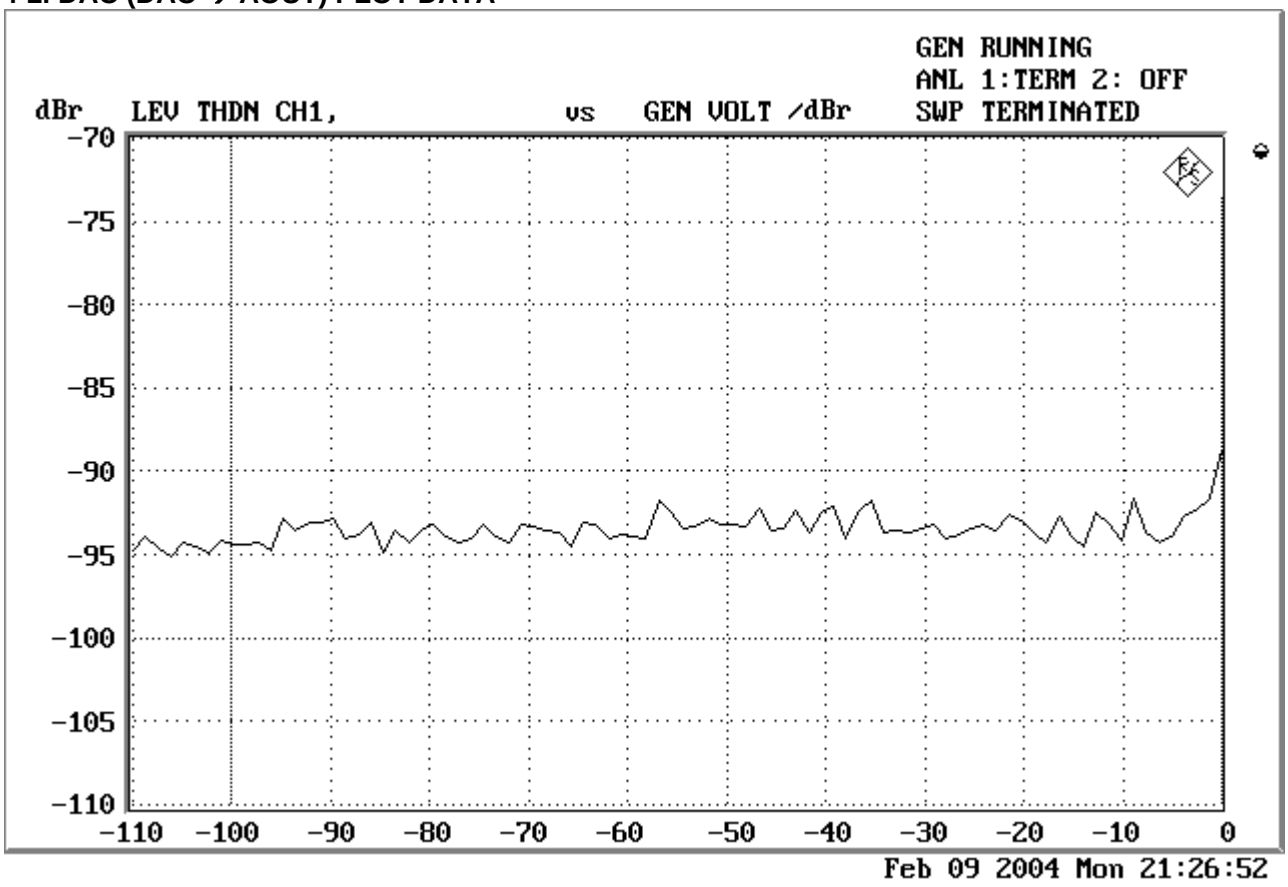


Figure 15. THD+N vs. Input Level

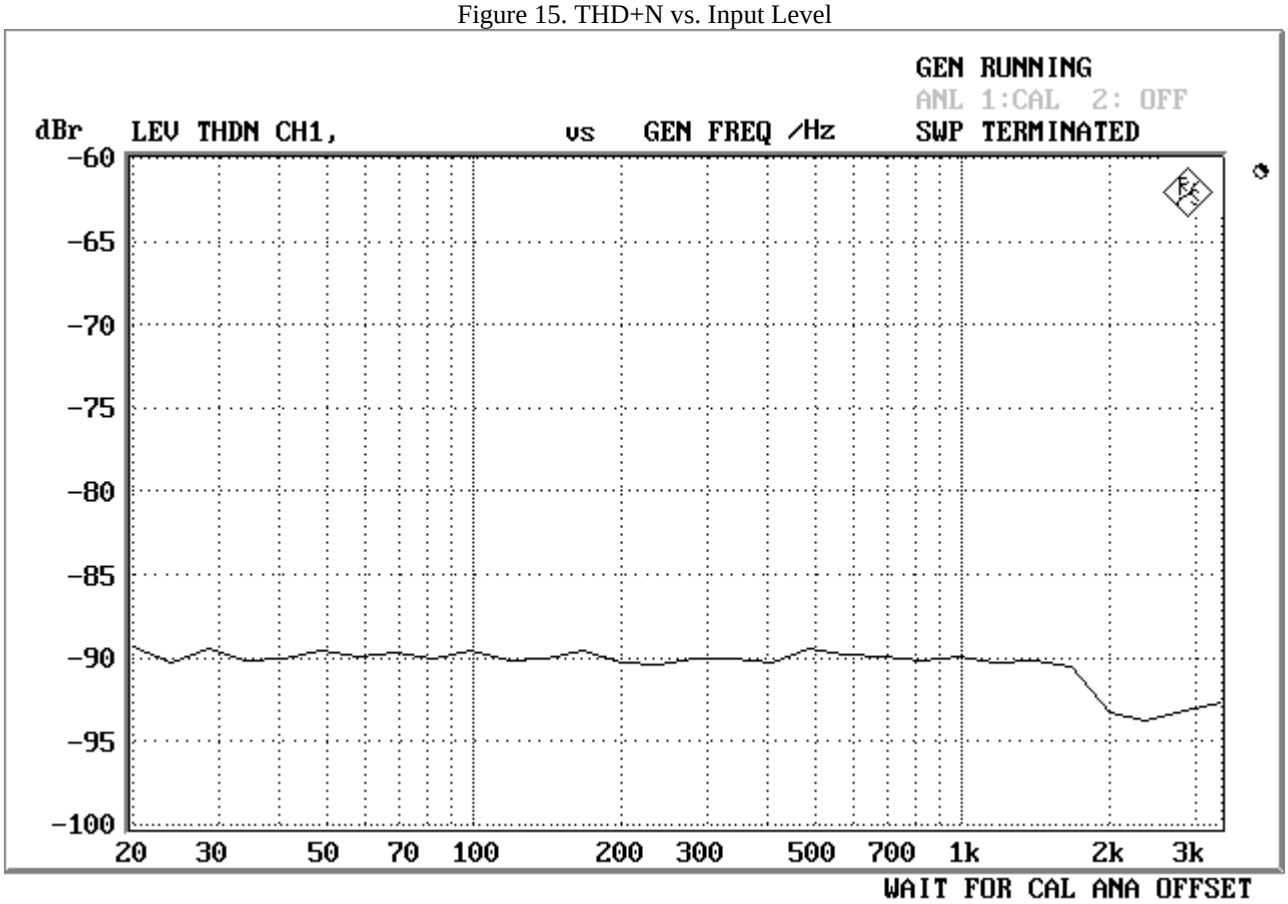


Figure 16. THD+N vs. Input Frequency (Input Level = 0dBFS)

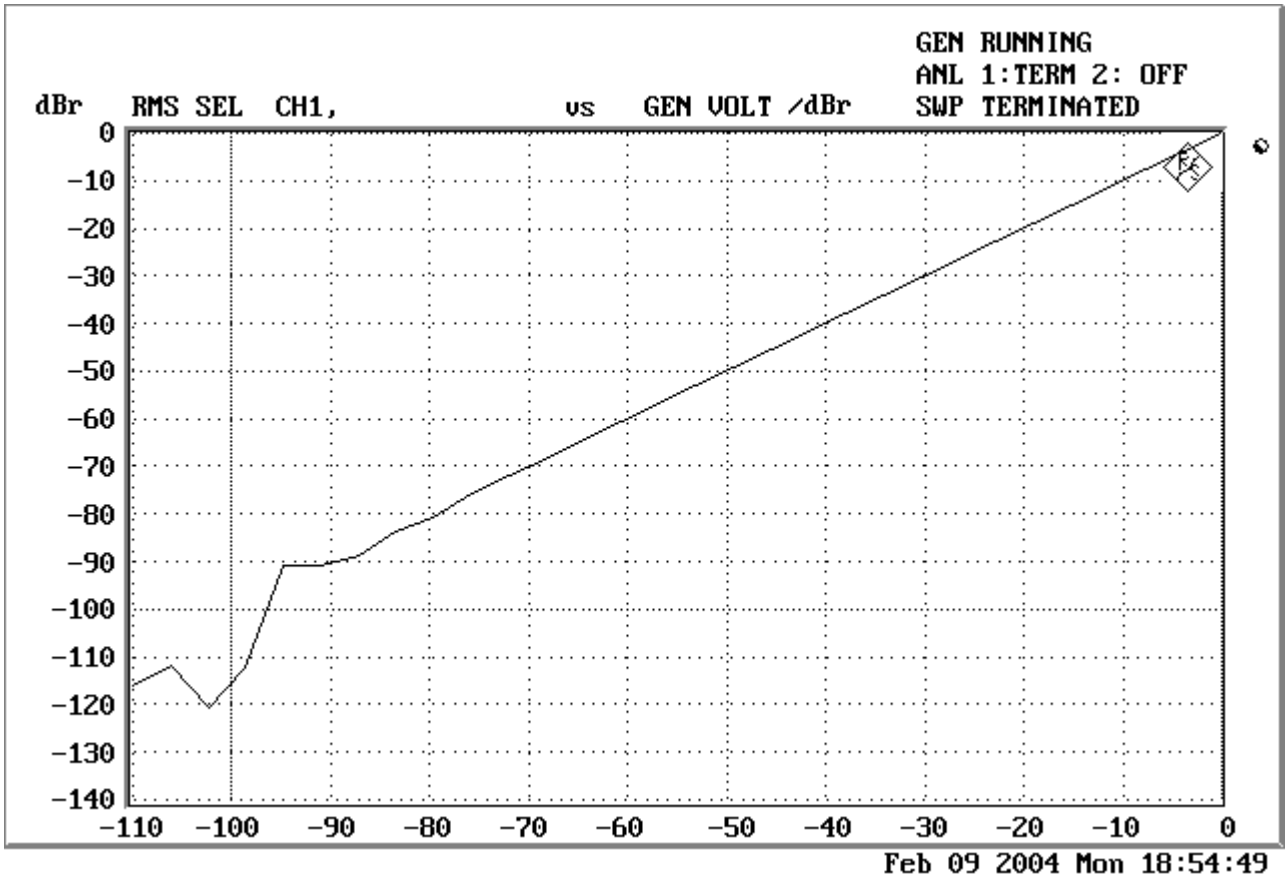


Figure 17. Linearity

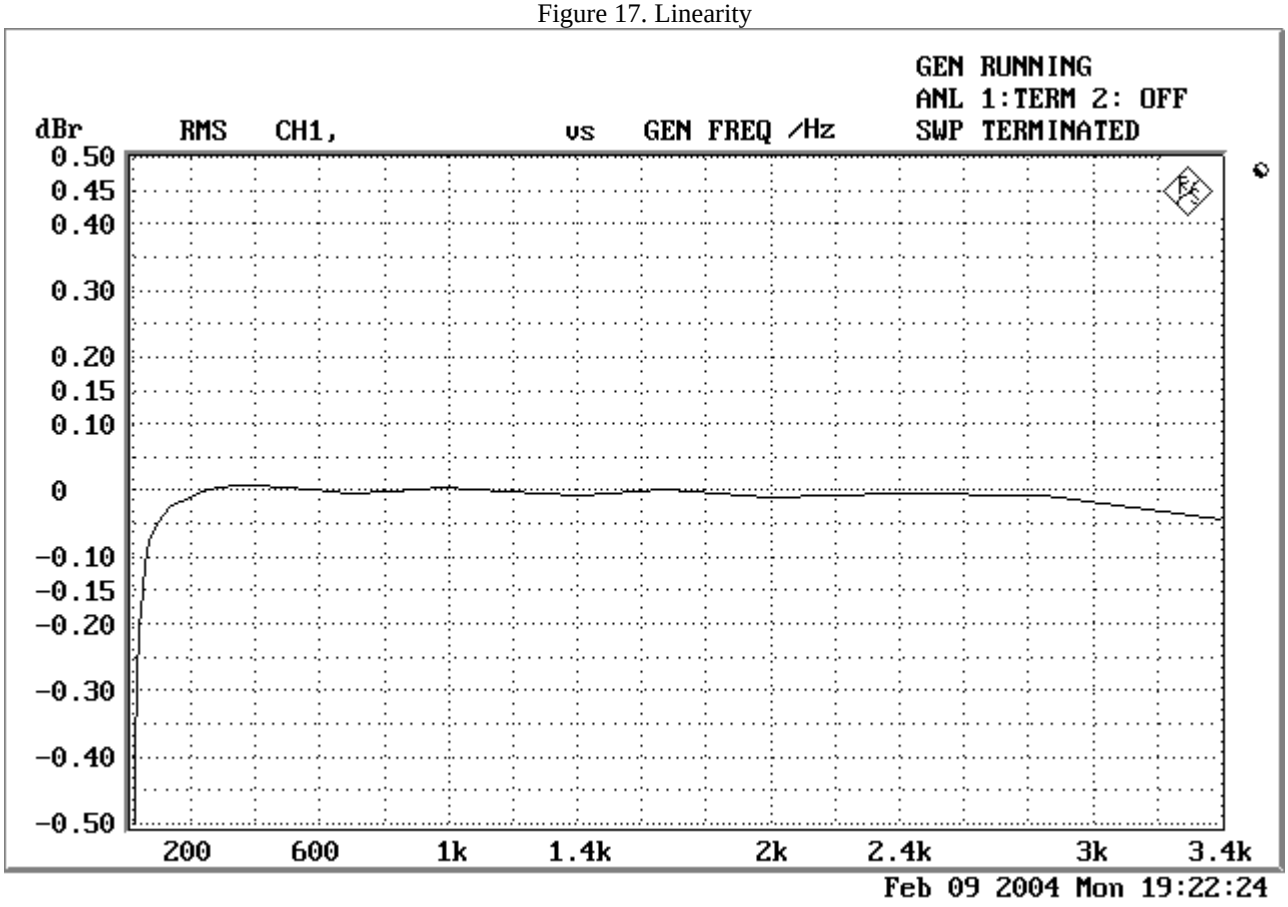


Figure 18. Frequency Response

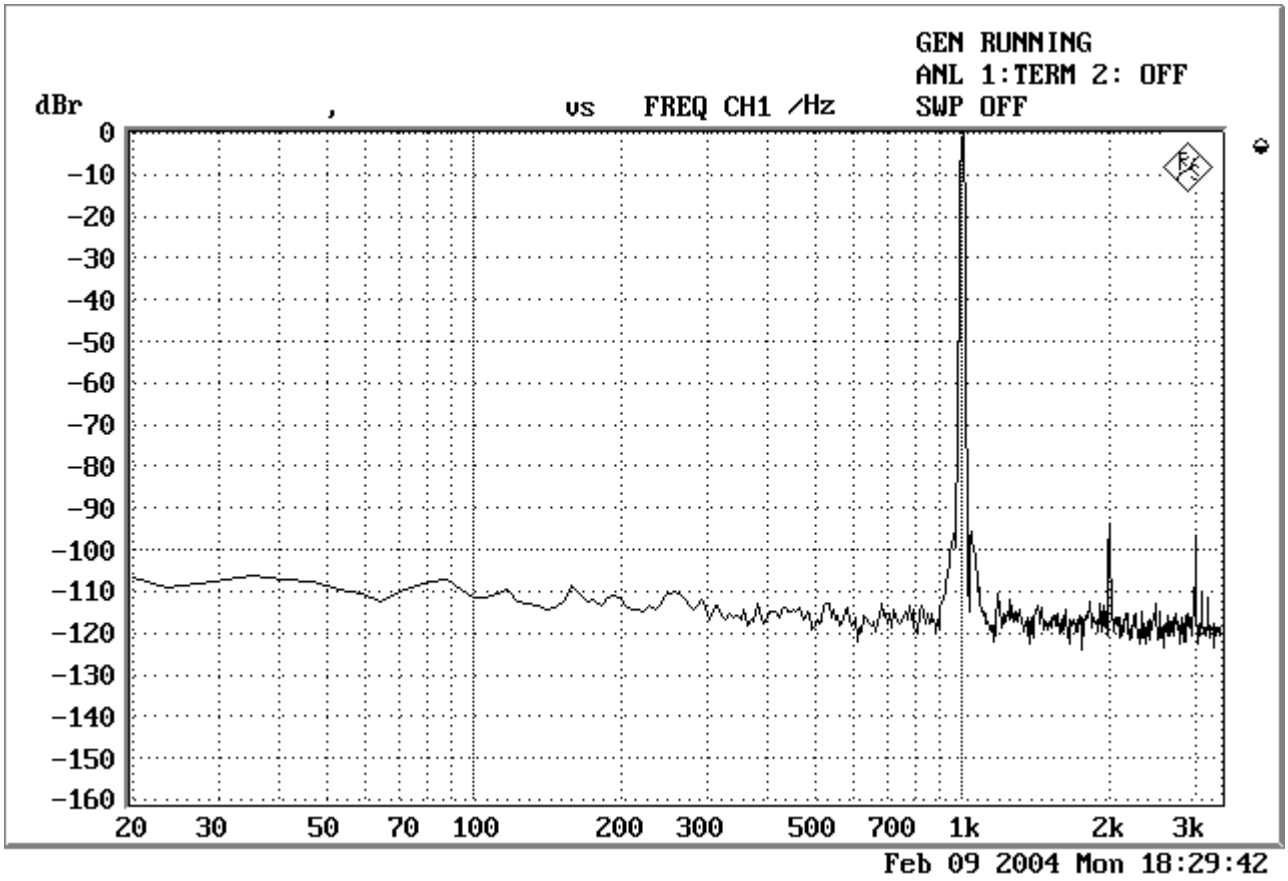


Figure 19. FFT Plot (Input level=0dBFS)

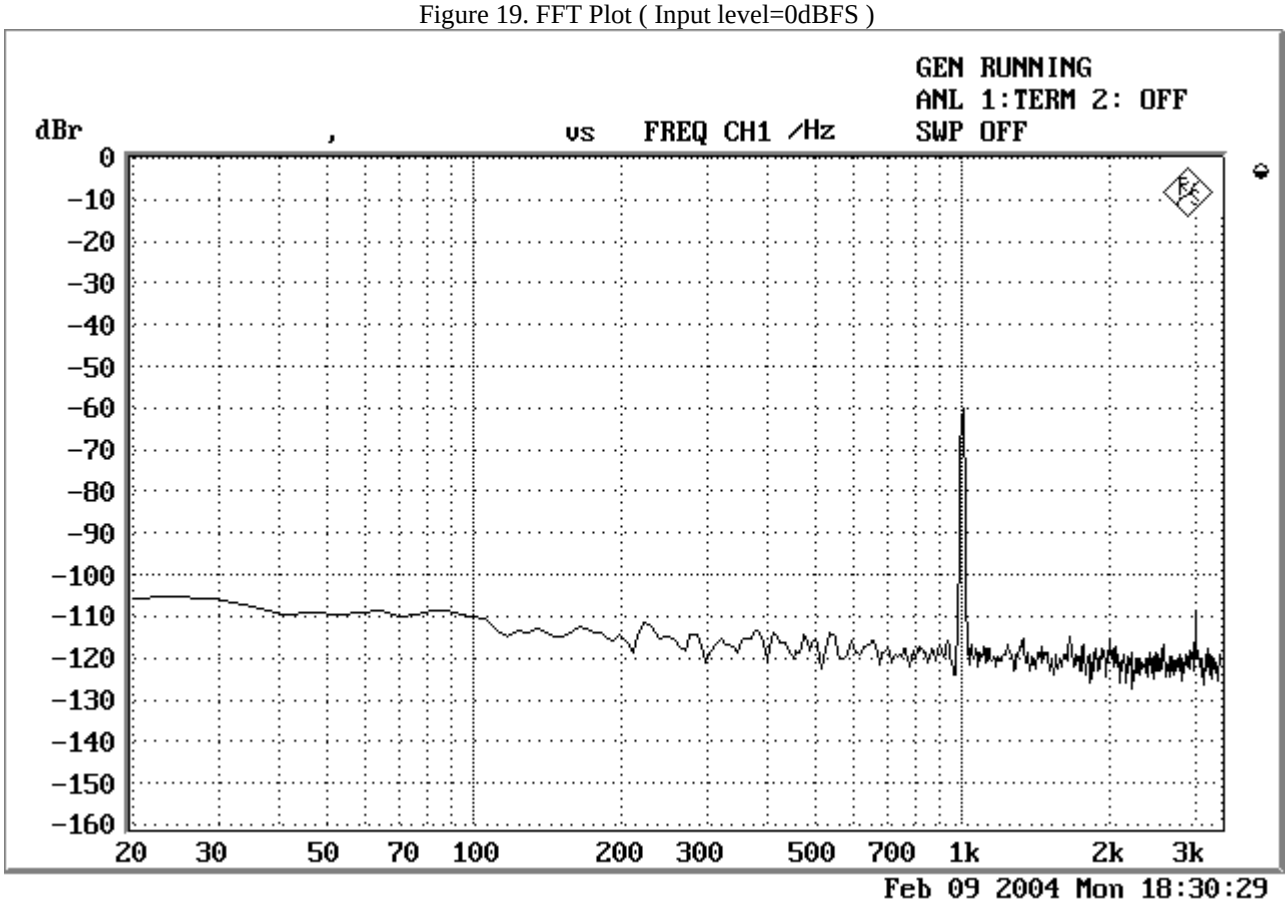


Figure 20. FFT Plot (Input level=-60.0dBFS)

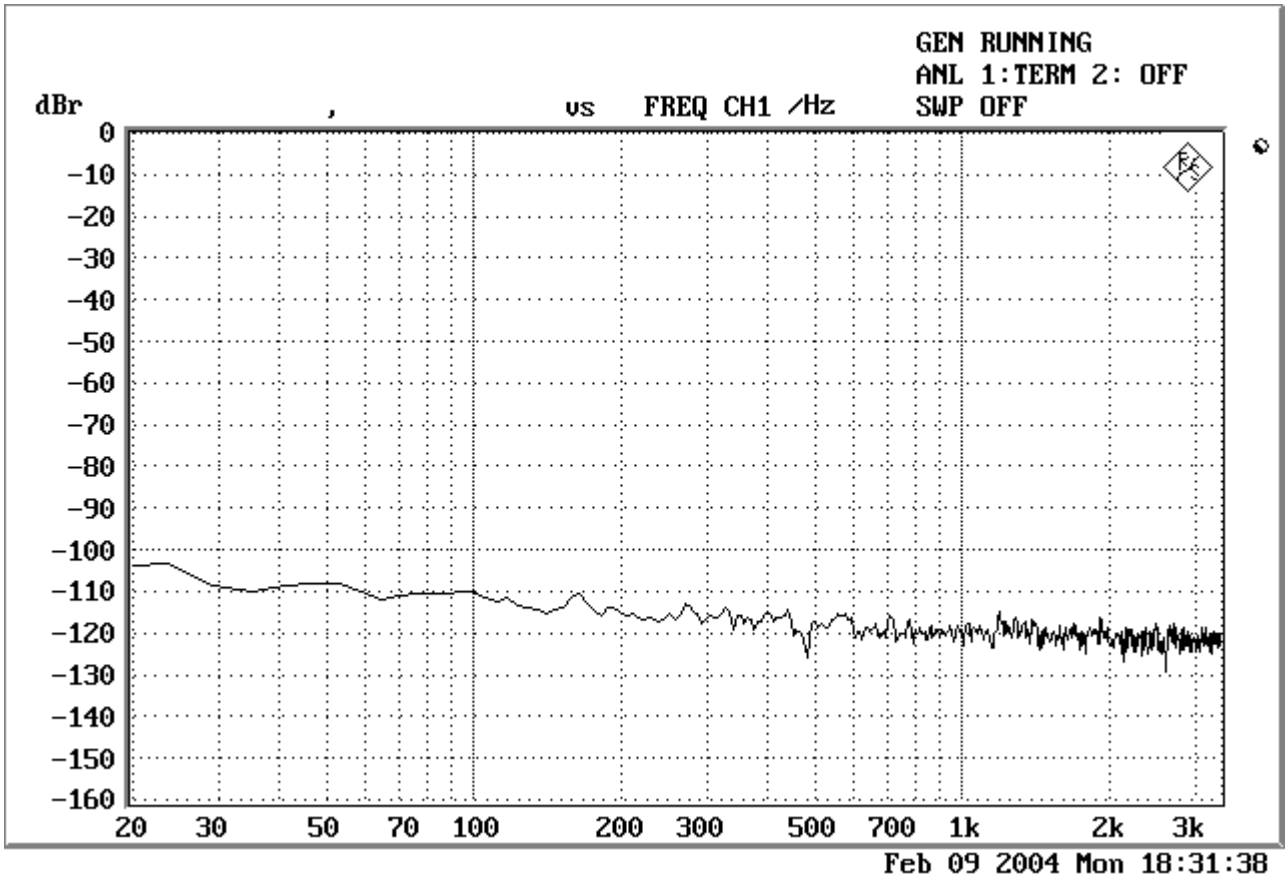
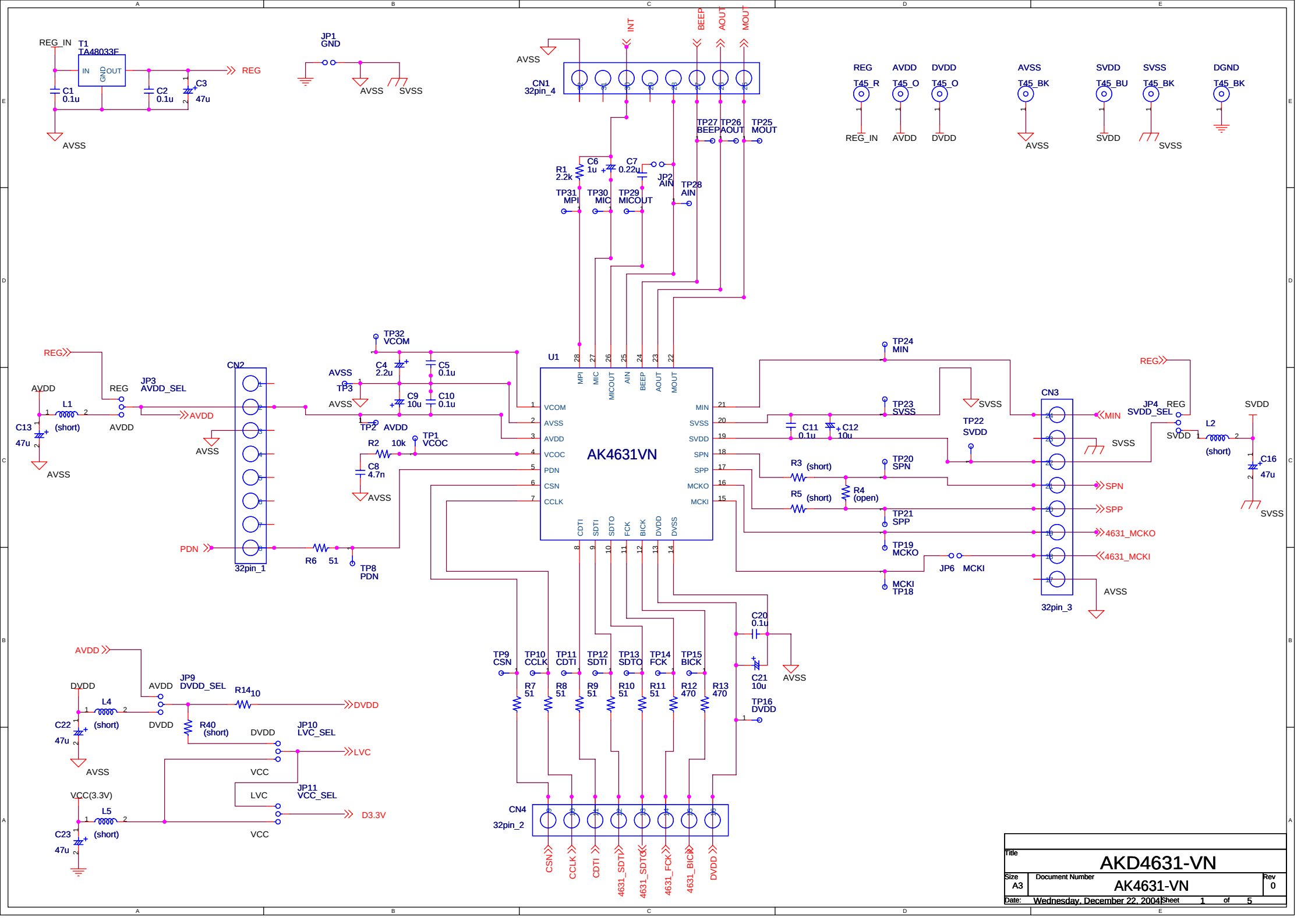


Figure 21. FFT Plot (“0” data input)

Revision History

Date	Manual Revision	Board Revision	Reason	Contents
04/01/25	KM077300	0	First Edition	


REG_IN
T1
TA48033F
IN
GND
OUT
REG
C1
0.1u
C2
0.1u
C3
47u
AVSS
JP1
GND
AVSS
SVSS
INT
BEEP
AOUT
MOUT
CN1
32pin_4
REG
T45_R
REG_IN
AVDD
T45_O
AVDD
DVDD
T45_O
DVDD
AVSS
T45_BK
AVSS
SVDD
T45_BU
SVDD
SVSS
T45_BK
SVSS
DGND
T45_BK
TP27
BEEP
TP26
AOUT
TP25
MOUT
R1
2.2k
C6
1u
C7
0.22u
JP2
AIN
TP28
AIN
TP31
MPI
TP30
MIC
TP29
MICOUT
U1
AK4631VN
MPI
MIC
MICOUT
AIN
BEEP
AOUT
MOUT
VCOM
AVSS
AVDD
VCOC
PDN
CSN
CCLK
MIN
SVSS
SVDD
SPN
SPP
MCKO
MCKI
CDTI
SDTI
SDTO
FCK
BICK
DVDD
DVSS
REG
AVDD
L1
(short)
C13
47u
JP3
AVDD_SEL
AVDD
AVSS
CN2
32pin_1
TP32
VCOM
C4
2.2u
C5
0.1u
AVSS
TP3
C9
10u
C10
0.1u
TP2
AVDD
R2
10k
TP1
VCOC
C8
4.7n
AVSS
PDN
R6
51
TP8
PDN
TP24
MIN
TP23
SVSS
TP22
SVDD
C11
0.1u
C12
10u
R3
(short)
TP20
SPN
R4
(open)
R5
(short)
TP21
SPP
TP19
MCKO
JP6
MCKI
MCKI
TP18
CN3
32pin_3
MIN
SVSS
SPN
SPP
4631_MCKO
4631_MCKI
AVSS
REG
JP4
SVDD_SEL
SVDD
L2
(short)
C16
47u
SVSS
AVDD
DVDD
JP9
DVDD_SEL
AVDD
R14
10
DVDD
L4
(short)
C22
47u
AVSS
DVDD
R40
(short)
DVDD
JP10
LVC_SEL
LVC
VCC
VCC(3.3V)
L5
(short)
C23
47u
AVSS
LVC
JP11
VCC_SEL
D3.3V
VCC
TP9
CSN
TP10
CCLK
TP11
CDTI
TP12
SDTI
TP13
SDTO
TP14
FCK
TP15
BICK
R7
51
R8
51
R9
51
R10
51
R11
51
R12
470
R13
470
C20
0.1u
C21
10u
AVSS
TP16
DVDD
CN4
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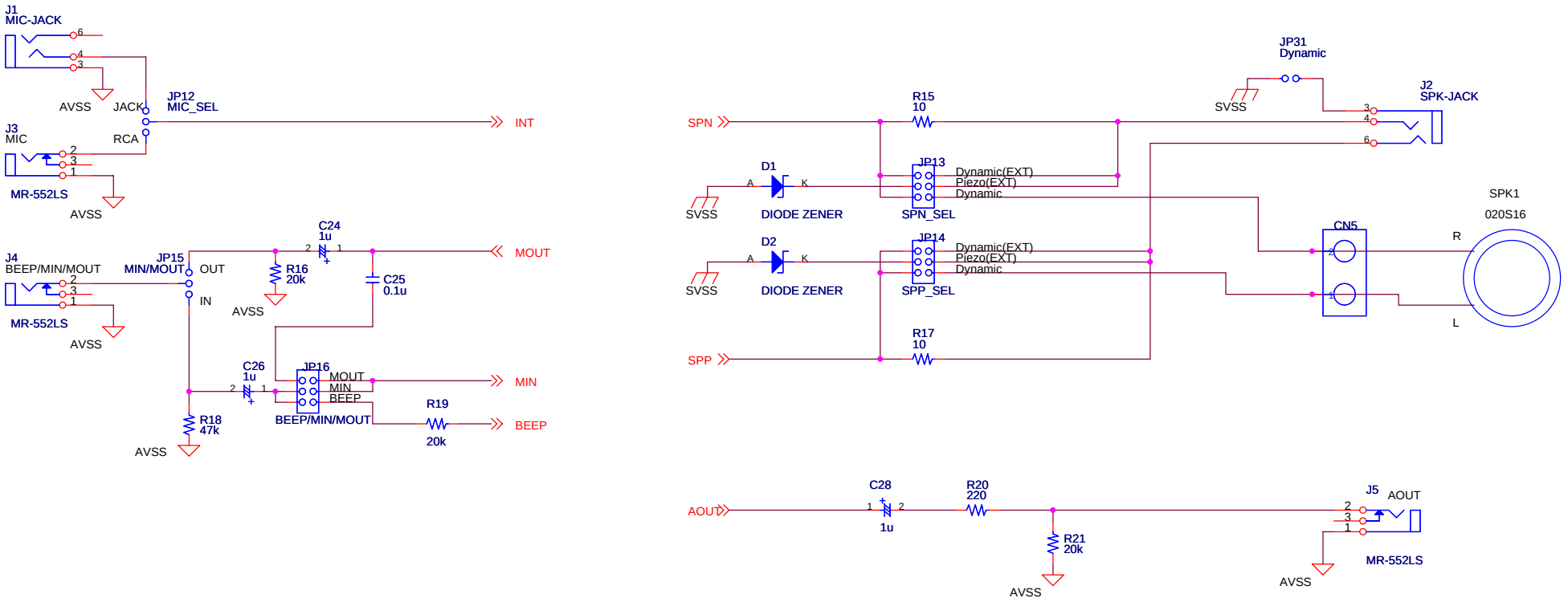
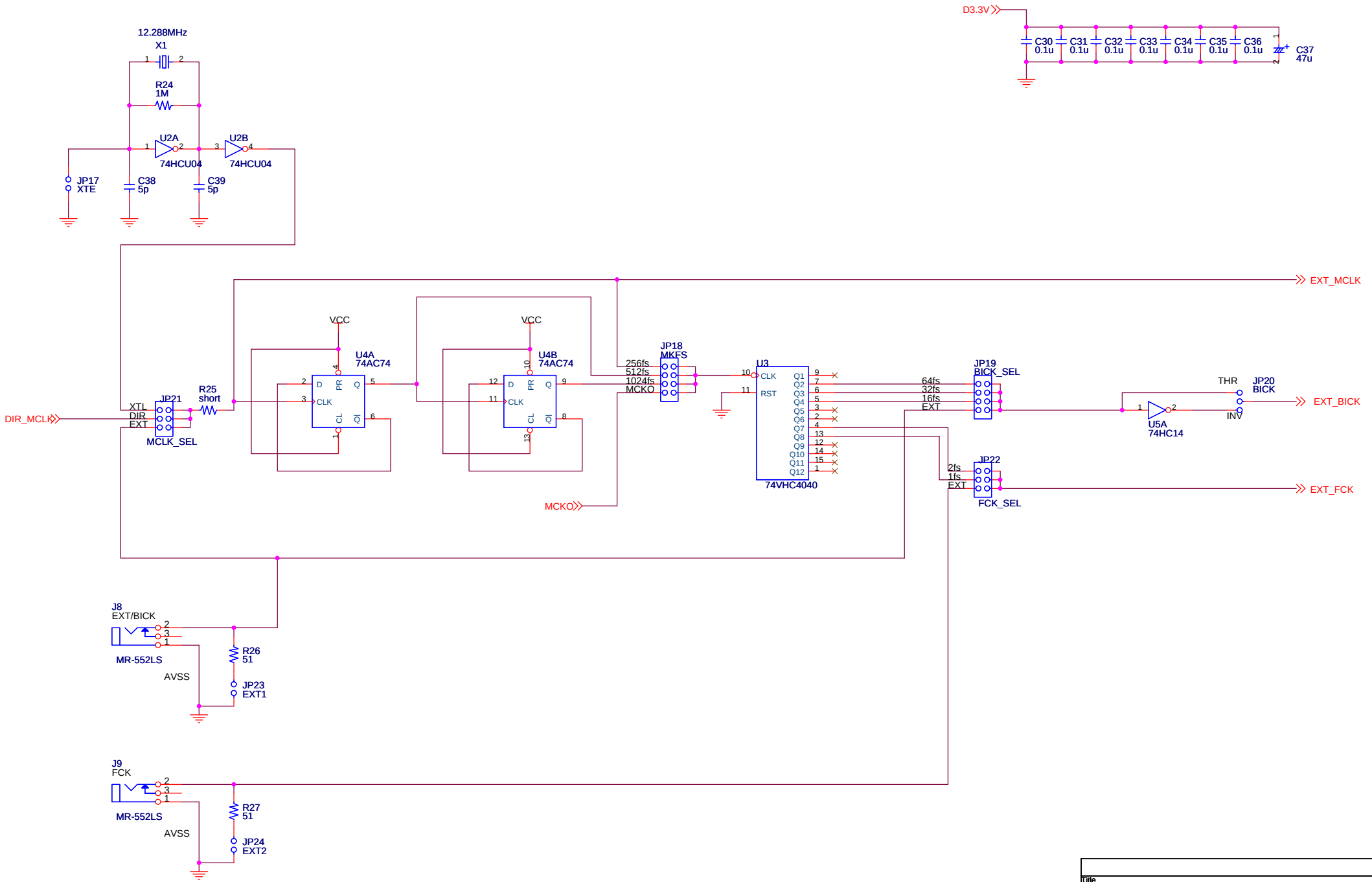
CSN
CCLK
CDTI
4631_SDTI
4631_SDTO
4631_FCK
4631_BICK
DVDD
Title
AKD4631-VN
Size
A3
Document Number
AK4631-VN
Rev
0
Date:
Wednesday, December 22, 2004
Sheet
1
of
5



Title	AKD4631-VN	
Size: A3	Document Number: Input/Output	Rev: 0
Date: Wednesday, December 22, 2004	Sheet 2 of 5	

for
74HCU04,74AC74,74VHC4040,74HC14,74HC14,74HC541,74HCT04



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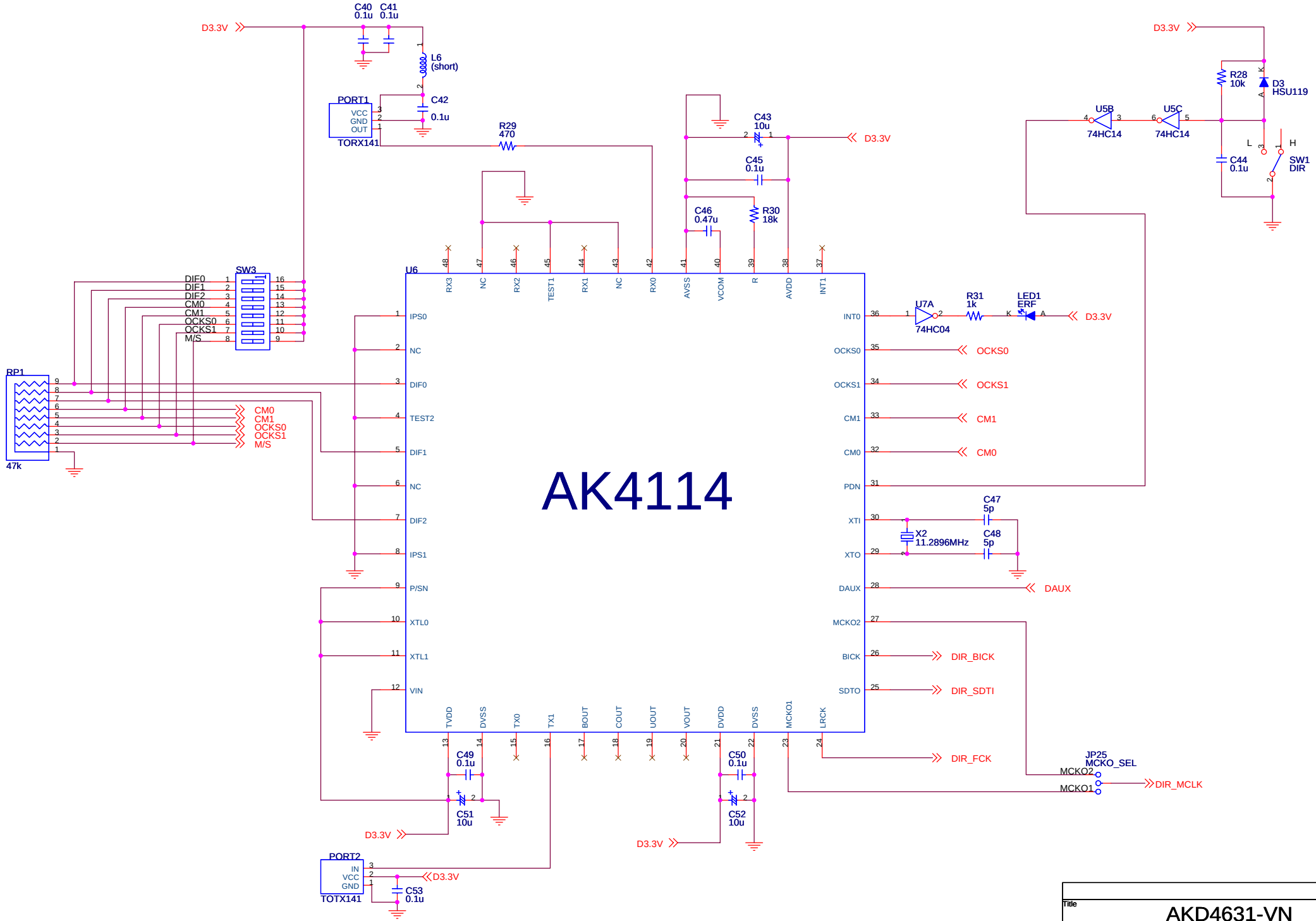
Size A3	Document Number CLOCK	Rev 0
Date: Wednesday, December 22, 2004	Sheet 3 of 5	



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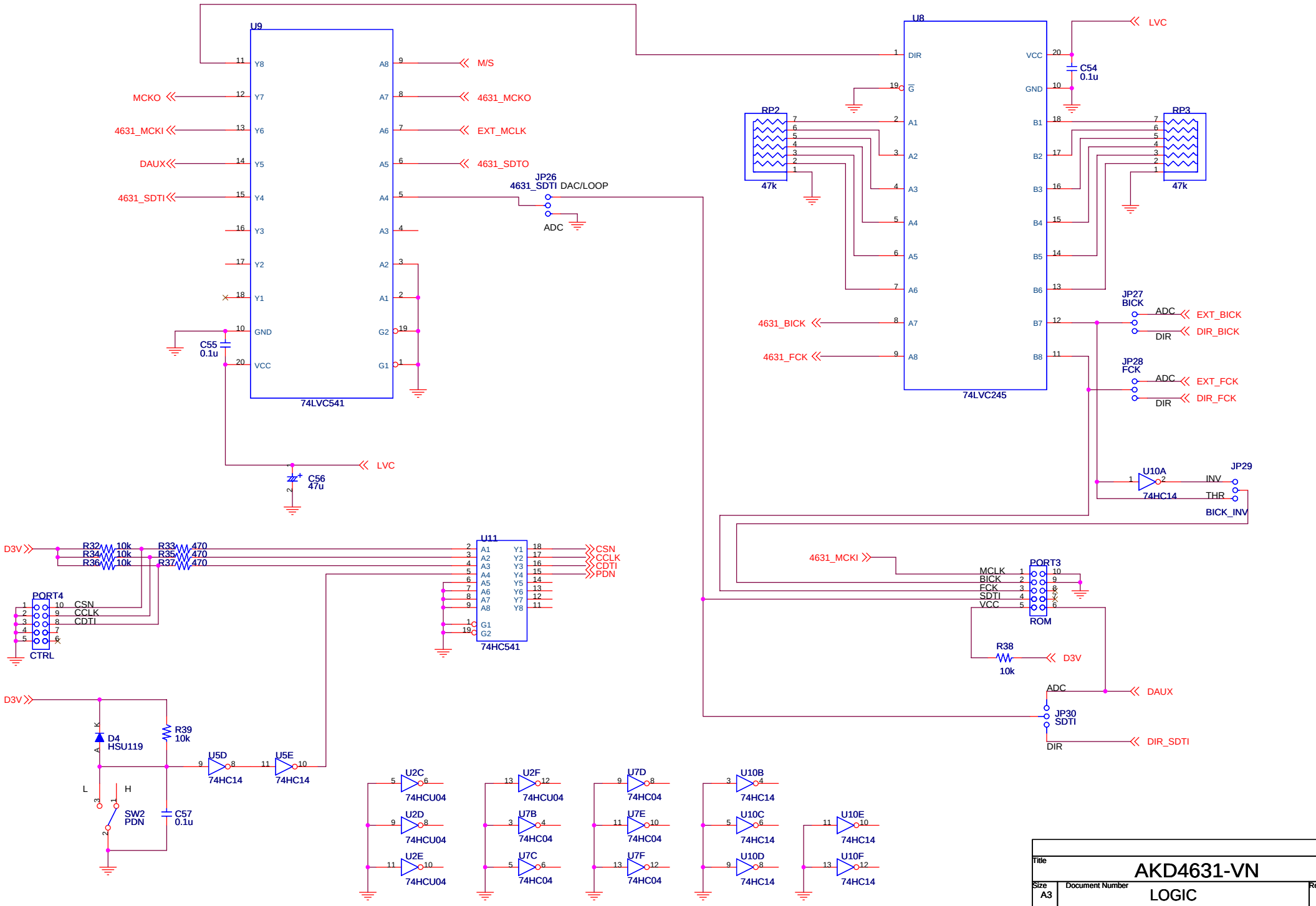
Date: Wednesday, December 22, 2004	Sheet 4 of 5	



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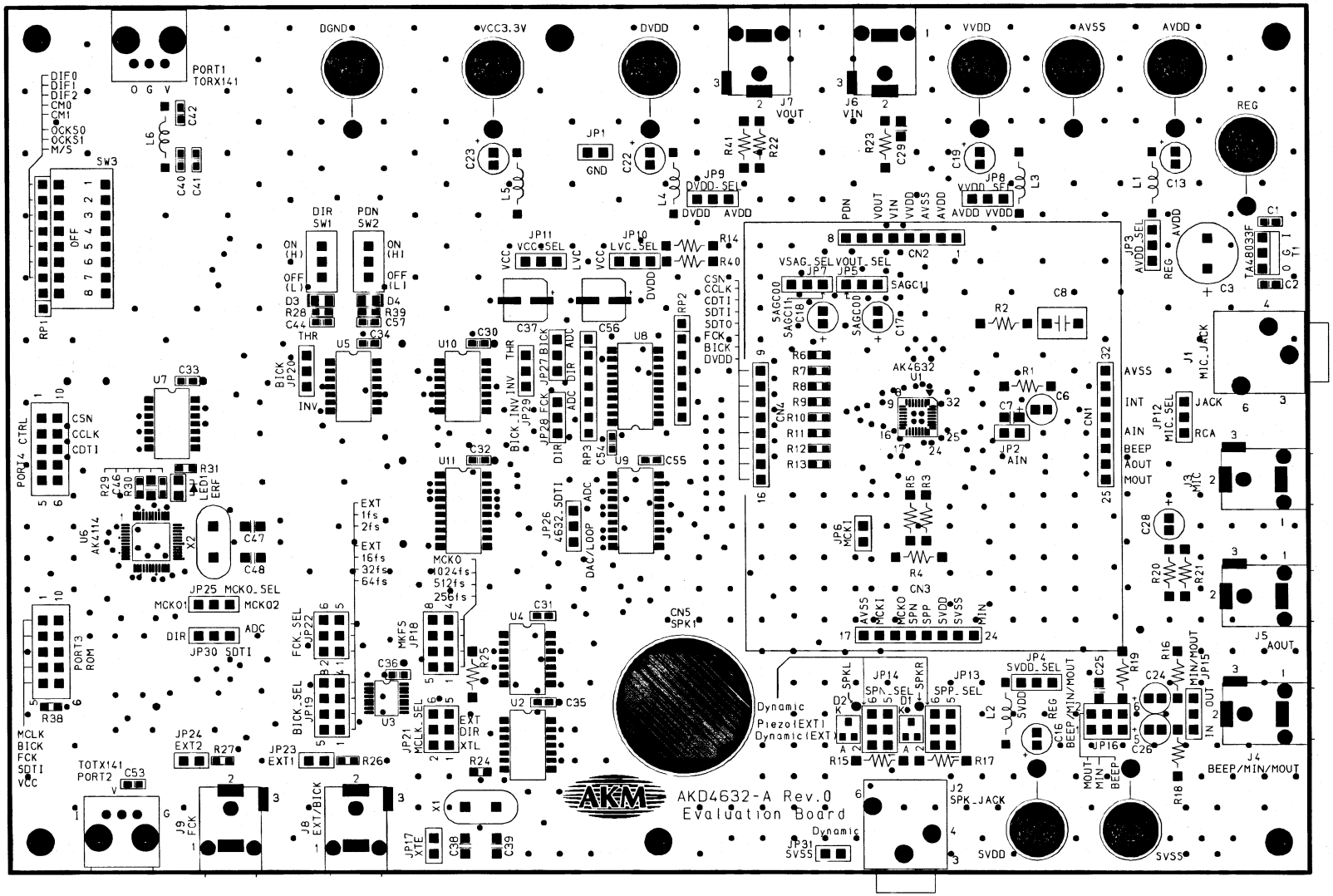
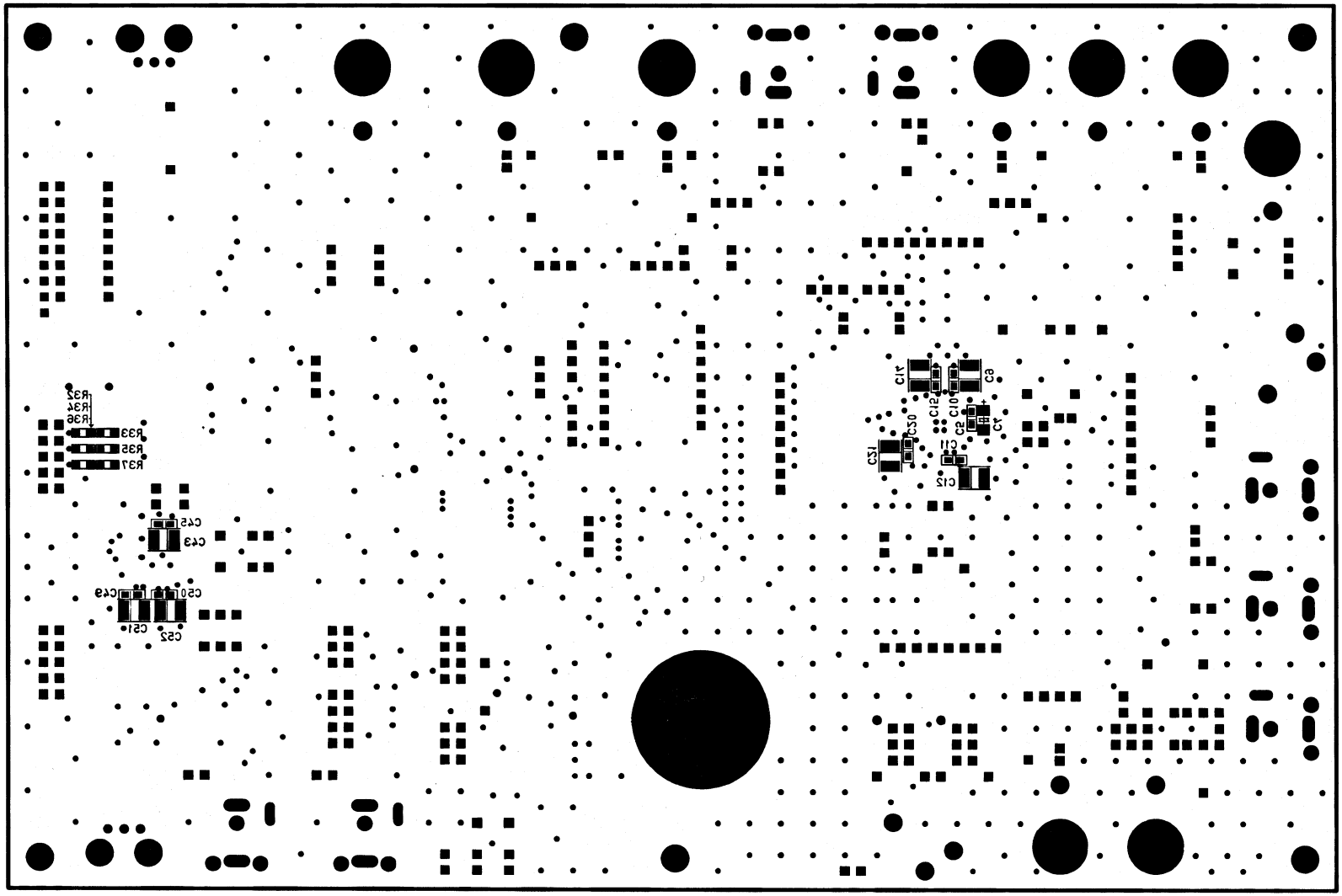
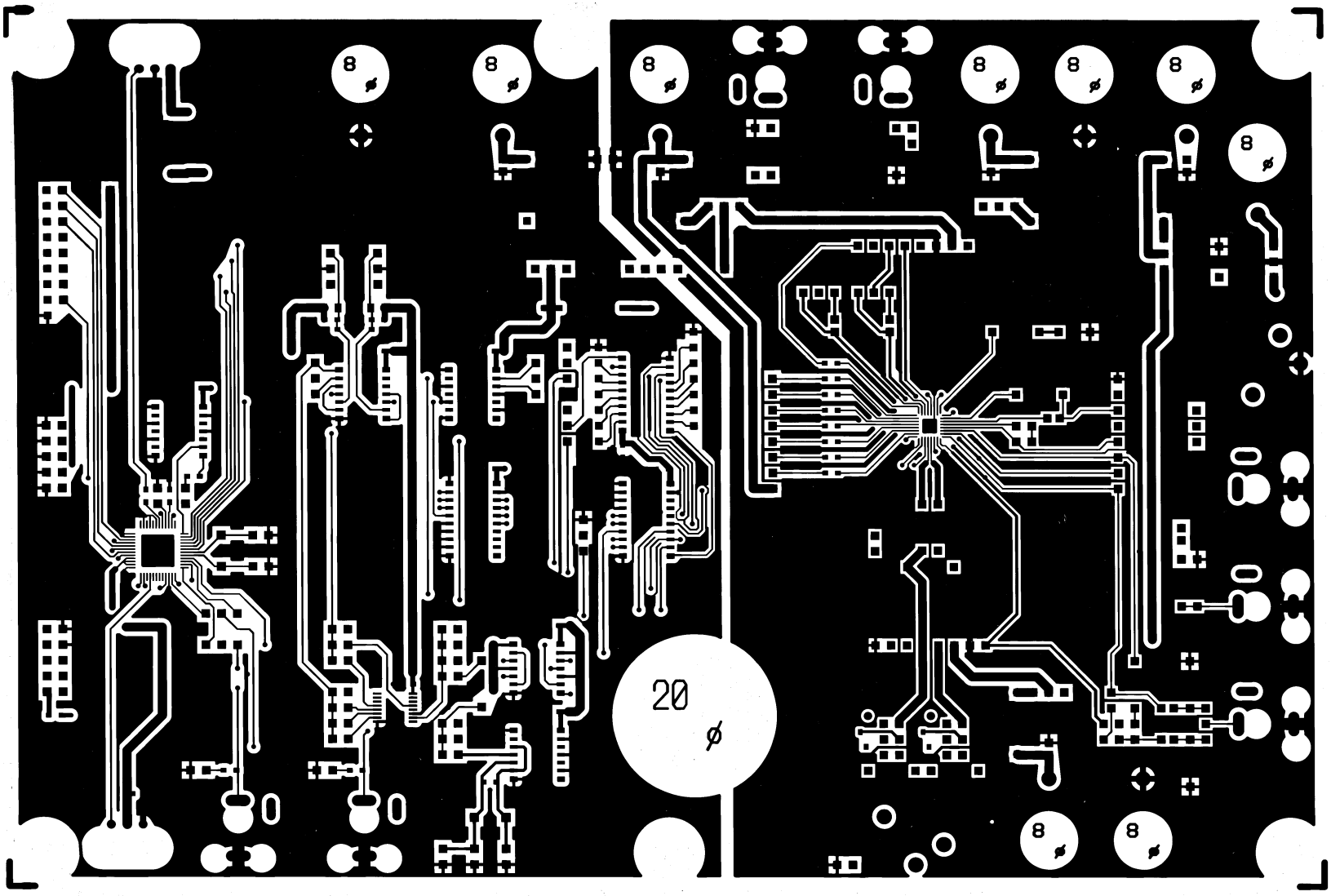
Size A3	Document Number LOGIC	Rev 0
Date: Wednesday, December 22, 2004	Sheet 5 of 5	



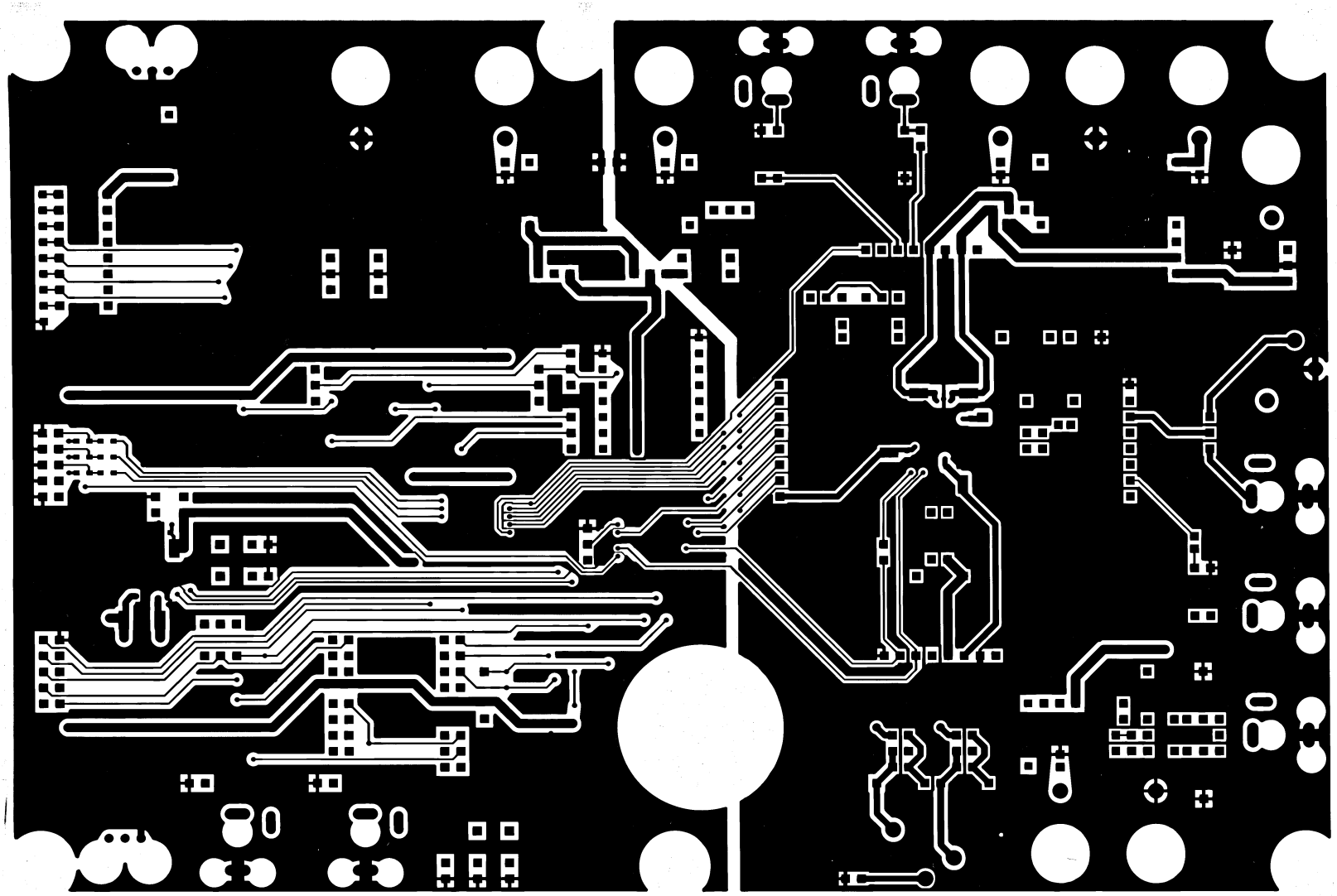
AKD4631-VN　L1 SILK



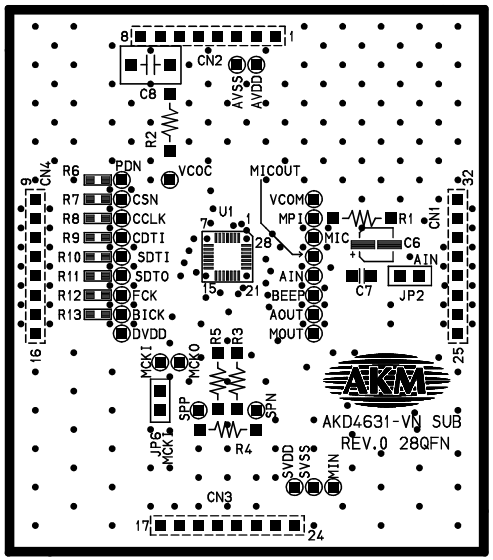
AKD4631-VN　L2 SILK



AKD4631-VN L1

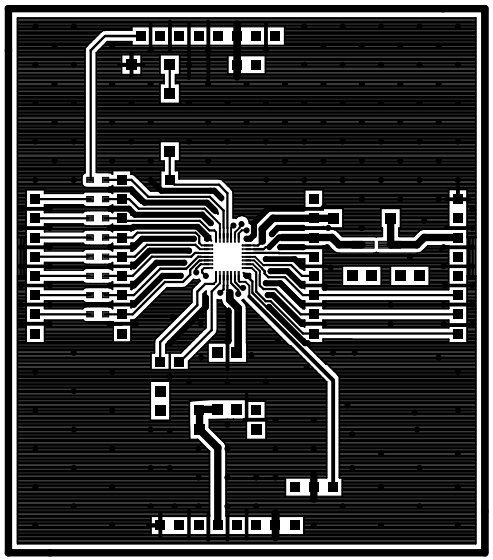


AKD4631-VN L2



AKD4631-VN SUB 28QFN L1 SILK

AKD4631-VN SUB 280FN L2 SILK



AKD4631-VN SUB 28QFN L1

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