



# MOS DIGITAL INTEGRATED CIRCUIT

## $\mu$ PD6529C

6427525 N E C ELECTRONICS INC

72C 09077 D T-49-15-02

### AUTOMOTIVE CLOCK CMOS LSI

#### GENERAL DESCRIPTION

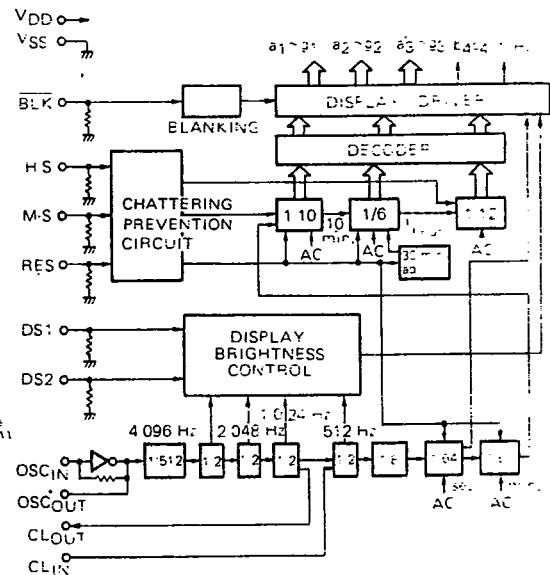
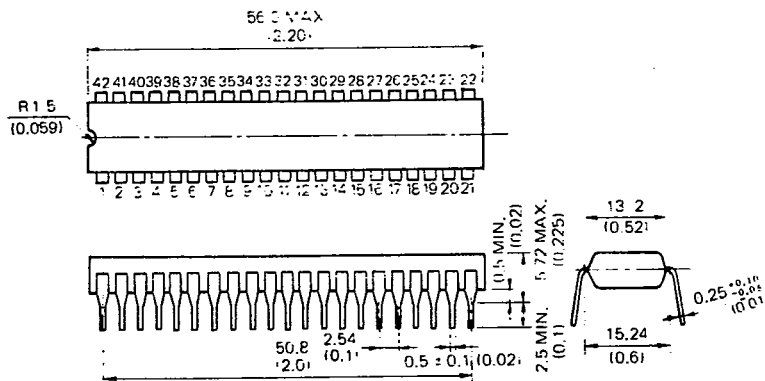
The  $\mu$ PD6529C is a monolithic CMOS LSI for crystal controlled automotive clocks. The circuits interface directly with fluorescent indicator panel. The display format is 12 hours. It is also provided with a 4-ways display brightness control function and can be driven by an external clock signal.

#### FEATURES

- Crystal controlled oscillator (4.194 304 MHz)
- Direct interface to fluorescent indicator panel (FIP4E8S)
- 12 hours display format
- 4-ways display brightness control (duty controlled dimmer 1, 1/4, 1/8, 1/16)
- External clock drive possible (1 024 Hz)
- Separated hours and minutes set controls (2 Hz)
- On the hour adjustment control ( $\pm 30$  minutes)
- 1 024 Hz output
- 42 Pin DIP mold

#### BLOCK DIAGRAM

#### PACKAGE DIMENSIONS in millimeters (inches)

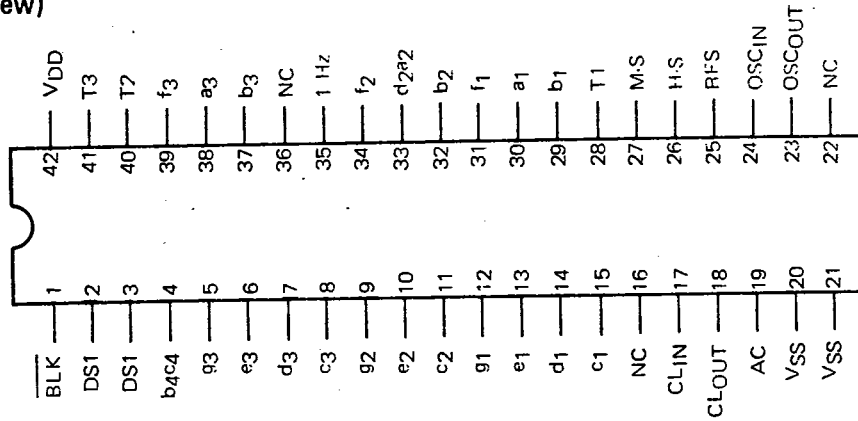


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CONNECTION DIAGRAM  
(Top View)



PIN NO.	SYMBOL		PIN NAME	INTERNAL STATE	PIN NO.	SYMBOL		PIN NAME	INTERNAL STATE
	INPUT	OUTPUT				INPUT	OUTPUT		
1	BLK		Blanking input	Pull down	22		NC		
2	DS1		Dimmer input 1		23		OSCOUT	OSC output	
3	DS2		Dimmer input 2		24		OSCIN	OSC input	
4		b4c4	Segment output	P-ch Open Drain	25		RES	RES input	Pull down
5		a3			26		H-S	Hour adj. input	
6		e3			27		M-S	Minute adj. input	
7		d3			28		T1	Test pin 1	
8		c3			29		b1	Segment output	P-ch Open Drain
9		g2			30		a1		
10		e2			31		f1		
11		c2			32		b2		
12		g1			33		d2a2		
13		e1			34		f2		
14		d1			35		1 Hz	1 Hz signal	
15		c1			36		NC		
16		NC			37		b3	Segment output	P-ch Open Drain
17		CLIN	Ex. Clock input		38		a3		
18		CLOUT	Clock output		39		f3		
19		AC	Clear input	Pull down	40		T2	Test pin 2	
20		VSS	-Power supply		41		T3	Test pin 3	
21		VSS			42		VDD	+Power supply	

**ABSOLUTE MAXIMUM RATINGS (T<sub>a</sub>=25 °C)**

Power supply voltage	V <sub>DD</sub> -V <sub>SS</sub>	-0.3	to	+8.0	V
Input voltage	V <sub>IN</sub>	V <sub>SS</sub> -0.3	to	V <sub>DD</sub> +0.3	V
Output voltage	V <sub>OUT</sub>	V <sub>DD</sub> -20	to	V <sub>DD</sub> +0.3	V
Operating temperature	T <sub>opt</sub>	-40	to	+85	°C
Storage temperature	T <sub>stg</sub>	-55	to	+125	°C

**RECOMMENDED OPERATING CONDITIONS**

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage	V <sub>DD</sub> -V <sub>SS</sub>	3.0	-	7.0	V
High Level Input Voltage	V <sub>IH</sub>	0.7 V <sub>DD</sub>	-	V <sub>DD</sub>	V
Low Level Input Voltage	V <sub>IL</sub>	V <sub>SS</sub>	-	0.3 V <sub>DD</sub>	V
External Clock Duty	CLD	40	50	60	%

**ELECTRICAL CHARACTERISTICS 1 (Unless otherwise noted V<sub>DD</sub>-V<sub>SS</sub>=6.0 V, T<sub>a</sub>=25 °C, RH≤70 %, C<sub>D</sub>=C<sub>G</sub>=15 pF, X<sub>tal</sub>=4.194 304 MHz)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Supply Current	I <sub>DD</sub>	No output loads	-	-	1	mA
High Level Output Current 1, Note 1	I <sub>OH1</sub>	V <sub>DD</sub> -V <sub>SS</sub> =3.0 V, V <sub>DD</sub> -V <sub>OUT</sub> =0.5 V	300	-	-	μA
High Level Output Current 2, Note 2	I <sub>OH2</sub>	V <sub>DD</sub> -V <sub>SS</sub> =3.0 V, V <sub>DD</sub> -V <sub>OUT</sub> =0.5 V	500	-	-	μA
AC Response Time	T <sub>AC</sub>	V <sub>DD</sub> -V <sub>SS</sub> =3.0~7.0 V V <sub>IN</sub> =0.7 V <sub>DD</sub> ~V <sub>DD</sub>	-	-	100	μs
Low Level Output Current, Note 3	I <sub>OL</sub>	V <sub>DD</sub> -V <sub>SS</sub> =3.0 V, V <sub>OUT</sub> -V <sub>SS</sub> =0.5 V	500	-	-	μA
High Level Input Current 1, Note 4	I <sub>IH1</sub>	V <sub>IN</sub> =V <sub>DD</sub>	-	15	30	μA
High Level Input Current 2, Note 5	I <sub>IH2</sub>	V <sub>IN</sub> =V <sub>DD</sub>	-	120	600	μA
Low Level Input Current	I <sub>IL</sub>	V <sub>IN</sub> =V <sub>SS</sub>	-	-	50	μA
External Clock Duty	CLD		40	50	60	%

**ELECTRICAL CHARACTERISTICS 2 (Unless otherwise noted V<sub>DD</sub>-V<sub>SS</sub>=3.0 to 7.0 V, T<sub>a</sub>=-40 to +85 °C, RH≤70 %, C<sub>D</sub>=C<sub>G</sub>=15 pF, X<sub>tal</sub>=4.194 304 MHz)**

CHARACTERISTIC	SYMBOL	TEST CONDITONS	MIN.	TYP.	MAX.	UNIT
Power Supply Current	I <sub>DD</sub>	No output loads	-	-	2	mA
High Level Output Current 1, Note 1	I <sub>OH1</sub>	V <sub>DD</sub> -V <sub>SS</sub> =3.0 V, V <sub>DD</sub> -V <sub>OUT</sub> =0.5 V	250	-	-	μA
High Level Output Current 1, Note 2	I <sub>OH2</sub>	V <sub>DD</sub> -V <sub>SS</sub> =3.0 V, V <sub>DD</sub> -V <sub>OUT</sub> =0.5 V	400	-	-	μA

Note 1) for segments other than those specified in Note 2

Note 2) for segments b4C4 and a2d2, 1 Hz and C<sub>L</sub>OUT

Note 3) for C<sub>L</sub>OUT

Note 4) for DS1, DS2, RES, H·S, M·S, and  $\overline{\text{BLK}}$

Note 5) for T1, T2, T3 and AC

μPD6529C

**INTERFACE SIGNAL DESCRIPTION**

[1] H-S input (pin 26)

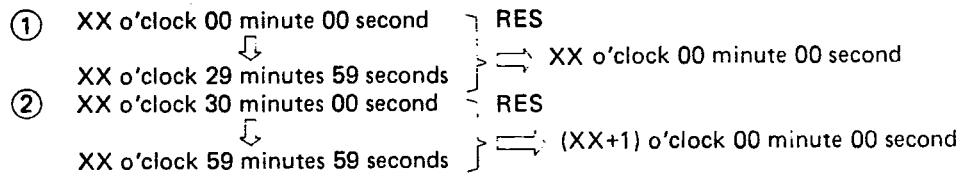
Put this pin (26) to High Level ( $V_{DD}$ ) and the Hour counter is fast fed at 2 Hz. No counting up from Minutes to Hours is provided.

[2] M-S input (pin 27)

Put this pin (27) to High Level ( $V_{DD}$ ) and the Minutes counter is fast fed at 2 Hz. No counting up from Seconds to Minutes is provided.

[3] RES input (pin 25)

Put this pin (25) to High Level ( $V_{DD}$ ) and the adjustment to a right o'clock is made within  $\pm 30$  minutes range, as shown below.



[4] BLK input (pin 1)

Put this pin (25) to Low Level (open) and the display outputs are turned off (Blanking). During Blanking, H-S, M-S and RES inputs are ineffective. Return this pin to High Level and the display outputs are recovered.

[5] DS1 input (pin 2) and DS 2 input (pin 3)

Combine DS1 and DS2 as shwn below and the display brightness is dimmed accordingly.

DS2	DS1	Output ON Duty Ratio	Clock Mode
L	L	1	Internal, External
L	H	1/4	↓
H	L	1/8	
H	H	1/16	↓

- Internal Clock Mode  
4.194 304 MHz crystal oscillator is used.
- External Clock Mode  
1 024 Hz signal is input to CL<sub>IN</sub> pin.

Dimmer Frequency : 512 Hz

[6] AC input (pin 19)

Put this pin to High Level ( $V_{DD}$ ) and this IC is reset to display 1 o'clock 00 minute (00 second).

[7] CL<sub>IN</sub> input (pin 17)

When this IC is to be driven by a crystal oscillator, put this pin to Low Level ( $V_{SS}$ ).

When this IC is to be driven by an external clock, input a 1 024 Hz signal voltage within the specified input voltage range.

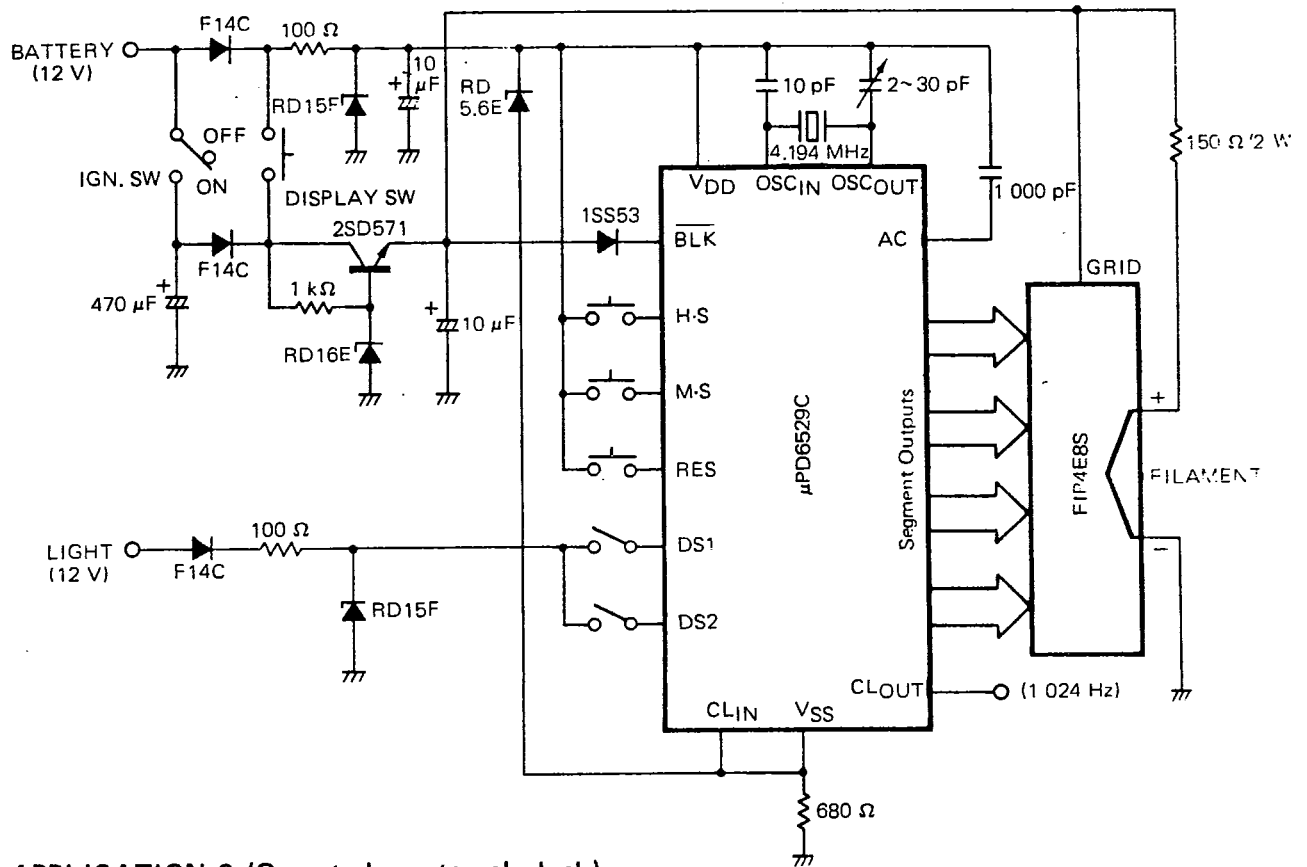
[8] CL<sub>OUT</sub> output (pin 18)

A 1 024 Hz signal with 50 % duty is output on this pin (as a CMOS output). When this IC is operated on an external clock, this output is suppressed.

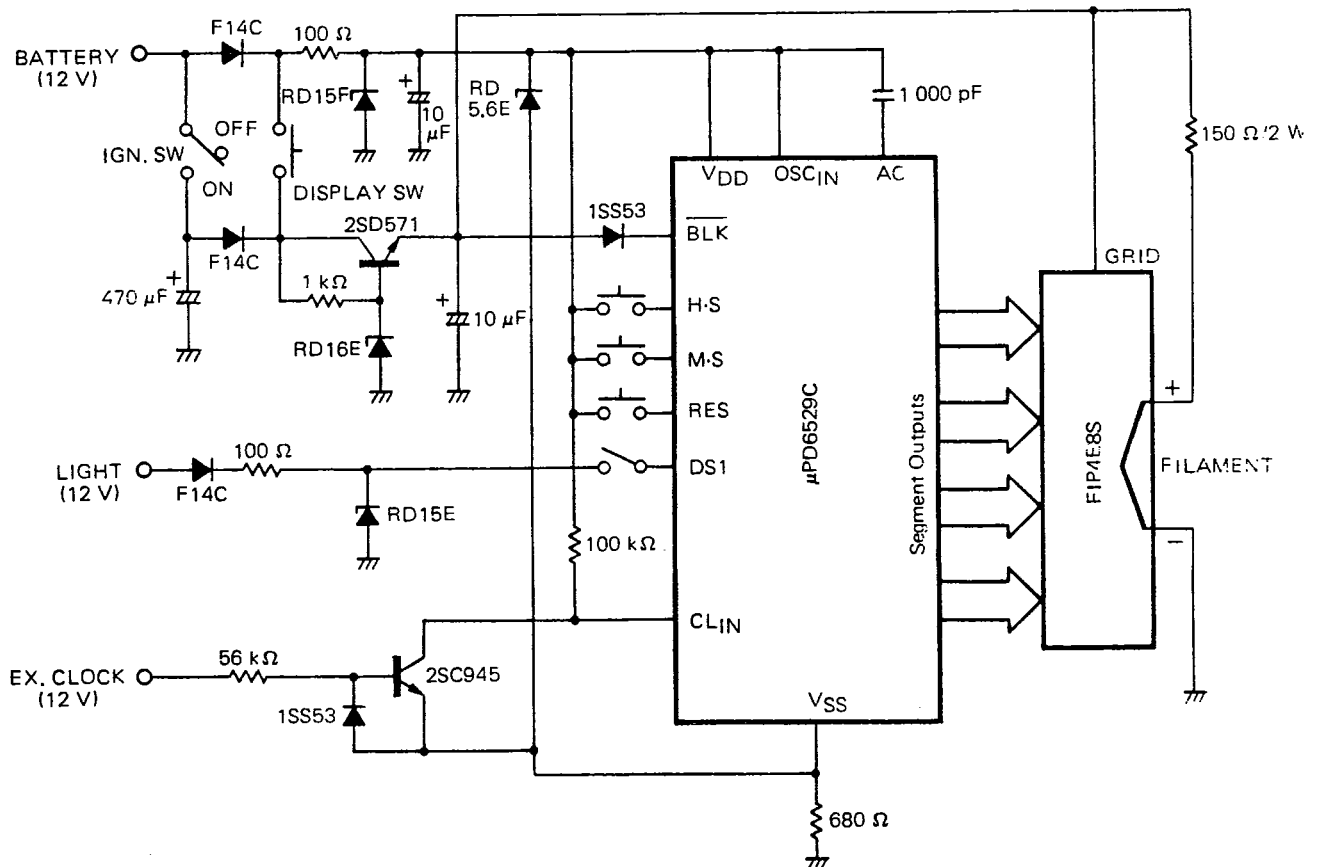
[9] T1 (pin 28), T2 (pin 40) and T3 (pin 41)

These pins are provided for the LSI testing and should be kept on Low Level ( $V_{SS}$ ) during operation.

APPLICATION 1



APPLICATION 2 (Operate by external clock)



$\mu$ PD6529C

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NEC ELECTRON DEVICE

T-49-15-02

NEC cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

The application circuits above shown are not intended to give any mass production design that needs deliberate considerations on possible deviations and thermal dependencies of component parts characteristics.

**Nippon Electric Co., Ltd.**

NEC Building, 33-1, Shiba Gochome, Minato-ku, Tokyo 108, Japan  
Tel: Tokyo 454-1111  
Telex Address: NECTOK J22686  
Cable Address: MICROPHONE TOKYO

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