



Frequency Generator for Modem Systems

General Description

The ICS9117-02 is a low-cost, high-performance frequency generator designed to support fax/data modem systems. Data-pump and UART clocks are synthesized from a microcontroller crystal using high-accuracy, low-jitter PLLs, meeting the frequency tolerance and -96dB signal-to-noise ratios required by 16-bit DSP modem systems. Fast output clock edge rates minimize board induced jitter.

Exact frequency multiplying ratios ensure better than ± 80 ppm frequency accuracy using a standard low cost crystal with external load capacitors (typically $33\text{pF} \pm 5\%$ for an 18pF series load crystal). Achieving ± 80 ppm over four years requires the crystal to have ± 20 ppm initial accuracy, ± 20 ppm temperature and ± 5 ppm/year aging coefficients.

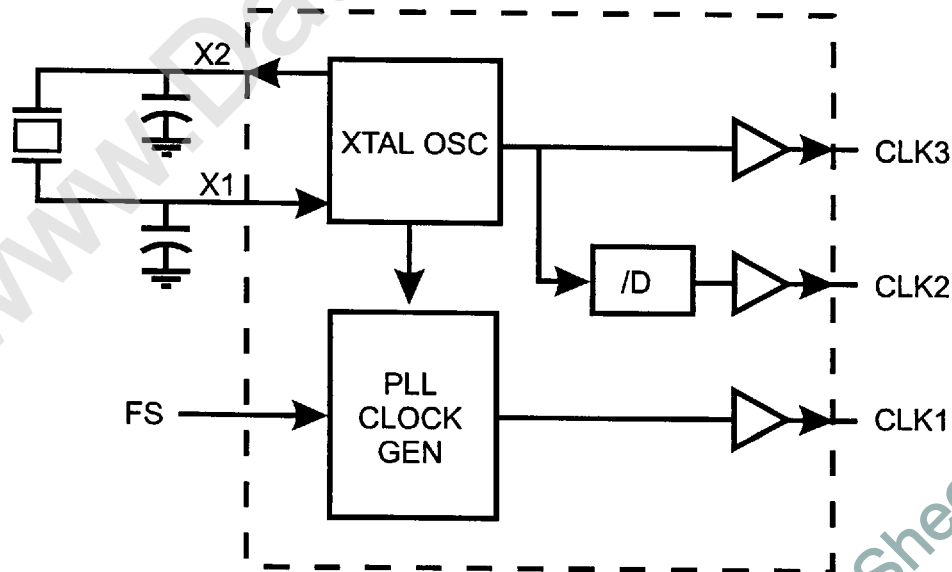
Features

- Generates the 35.2512 MHz microcontroller, 40.320 MHz datapump and selectable microcontroller clocks plus the UART clock.
- Less than ± 80 ppm frequency variation including temperature, voltage, load and aging tolerances
- Single crystal reference minimizes crystal reliability and inventory issues
- 100 ps one sigma jitter maintains 16-bit performance
- Output rise/fall times less than 1.5ns
- On-chip loop filter components
- 3.0V or 5.5V operation
- 8-pin, 150-mil SOIC package

Applications

- Specifically designed to support the high-performance of fax/data modem and WLAN systems.

Block Diagram

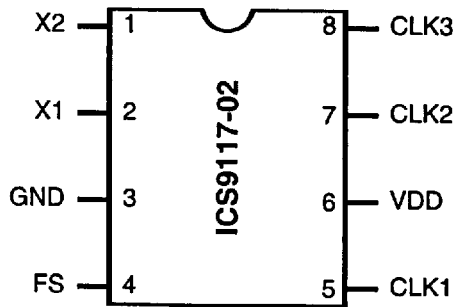


ICS9117-02



Advanced Information

Pin Configuration



Functionality

X1, X2 (MHz)	FS	CLK3 (MHz)	CLK1 (MHz)	CLK2 (MHz)
22.1184	0	22.1184	35.2512	1.8432
44.4000	1	44.4000	40.320	1.8500

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	X2	OUT	22.1 or 44.4 MHz crystal drive output.
2	X1	IN	22.1 or 44.4 MHz crystal or clock input.
3	GND	PWR	Power Gnd
4	FS	IN	Frequency selection inut (see frequency table).
5	CLK1	OUT	datapump clock output.
6	VDD	PWR	+5V or +3.3V power supply.
7	CLK2	OUT	UART clock output.
8	CLK3	OUT	Microcontroller clock output.



Absolute Maximum Ratings

AV _{DD} , V _{DD} referenced to GND	7V
Operating temperature under bias	0 °C to +70 °C
Storage temperature	-65 °C to +150 °C
Voltage on I/O pins referenced to GND	GND - 0.5V to V _{DD} + 0.5V
Power dissipation	0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

Operating V_{DD} = +3.0 V to +3.7V; T_A = 0 °C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V _{IL}		-	-	0.8	V
Input High Voltage	V _{IH}		2.0	-	-	V
Input Low Current	I _{IL}	V _{IN} =0V	-	7.0	-25.0	μA
Input High Current	I _{IH}	V _{IN} =V _{DD}	-	-	5.0	μA
Output Low Voltage	V _{OL} *	I _{OL} =+10mA	-	0.15	0.4	V
Output High Voltage	V _{OH} *	I _{OH} =-10mA	2.4	3.7	-	V
Output Low Current	I _{OL} *	V=0.8V	20.0	35.0	-	mA
Output High Current	I _{OH} *	V=2.4V	-	-20.0	-10.0	mA
Supply Current	I _{CC}	Unloaded	-	14.0	30.0	mA
Pull-up Resistor Value	R _{pu} *		-	400.0	800.0	k ohm
AC Characteristics						
Rise Time	T _r *	150f kiadm 0.8 to 2.0V		1.2	2.0	ns
Fall Time	T _f *	15pF load, 2.0 to 0.8V		1.0	1.5	ns
Lock Time	T _L *	15pF load, 20%to 80%			0	ms
Duty Cycle	D _t *	15pFload @50% of VDD; Except REFCLK	45	50	55	%
Duty Cycle	D _t *	15pF load@50% of VDD; Except REFCLK only	45	50	55	%
Jitter, One Sigma	T _{jis} *	For all frequencies except REFCLK		70	100	ps
Jitter, Absolute	T _{jab} *	For all frequencies except REFCLK	-300		+300	ps
Jitter, One Sigma	T _{jis} *	REFCLK only		200	300	ps
Jitter, Absolute	T _{jab} *	REFCLK only	-500		+500	ps
Input Frequency Range	F _i *		4		28	MHz
Output Frequency Range	F _o *		11.7		+4	MHz
Output Mean Frequency Accuracy vs. Target	F _{oa} *	With 14.318 MHz input	-30		+80	ppm
Power-up Time	T _{pu} *	0 to 33.8 MHz		2.5	4.5	ms
Crystal Input Capacitance	C _{inx} *	X1 (Pin 1) X2 (Pin 8)		18		pF

* Parameter is guaranteed by design and characterization. Not 100% tested in production.



Advanced Information

Absolute Maximum Ratings

V_{DD} , V_{DD} referenced to GND ----- 7V
 Operating temperature under bias ----- 0 °C to +70 °C
 Storage temperature ----- -65 °C to +150 °C
 Voltage on I/O pins referenced to GND ----- GND - 0.5 V to $V_{DD} + 0.5$ V
 Power dissipation ----- 0.5 Watts

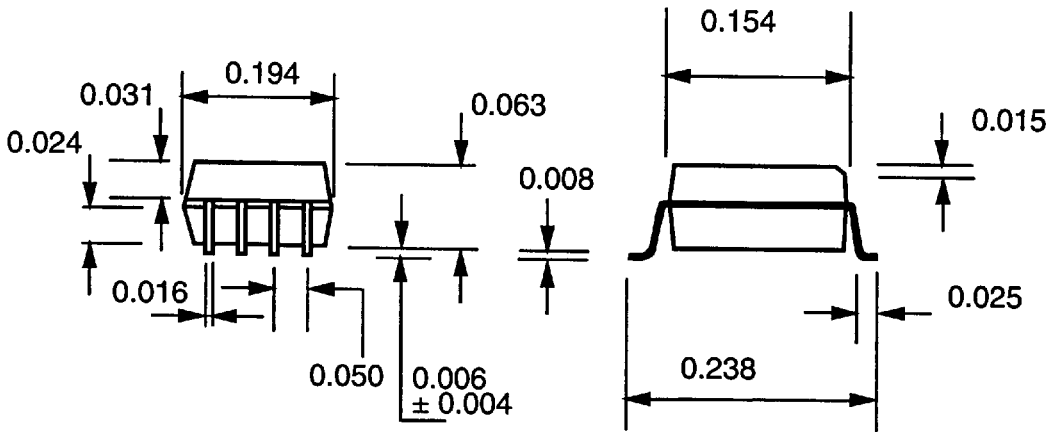
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5.0V-5.5V

Operating $V_{DD} = +3.0$ V to +3.7V; $T_A = 0$ °C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	-	V
Input Low Current	I_{IL}	$V_{IN}=0V$	-	-4.0	-25	μA
Input High Current	I_{IH}	$V_{IN}=V_{DD}$	-	-	5.0	μA
Output Low Voltage	V_{OL}^*	$I_{OL}=+10mA$	-	0.15	0.4	V
Output High Voltage	V_{OH}^*	$I_{OH}=-15mA$	4.0	4.2	-	V
Output Low Current	I_{OL}^*	$V=0.8V$	25.0	40.0	-	mA
Output High Current	I_{OH}^*	$V=2.4V$	-	-85.0	-65	mA
Supply Current	I_{CC}	Unloaded	-	20.0	-35	mA
Pull-up Resistor Value	R_{pu}^*		-	400.0	800.0	k ohm
AC Characteristics						
Rise Time	T_r^*	15o/f kiadm 0.8 to 2.0V		0.8	1.5	ns
Fall Time	T_f^*	15pF load, 2.0 to 0.8V		1.0	2.5	ns
Lock Time	T_L^*	15pF load, 20%to 80%			10	ms
Duty Cycle	D_i^*	15pFload @50% of V_{DD} ; Except REFCLK	45	50	55	%
Duty Cycle	D_i^*	15pF load@50% of V_{DD} ; Except REFCLK only	45	50	55	%
Jitter, One Sigma	T_{jis}^*	For all frequencies except REFCLK		80	100	ps
Jitter, Absolute	T_{jab}^*	For all frequencies except REFCLK	-300		+300	ps
Jitter, One Sigma	T_{jis}^*	REFCLK only		200	250	ps
Jitter, Absolute	T_{jab}^*	REFCLK only	-500		+500	ps
Input Frequency Range	F_i^*		5		4.3	MHz
Output Frequency Range	F_o^*		14		114	MHz
Output Mean Frequency Accuracy vs. Target	F_{oa}^*	With 14.318 MHz input	-80		+80	ppm
Power-up Time	T_{pu}^*	0 to 33.8 MHz		2.5	4.5	ms
Crystal Input Capacitance	C_{inx}^*	X1 (Pin 1) X2 (Pin 8)		18		pF

* Parameter is guaranteed by design and characterization. Not 100% tested in production.



8-Pin SOIC

Ordering Information

ICS9117M-02

Example:

ICS XXXX M-PPP

