

CF003 Series GaAs Pseudomorphic HEMT and MESFET Chips

- ❑ Low Noise Figure: 1.0 dB at 12 GHz
- ❑ High Gain: 10 dB at 12 GHz
- ❑ P_{1dB} Power: +22 dBm at 12 GHz
- ❑ Wide Dynamic Range
- ❑ Active Layers Include:
Pseudomorphic HEMT,
Epitaxial and Ion Implanted
- ❑ Wafer Qualification Procedure
- ❑ Customer Wafer Selection Available

Celeritek CF003 Series Chips

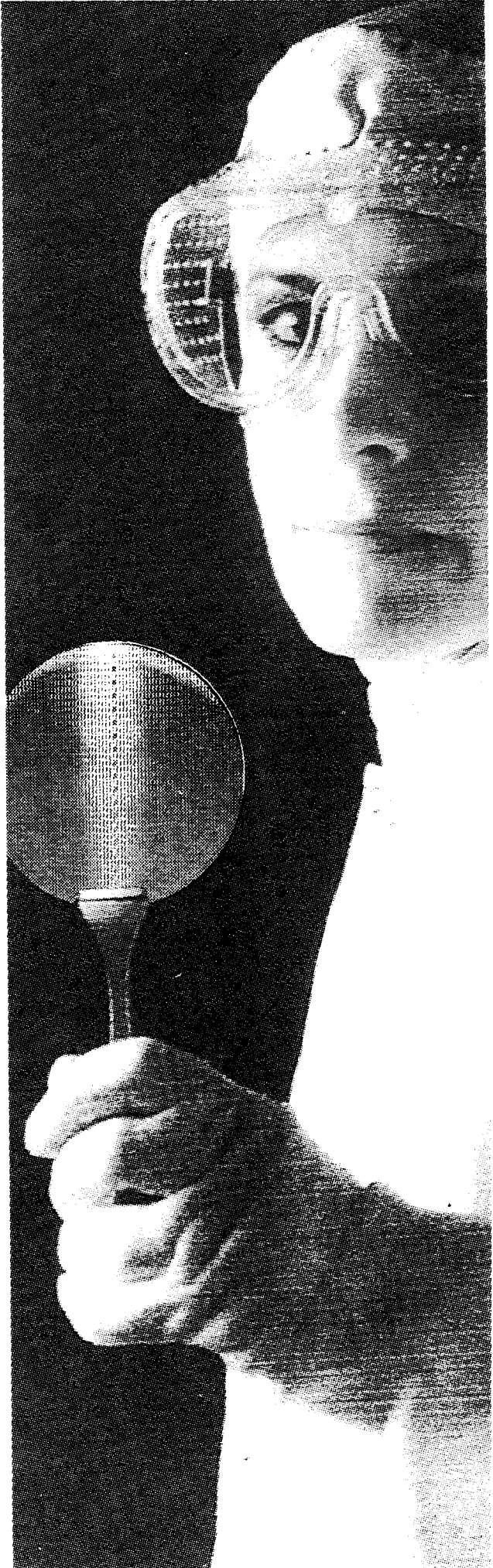
Celeritek CF003 Series chips are GaAs-based transistors which include the CF003-01, CF003-02 and CF003-03 models. They are 600 μm gate width transistors with sub half-micron gate length and Celeritek's proprietary Silicon Nitride passivation.

Celeritek's Wafer Qualification Procedure for CF003 Series FETs consists of DC, RF and reliability testing of both individual die and generic 6 to 18 GHz amplifier modules.

The CF003-01, with its unique straight gate design, provides high gain and medium output power. It is suitable in narrow- and wide-band amplifier applications up to 26 GHz.

The CF003-03 provides low-noise and wide dynamic range up to 26 GHz. It is suitable for narrow- and wide-band amplifiers. Superior g_m also makes this model useful for high gain feed back amplifiers. Its rugged construction allows it to withstand the same input power as conventional MESFETs.

All CF003 Series devices are available in chip form and are suitable for airborne, shipboard and ground-based equipment. Screening includes MIL-STD-750 Class B, Class S and commercial screening. These devices are also available in packaged form. Please consult the CFB003 Series and CFC003 Series data sheets or contact the factory for further information.



CELERITEK

CF003 Series GaAs Chips

Specifications ($T_A = 25^\circ\text{C}$)				CF003-01			CF003-02			CF003-03		
Active Layer				Ion Implanted			Epitaxial			Pseudomorphic HEMT		
Symbol	Parameters and Conditions	Frequency (GHz)	Units	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
NF_{opt}	Optimum Noise Figure $V_{DS} = 3.0\text{ V}$, $I_{DS} = 30\text{ mA}$	12.0	dB		1.8	2.6		1.4	2.0		1.0	1.4
G_a	Gain at NF_{opt} $V_{DS} = 3.0\text{ V}$, $I_{DS} = 30\text{ mA}$	12.0	dB	7.0	8.0		8.0	9.0		9.0	10.0	
$ S_{21} ^2$	50 Ohm Insertion Gain $V_{DS} = 6.0\text{ V}$, $I_{DS} = 80\text{ mA}$	2.0	dB		16.0			17.0			18.0	
		10.0	dB		7.0			8.0			9.0	
		18.0	dB		3.0			4.0			5.0	
P_{1dB}	Power Output @ 1 dB GC $V_{DS} = 6.0\text{ V}$, $I_{DS} = 80\text{ mA}$	12.0	dBm		22.0			20.0			20.0	
g_m	Transconductance $V_{DS} = 3.0\text{ V}$, $V_{GS} = 0\text{ V}$		mS		120			150			180	
I_{DSS}	Drain Current $V_{DS} = 3.0\text{ V}$, $V_{GS} = 0\text{ V}$		mA	120	180	240	120	180	240	120	180	240
V_P	Pinchoff Voltage $V_{DS} = 3.0\text{ V}$, $I_{DS} = 1\text{ mA}$		Volts	-0.7	-1.3	-2.5	-0.7	-1.3	-2.5	-0.7	-1.3	-2.5
BV_{GD}	Breakdown Voltage, Gate-Drain $i_{GD} = 100\text{ }\mu\text{A}$		Volts	-5.5	-8.0		-5.5	-8.0		-5.5	-8.0	
R_{th}	Thermal Resistance		$^\circ\text{C/W}$		80			80			80	

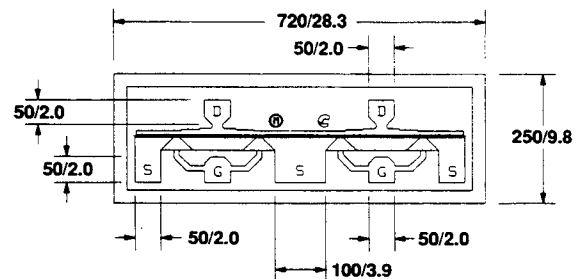
Absolute Maximum Ratings

Parameter	Symbol	Ratings
Drain-Source Voltage	V_{DS}	8V
Gate-Source Voltage	V_{GS}	-5V
Drain Current	I_{DS}	I_{DSS}
Continuous Dissipation	P_T	1600 mW
Channel Temperature	T_{CH}	175 $^\circ\text{C}$
Storage Temperature	T_{STG}	-65 $^\circ\text{C}$ to +175 $^\circ\text{C}$

Typical Noise Parameters - CF003-03 $V_{DS}=3.0\text{V}$, $I_{DS}=30\text{mA}$

Frequency (GHz)	NF_{opt} (dB)	G_a (dB)	Γ_{opt} (Mag)	Γ_{opt} (Ang)	$R_n/50$
2.0	0.38	18.8	0.84	14	0.29
4.0	0.50	15.8	0.70	37	0.19
6.0	0.62	13.6	0.59	61	0.16
8.0	0.74	12.1	0.52	88	0.13
10.0	0.86	11.1	0.48	114	0.09
12.0	0.98	10.4	0.47	141	0.06
14.0	1.10	9.9	0.48	166	0.04
16.0	1.22	9.3	0.49	-171	0.04
18.0	1.34	8.6	0.51	-151	0.07
20.0	1.46	7.4	0.53	-135	0.14

Chip Outline Drawing



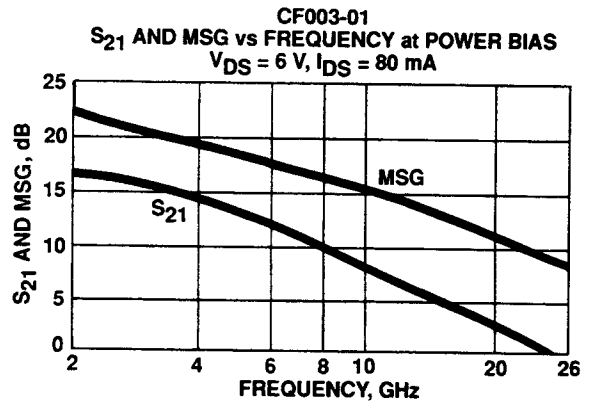
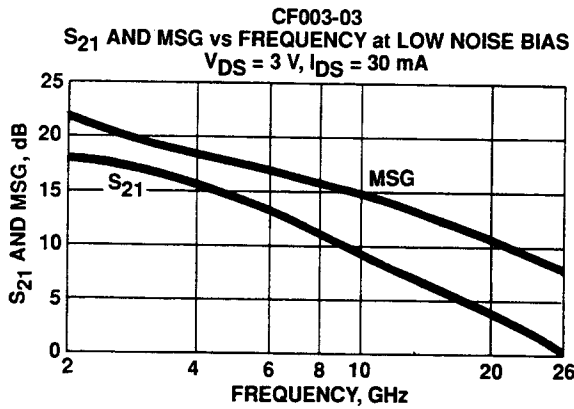
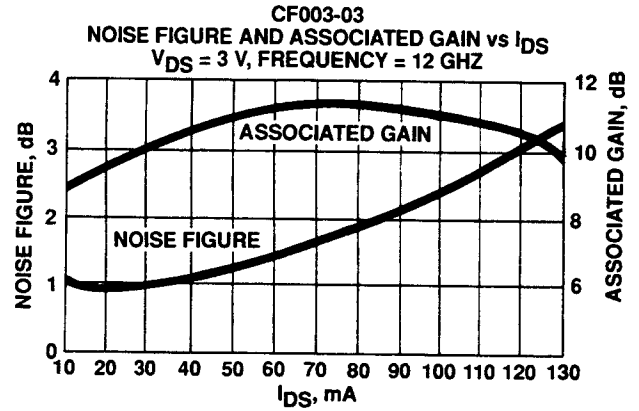
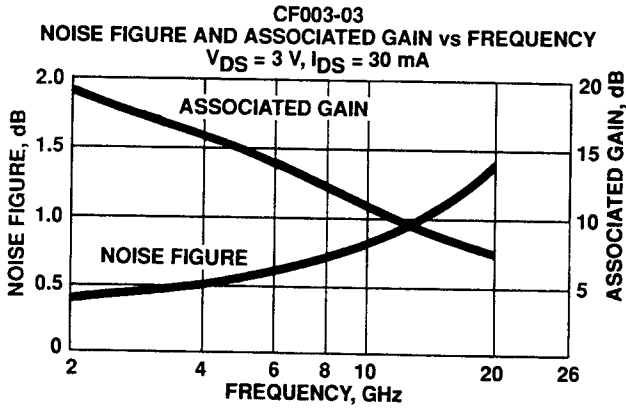
CF003 CHIP (UNITS IN MICRONS/MILS)
THICKNESS: 110 MICRONS/4.3 MILS

Die Attach and Bonding Procedures

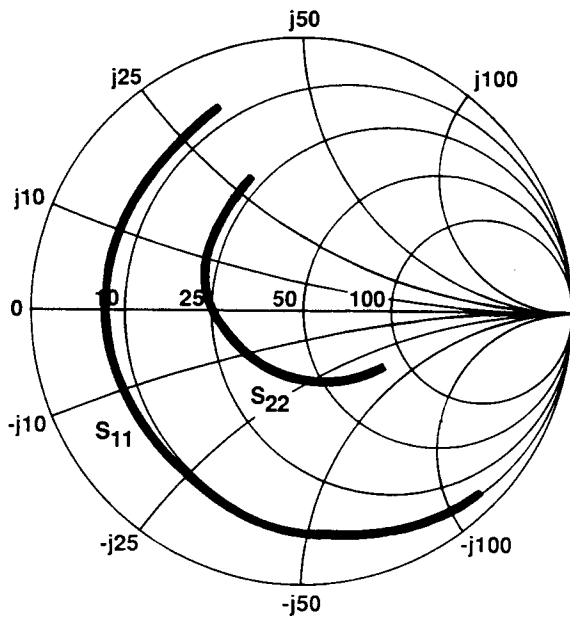
Die Attach: Conductive epoxy or eutectic die attach is recommended. For eutectic die attach: Preform: AuSn (80% Au, 20% Sn); Stage Temperature: 290 $^\circ\text{C}$, $\pm 5^\circ\text{C}$; Handling Tool: Tweezers; Time: 1 min or less.

Wire Bonding: Wire Size: 0.7 to 1.0 mil in diameter (pre-stressed); Thermocompression bonding is preferred over thermosonic bonding. For thermocompression bonding: Stage Temperature: 250 $^\circ\text{C}$; Bond Tip Temperature: 150 $^\circ\text{C}$; Bonding Tip Pressure: 18 to 40 gms depending on size of wire.

Typical Performance ($T_A = 25^\circ\text{C}$)

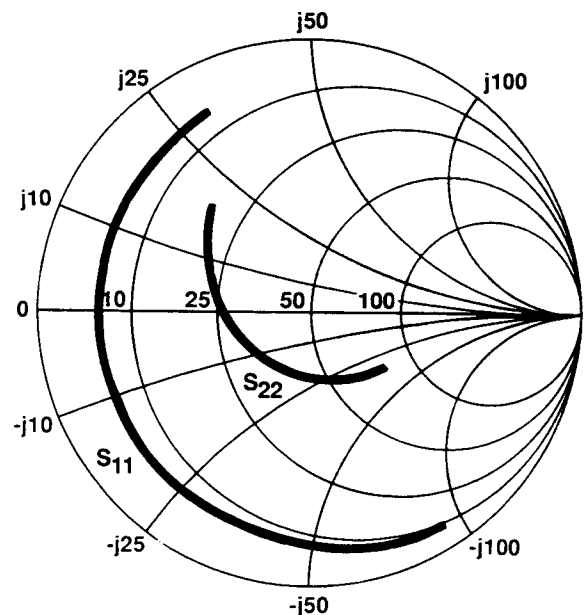


CF003-03
 S_{11} AND S_{22} vs FREQUENCY at LOW NOISE BIAS
 $V_{DS} = 3\text{ V}, I_{DS} = 30\text{ mA}$



FREQUENCY 2.0 to 26.0 GHz

CF003-01
 S_{11} AND S_{22} vs FREQUENCY at POWER BIAS
 $V_{DS} = 6\text{ V}, I_{DS} = 80\text{ mA}$



FREQUENCY 2.0 to 26.0 GHz

CF003 Series GaAs Chips

Typical Scattering Parameters, Common Source (S-Parameters Include Bonding Wire Parasitics)

CF003-01 at Power Bias

$V_{DS} = 6\text{ V}$, $I_{DS} = 80\text{ mA}$

Frequency (GHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂		K	MSG (dB)		
	(Mag)	(Ang)	(dB)	(Mag)	(Ang)	(dB)	(Mag)	(Ang)				
2.0	0.91	-62	16.7	6.86	138	-28.6	0.04	59	0.23	-37	0.38	22.7
4.0	0.83	-108	14.1	5.10	107	-25.1	0.06	41	0.18	-74	0.53	19.6
6.0	0.80	-132	11.8	3.88	88	-24.0	0.06	33	0.17	-90	0.71	17.9
8.0	0.79	-155	9.6	3.01	71	-23.7	0.07	26	0.19	-120	0.88	16.6
10.0	0.78	-172	7.6	2.39	57	-24.1	0.06	24	0.23	-134	1.15	15.8
12.0	0.80	177	6.2	2.03	45	-23.3	0.07	21	0.27	-147	1.10	14.7
14.0	0.80	166	5.0	1.78	33	-23.2	0.07	17	0.31	-156	1.20	14.1
16.0	0.79	150	4.1	1.61	20	-22.1	0.08	14	0.33	-163	1.20	13.1
18.0	0.80	135	3.5	1.49	5	-21.3	0.09	9	0.32	179	1.18	12.4
20.0	0.81	126	2.3	1.31	-10	-20.4	0.10	2	0.36	153	1.19	11.3
22.0	0.87	117	1.1	1.14	-22	-19.6	0.11	-4	0.46	138	0.79	10.3
24.0	0.83	112	-0.7	0.93	-28	-18.9	0.11	-4	0.48	136	1.11	9.1
26.0	0.87	115	-1.4	0.85	-33	-18.1	0.13	-9	0.51	134	0.73	8.3

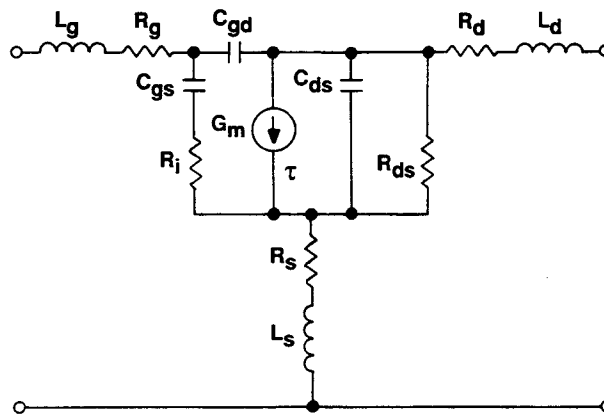
CF003-03 at Low Noise Bias

$V_{DS} = 3\text{ V}$, $I_{DS} = 30\text{ mA}$

Frequency (GHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂		K	MSG (dB)		
	(Mag)	(Ang)	(dB)	(Mag)	(Ang)	(dB)	(Mag)	(Ang)				
2.0	0.92	-58	18.0	7.93	139	-25.7	0.05	60	0.32	-48	0.21	21.9
4.0	0.81	-103	15.5	5.95	109	-22.2	0.08	40	0.24	-94	0.40	18.8
6.0	0.75	-127	13.2	4.55	91	-21.0	0.09	31	0.20	-118	0.56	17.1
8.0	0.73	-151	11.0	3.54	74	-20.7	0.09	24	0.23	-147	0.70	15.8
10.0	0.71	-169	9.0	2.80	61	-21.0	0.09	19	0.27	-159	0.91	15.0
12.0	0.73	180	7.5	2.38	49	-20.5	0.10	16	0.30	-169	0.93	14.0
14.0	0.73	168	6.4	2.08	38	-20.2	0.10	11	0.33	-177	1.01	13.3
16.0	0.73	154	5.5	1.89	26	-19.5	0.11	7	0.33	174	1.04	12.5
18.0	0.74	141	4.8	1.74	12	-18.9	0.11	1	0.33	150	1.06	11.8
20.0	0.76	132	3.7	1.53	-2	-18.2	0.12	-3	0.40	126	1.07	10.9
22.0	0.82	124	2.4	1.32	-13	-17.7	0.13	-9	0.50	114	0.87	10.1
24.0	0.79	118	0.7	1.08	-20	-17.1	0.14	-9	0.51	114	1.05	8.9
26.0	0.84	120	-0.2	0.98	-24	-16.7	0.15	-11	0.53	114	0.84	8.2

Device Model

Parameters	CF003-01 $V_{DS} = 6\text{ V}$, $I_{DS} = 80\text{ mA}$	CF003-03 $V_{DS} = 3\text{ V}$, $I_{DS} = 30\text{ mA}$	Units
L_g	0.21	0.20	nH
R_g	0.50	0.50	Ω
C_{gs}	0.71	0.55	pF
R_i	1.4	1.4	Ω
C_{gd}	0.053	0.068	pF
G_m	134	158	mS
τ	2.8	2.3	ps
C_{ds}	0.16	0.15	pF
R_{ds}	87	92	Ω
R_d	0.67	0.67	Ω
L_d	0.21	0.22	nH
R_s	0.53	0.80	Ω
L_s	0.4	0.05	nH



Wafer Qualification Procedure

100% DC Test 100% Visual Insp.	
Sample Chip Performance Test	NF, Power, S-Parameters, IP3, Power Blast
Sample Circuit Performance Tests 6-18 GHz Module	NF, Power, Gain, VSWR
Reliability Assessment	Power Blast & Burn-In
80% of tested samples must meet specifications for wafer acceptance.	

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Specifications subject to change.

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