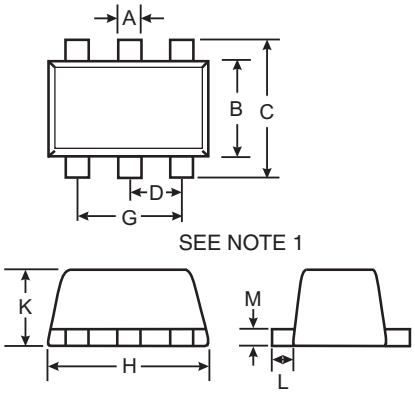
2N7002V/VA

DUAL N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

NEW PRODUCT

Features

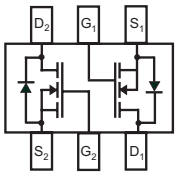
- Dual N-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- **Lead Free By Design/RoHS Compliant (Note 3)**



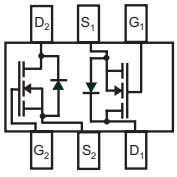
SOT-563			
Dim	**Min**	**Max**	**Typ**
A	0.15	0.30	0.25
B	1.10	1.25	1.20
C	1.55	1.70	1.60
D		0.50	
G	0.90	1.10	1.00
H	1.50	1.70	1.60
K	0.56	0.60	0.60
L	0.10	0.30	0.20
M	0.10	0.18	0.11
All Dimensions in mm			

Mechanical Data

- Case: SOT-563
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Terminals Connections: See Diagram
- Terminals: Finish - Matte Tin annealed over Alloy 42 leadframe. Solderable per MIL-STD-202, Method 208
- Terminals: Lead bearing terminal plating available. See Ordering information Page 2, Note 6
- Marking: See Page 2
- Ordering & Date Code Information: See Page 2
- Weight: 0.006 grams (approximate)



2N7002V
(KAS Marking Code)



2N7002VA
(KAY Marking Code)

Maximum Ratings @ T_A = 25°C unless otherwise specified

Characteristic		Symbol	Value	Units
Drain-Source Voltage		V_{DSS}	60	V
Drain-Gate Voltage $R_{GS} \leq 1.0M\Omega$		V_{DGR}	60	V
Gate-Source Voltage (Note 3)	Continuous Pulsed	V_{GSS}	±20 ±40	V
Drain Current (Note 3)	Continuous	I_D	280	mA
Drain Current (Note 3)	Pulsed	I_{DM}	1.5	A
Total Power Dissipation		P_d	150	mW
Thermal Resistance, Junction to Ambient		$R_{\theta JA}$	833	°C/W
Operating and Storage Temperature Range		T_j, T_{STG}	-55 to +150	°C

Notes:
1. Package is non-polarized. Parts may be on reel in orientation illustrated, 180° rotated, or mixed (both ways).
2. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch; pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.
3. No purposefully added Lead.

NEW PRODUCT

Electrical Characteristics @ T_A = 25°C unless otherwise specified

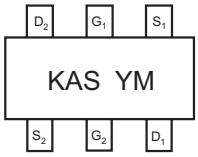
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 4)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	70	—	V	V_{GS} = 0V, I_D = 10μA
Zero Gate Voltage Drain Current @ T_C = 25°C @ T_C = 125°C	I_{DSS}	—	—	1.0 500	μA	V_{DS} = 60V, V_{GS} = 0V
Gate-Body Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 4)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	—	2.5	V	V_{DS} = V_{GS}, I_D = 250μA
Satic Drain-Source On-Resistance	$R_{DS\ (ON)}$	— —	— —	7.5 13.5	Ω	V_{GS} = 5V, I_D = 0.05A, V_{GS} = 10V, I_D = 0.5A, T_j = 125°C
On-State Drain Current	$I_{D(ON)}$	0.5	1.0	—	A	V_{GS} = 10V, V_{DS} = 7.5V
Forward Transconductance	g_{FS}	80	—	—	mS	V_{DS} = 10V, I_D = 0.2A
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	—	—	50	pF	V_{DS} = 25V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	—	25	pF	
Reverse Transfer Capacitance	C_{rss}	—	—	5.0	pF	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$	—	—	20	ns	V_{DD} = 30V, I_D = 0.2A, R_L = 150Ω, V_{GEN} = 10V, R_{GEN} = 25Ω
Turn-Off Delay Time	$t_{D(OFF)}$	—	—	20	ns	

Ordering Information (Note 5)

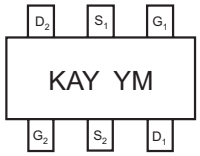
Device	Packaging	Shipping
2N7002V-7	SOT-563	3000/Tape & Reel
2N7002VA-7	SOT-563	3000/Tape & Reel
2N7002V-7-L	SOT-563	3000/Tape & Reel
2N7002VA-7-L	SOT-563	3000/Tape & Reel

Notes: 4. Short duration test pulse used to minimize self-heating effect.
5. For Packaging Details, go to our website at http://www.diodes.com/datasheets/ap02007.pdf.
6. "-L" suffix on part number indicates Pb/Sn terminal plating. "-L" version is a Non Lead-Free, Non RoHS-compliant device.

Marking Information



KAS = 2N7002V Product Type Marking Code (See Note 1)
YM = Date Code Marking
Y = Year ex: R = 2004
M = Month ex: 9 = September



KAY = 2N7002VA Product Type Marking Code (See Note 1)
YM = Date Code Marking
Y = Year ex: R = 2004
M = Month ex: 9 = September

Date Code Key

Year	2004	2005	2006	2007	2008	2009
Code	R	S	T	U	V	W

Month	Jan	Feb	March	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

NEW PRODUCT

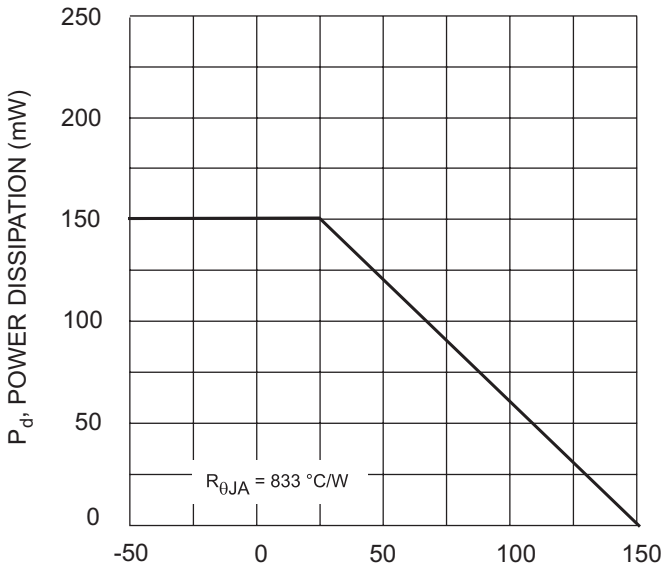


Fig. 1, Derating Curve - Total