Dual Digital Controlled Potentiometers (XDCP™) X95820

FEATURES

- **Two potentiometers in one package**
- **256 resistor taps–0.4% resolution**
- **2-wire serial interface**
- **Wiper resistance: 70Ω typical @ 3.3V**
- **Non-volatile storage of wiper position**
- **Standby current < 5µA max**
- **Power supply: 2.7V to 5.5V**
- **50kΩ, 10kΩ total resistance**
- **High reliability**
  - **—Endurance: 150,000 data changes per bit per register**
  - **—Register data retention: 50 years @ T ≤ 75°C**
- **14-lead TSSOP, 14-pin FCP (Flip-Chip Package)**

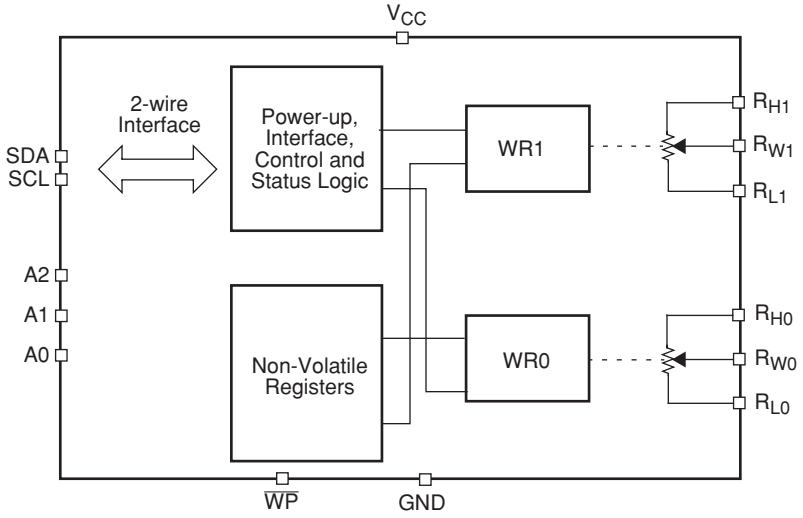
DESCRIPTION

The X95820 integrates two digitally controlled potentiometers (XDCP) on a monolithic CMOS integrated circuit.

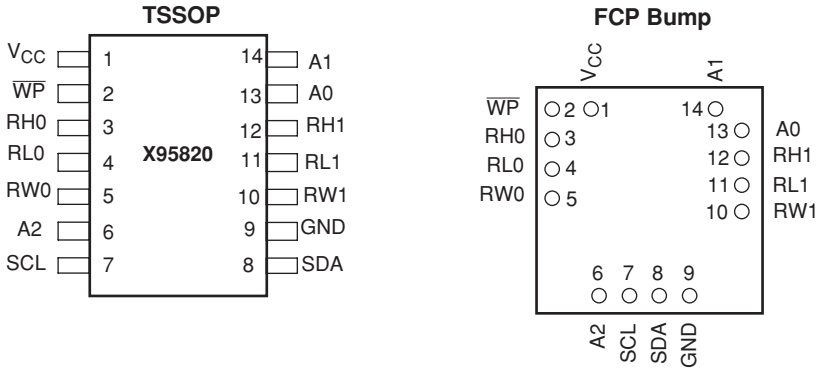
The digitally controlled potentiometers are implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the 2-wire bus interface. Each potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR), that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. At power up the device recalls the contents of the two DCP's IVR to the corresponding WRs.

The DCPs can be used as three-terminal potentiometers or as two-terminal variable resistors in a wide variety of applications including control, parameter adjustments, and signal processing.

BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFO

Ordering Number	Package	Resistance Option
X95820WV14I-2.7	14-lead TSSOP	10kΩ
X95820UV14I-2.7	14-lead TSSOP	50kΩ
X95820WX14I-2.7	14-pin Flip-Chip	10kΩ
X95820UX14I-2.7	14-pin Flip-Chip	50kΩ

PIN ASSIGNMENTS

Pin	Symbol	Description
1	V_{CC}	Power supply pin
2	$\overline{WP}$	Hardware write protection pin. Active low. Prevents any “Write” operation of the 2-wire interface.
3	RH0	“High” terminal of DCP0
4	RL0	“Low” terminal of DCP0
5	RW0	“Wiper” terminal of DCP0
6	A2	Device address for the 2-wire interface
7	SCL	2-wire interface clock
8	SDA	Serial data I/O for the 2-wire interface
9	GND	Ground
10	RW1	“Wiper” terminal of DCP1
11	RL1	“Low” terminal of DCP1
12	RH1	“High” terminal of DCP1
13	A0	Device address for the 2-wire interface
14	A1	Device address for the 2-wire interface

ABSOLUTE MAXIMUM RATINGS

Storage temperature .....–65°C to +150°C
Voltage at any digital interface pin
with respect to GND .....–0.3V to V_{CC}+0.3
V_{CC} .....–0.3V to +6V
Voltage at any DCP pin with
respect to GND .....–0.3V to V_{CC}
Lead temperature (soldering, 10 seconds).....300°C
I_W (10 seconds)..... ±6mA

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Industrial	–40°C	+85°C

Parameter	Limits
V_{CC}	2.7V to 5.5V
Power rating of each DCP	5 mW
Wiper current of each DCP	±3.0 mA

ANALOG CHARACTERISTICS

(Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.(1)	Max.	Unit	
R_{TOTAL}	R_H to R_L resistance		10, 50		kΩ	W, U versions respectively
	R_H to R_L resistance tolerance	-20		+20	%	
R_W	Wiper resistance		70	200	Ω	VCC = 3.3V @ 25C Wiper current = V_{CC} / R_{TOTAL}
$C_H/C_L/C_W$	Potentiometer Capacitance(15)		10/10/25		pF	
I_{LkgDCP}	Leakage on DCP pins(15)		0.1	1	µA	Voltage at pin from GND to V_{CC}
Voltage Divider Mode (0V @ RL_i; V_{CC} @ RH_i; measured at RW_i, unloaded; i = 0 or 1)						
INL(6)	Integral non-linearity	-1		1	LSB(2)	
DNL(5)	Differential non-linearity	-0.5		0.5	LSB(2)	Monotonic over all tap positions
ZSerror(3)	Zero-scale error	0	1	7	LSB(2)	U option
		0	0.5	2		W option
FSerror(4)	Full-scale error	-7	-1	0	LSB(2)	U option
		-2	-1	0		W option
V_{MATCH}(7)	DCP to DCP matching	-2		2	LSB(2)	Any two DCPs at same tap position, same voltage at all RH terminals, and same voltage at all RL terminals
TC_V(8)	Ratiometric Temperature Coefficient		±4		ppm/°C	DCP Register set to 80 hex
Resistor Mode (Measurements between RW_i and RL_i with RH_i not connected, or between RW_i and RH_i with RL_i not connected. i = 0 or 1)						
RINL(12)	Intregal non-linearity	-1		1	MI(9)	DCP register set between 20 hex and FF hex. Monotonic over all tap positions
RDNL(11)	Differential non-linearity	-0.5		0.5	MI(9)	
Roffset(10)	Offset	0	1	7	MI(9)	DCP Register set to 00 hex
		0	0.5	2	MI(9)	
R_{MATCH}(13)	DCP to DCP Matching	-2		2	MI(9)	Any two DCPs at the same tap position with the same terminal voltages.
TC_R(14)	Resistance Temperature Coefficient		±45		ppm/°C	DCP register set between 20 hex and FF hex

OPERATING CHARACTERISTICS

(Over the recommended operating conditions unless otherwise specified.)

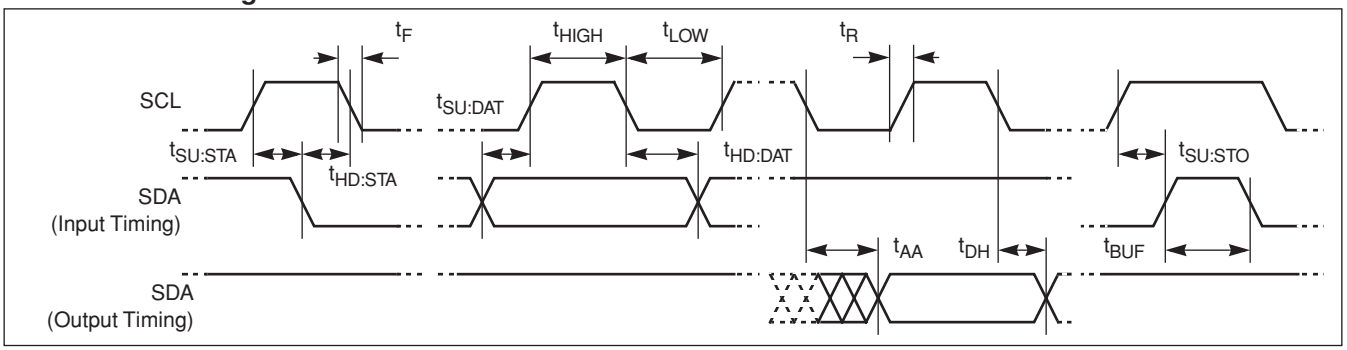
Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.[1]	Max.	Units	
I_{CC1}	V_{CC} supply current (Volatile write/read)			1	mA	f_{SCL} = 400kHz;SDA = Open; (for 2-Wire, Active, Read and Volatile Write States only)
I_{CC2}	V_{CC} supply current (nonvolatile write)			3	mA	f_{SCL} = 400kHz; SDA = Open; (for 2-Wire, Active, Nonvolatile Write State only)
I_{SB}	V_{CC} current (standby)			5	µA	V_{CC} = +5.5V, 2 Wire Interface in Standby State
				2	µA	V_{CC} = +3.6V, 2 Wire Interface in Standby State
I_{LkgDig}	Leakage current, at pins A0, A1, A2, SDA, SCL, and $\overline{WP}$ pins	-10		10	µA	Voltage at pin from GND to V_{CC}
t_{DCP}[15]	DCP wiper reponse time			1	µs	SCL falling edge of last bit of DCP Data Byte to wiper change
Vpor	Power-on recall voltage	1.8		2.6	V	Minimum V_{CC} at which memory recall occurs
VccRamp	V_{CC} ramp rate	0.2			V/ms	
t_D[15]	Power up delay			3	ms	V_{CC} above Vpor, to DCP Initial Value Register recall completed, and 2-Wire Interface in standby state
EEPROM Specs						
	EEPROM Endurance	150,000			Cycles	
	EEPROM Retention	50			Years	Temperature ≤ 75°C
Serial Interface Specs						
V_{IL}	$\overline{WP}$, A2, A1, A0, SDA, and SCL input buffer LOW voltage	-0.3		0.3*Vcc	V	
V_{IH}	$\overline{WP}$, A2, A1, A0, SDA, and SCL input buffer HIGH voltage	0.7*Vcc		Vcc+0.3	V	
Hysterisis[15]	SDA and SCL input buffer hysterisis	0.05* Vcc			V	
V_{OL}[15]	SDA output buffer LOW voltage, sinking 4 mA	0		0.4	V	
Cpin[15]	$\overline{WP}$, A2, A1, A0, SDA, and SCL pin capacitance			10	pF	
f_{SCL}	SCL frequency			400	kHz	
t_{IN}[15]	Pulse width suppression time at SDA and SCL inputs			50	ns	Any pulse narrower than the max spec is suppressed.
t_{AA}[15]	SCL falling edge to SDA output data valid			900	ns	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window.
t_{BUF}[15]	Time the bus must be free before the start of a new transmission	1300			ns	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition.
t_{LOW}	Clock LOW time	1300			ns	Measured at the 30% of V_{CC} crossing.
t_{HIGH}	Clock HIGH time	600			ns	Measured at the 70% of V_{CC} crossing.
$t_{SU:STA}$	START condition setup time	600			ns	SCL rising edge to SDA falling edge. Both crossing 70% of V_{CC}.
$t_{HD:STA}$	START condition hold time	600			ns	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}.
$t_{SU:DAT}$	Input data setup time	100			ns	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}

OPERATING CHARACTERISTICS

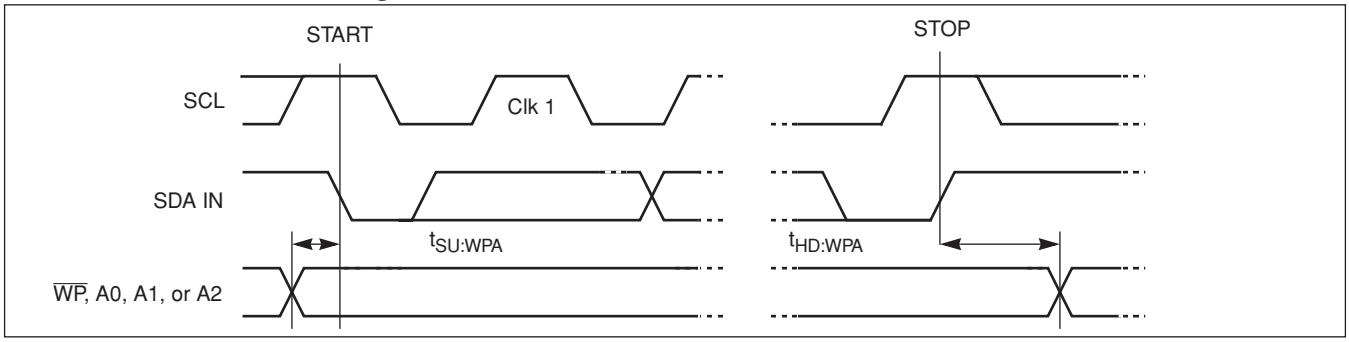
(Over the recommended operating conditions unless otherwise specified.) (Continued)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.[1]	Max.	Units	
$t_{HD:DAT}$	Input data hold time	0			ns	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window.
$t_{SU:STO}$	STOP condition setup time	600			ns	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}.
$t_{HD:STO}$	STOP condition setup time	600			ns	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}.
t_{DH}(15)	Output data hold time	0			ns	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window.
t_R(15)	SDA and SCL rise time	20 + 0.1 * Cb		250	ns	From 30% to 70% of V_{CC}
t_F(15)	SDA and SCL fall time	20 + 0.1 * Cb		250	ns	From 70% to 30% of V_{CC}
Cb(15)	Capacitive loading of SDA or SCL	10		400	pF	Total on-chip and off-chip
Rpu(15)	SDA and SCL bus pull-up resistor off-chip	1			kΩ	Maximum is determined by t_R and t_F. For Cb = 400 pF, max is about 2~2.5 kΩ. For Cb = 40 pF, max is about 15~20 kΩ
t_{WP}(15) (16)	Non-volatile Write cycle time		12	20	ms	
$t_{SU:WPA}$	A2, A1, A0, and $\overline{WP}$ setup time	600			ns	Before START condition
$t_{HD:WPA}$	A2, A1, A0, and $\overline{WP}$ hold time	600			ns	After STOP condition

SDA vs. SCL Timing



$\overline{WP}$, A0, A1, and A2 Pin Timing



Notes: (1) Typical values are for T_A = 25°C and 3.3V supply voltage.

(2) LSB: $[V(RW)_{255} - V(RW)_0] / 255$. $V(RW)_{255}$ and $V(RW)_0$ are V(RW) for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.

(3) ZS error = $V(RW)_0$ / LSB.

(4) FS error = $[V(RW)_{255} - V_{CC}]$ / LSB.

(5) DNL = $[V(RW)_i - V(RW)_{i-1}]$ / LSB-1, for i = 1 to 255. i is the DCP register setting.

(6) INL = $V(RW)_i - (i \bullet LSB - V(RW)_0)$ for i = 1 to 255.

(7) $V_{MATCH} = [V(RWx)_i - V(RWy)_i]$ / LSB, for i = 0 to 255, x = 0 to 1 and y = 0 to 1.

(8) $$TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{125°C}$$

for i = 16 to 240 decimal, T = -40°C to 85°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.

(9) $MI = |R_{255} - R_0| / 255$. R_{255} and R_0 are the measured resistances for the DCP register set to FF hex and 00 hex respectively.

(10) Roffset = R_0 / MI, when measuring between RW and RL.
Roffset = R_{255} / MI, when measuring between RW and RH.

(11) RDNL = $(R_i - R_{i-1}) / MI$, for i = 32 to 255.

(12) RINL = $[R_i - (MI \bullet i) - R_0] / MI$, for i = 32 to 255.

(13) $R_{MATCH} = (R_{i,x} - R_{i,y}) / MI$, for i = 0 to 255, x = 0 to 1 and y = 0 to 1.

(14) $$TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{125°C}$$

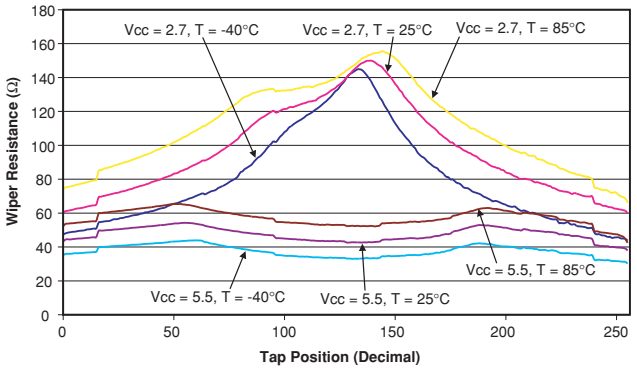
for i = 32 to 255, T = -40°C to 85°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.

(15) This parameter is not 100% tested.

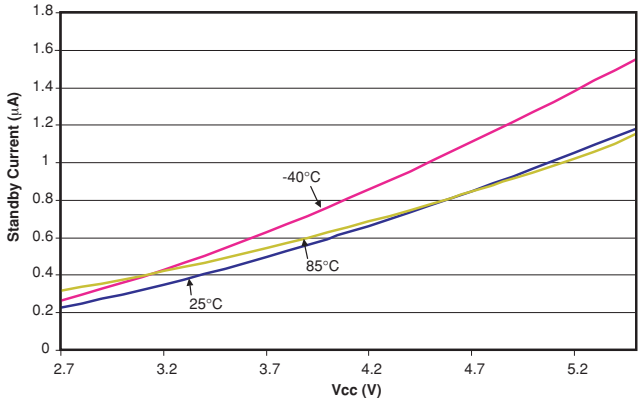
(16) t_{WC} is the minimum cycle time to be allowed for any non-volatile Write by the user, unless Acknowledge Polling is used. It is the time from a valid STOP condition at the end of a Write sequence of a 2-wire serial interface Write operation, to the end of the self-timed internal non-volatile write cycle.

GRAPHS

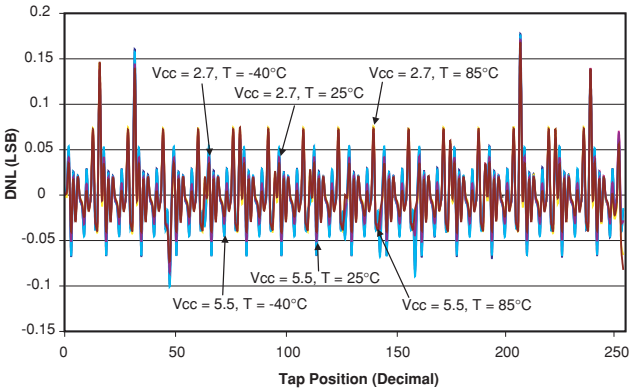
Wiper Resistance vs. Tap Position (Voltage Divider) RL= 0V, RH = Vcc



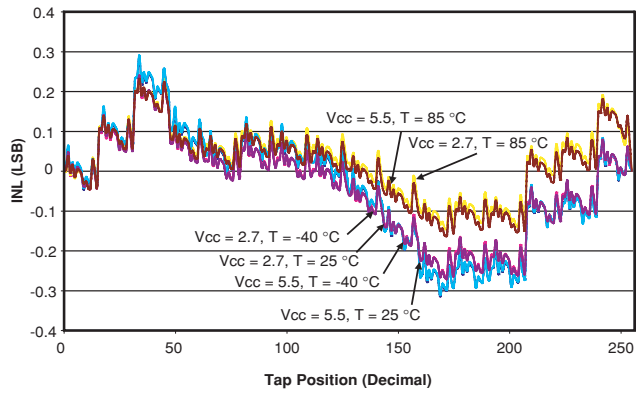
Standby Current vs. Vcc



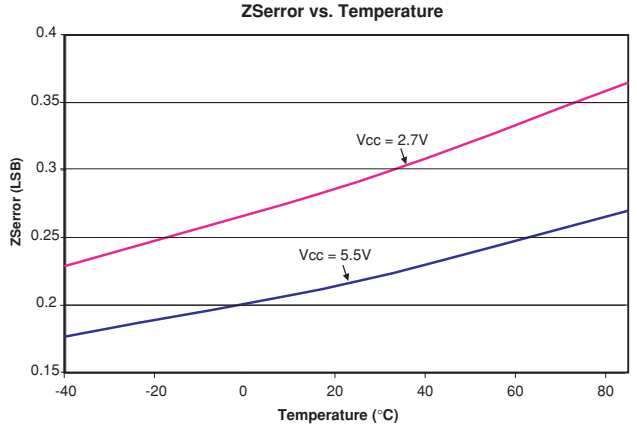
DNL vs. Tap Position in Voltage Divider Mode



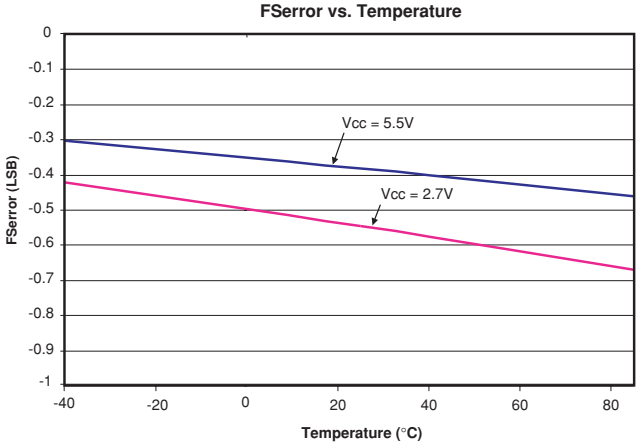
INL vs. Tap Position in Voltage Divider Mode



ZSerror vs. Temperature



FSerror vs. Temperature



PRINCIPLES OF OPERATION

The X95820 in as integrated circuit incorporating two DCPs with their associated registers, non-volatile memory, and a 2-wire serial interface providing direct communication between a host and the potentiometers and memory.

DCP Description

Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RH and RL pins). The RW pin of each DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WR). Each DCP has its own WR. When the WR of a DCP contains all zeroes (WR<7:0>: 00h), its wiper terminal (RW) is closest to its “Low” terminal (RL). When the WR of a DCP contains all ones (WR<7:0>: FFh), its wiper terminal (RW) is closest to its “High” terminal (RH). As the value of the WR increases from all zeroes (00h) to all ones (255 decimal), the wiper moves monotonically from the position closest to RL to the closest to RH. At the same time, the resistance between RW and RL increases monotonically, while the resistance between RH and RW decreases monotonically.

While the X95820 is being powered up, all two WRs are reset to 80h (128 decimal), which locates RW roughly at the center between RL and RH. Soon after the power supply voltage becomes large enough for reliable non-volatile memory reading, the X95820 reads the value stored on two different non-volatile Initial Value Registers (IVRs) and loads them into their corresponding WRs.

The WRs and IVRs can be read or written directly using the 2-wire serial interface as described in the following sections.

Memory Description

The X95820 contains eight non-volatile bytes. they are accessed by 2-wire interface operations with Address Bytes 0 through 7 decimal. The first two non-volatile bytes at addresses 0 and 1 contain the initial value loaded at power-up into the volatile Wiper Registers (WRs) of DCP0 and DCP1 respectively. Bytes at addresses 2, 3, 4, 5, and 6 are available to the user as general purpose registers. The byte at address 7 is reserved; the user should not write to it, and its value should be ignored if read.

The volatile WR, and the non-volatile Initial Value Register (IVR) of a DCP are accessed with the same Address Byte.

A volatile byte at address 8 decimal, controls what byte is read or written when accessing DCP registers: the WR, the IVR, or both.

When the byte at address 8 is all zeroes, which is the default at power up:

– A read operation to addresses 0 or 1 outputs the value of the non-volatile IVRs.

– A write operation to addresses 0 or 1 writes the same value to the WR and IVR of the corresponding DCP.

When the byte at address 8 is 80h (128 decimal):

– A read operation to addresses 0 or 1 outputs the value of the volatile WR.

– A write operation to addresses 0 or 1only writes to the corresponding volatile WR.

It is not possible to write to an IVR without writing the same value to its corresponding WR.

00h and 80h are the only values that should be written to address 8. All other values are reserved and must not be written to address 8.

To access the general purpose bytes at addresses 2, 3, 4, 5, or 6, the value at address 8 must be all zeros.

The X95820 is pre-programed with 80h in the two IVRs.

Table 1. Memory Map

Address	Non-Volatile	Volatile
8	—	Access Control
7	Reserved	
6 5 4 3 2	General Purpose	Not Available
1 0	IVR1 IVR0	WR1 WR0

WR: Wiper Register, IVR: Initial value Register.

2-WIRE SERIAL INTERFACE

The X95820 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the X95820 operates as a slave device in all applications.

All communication over the 2-wire interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions. See Figure 1. On power up of the X95820 the SDA pin is in the input mode.

All 2-wire interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The X95820 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met. See Figure 1. A START condition is ignored during the power up sequence and during internal non-volatile write cycles.

All 2-wire interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH. See Figure 1. A STOP condition at the end of a read operation, or at the end of a write operation to volatile bytes only places the device in its standby mode. A STOP condition during a write operation to a non-volatile byte, initiates an internal non-volatile write cycle. The device enters its standby state when the internal non-volatile write cycle is completed.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data. See Figure 2.

The X95820 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The X95820 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 1010 as the four MSBs, and the following three bits matching the logic values present at pins A2, A1, and A0. The LSB in the Read/$\overline{\text{Write}}$ bit. Its value is “1” for a Read operation, and “0” for a Write operation. See Table 2.

Table 2. Identification Byte Format

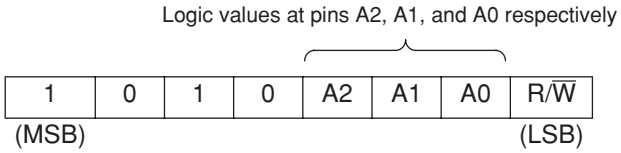


Figure 1. Valid Data Changes, Start, and Stop Conditions

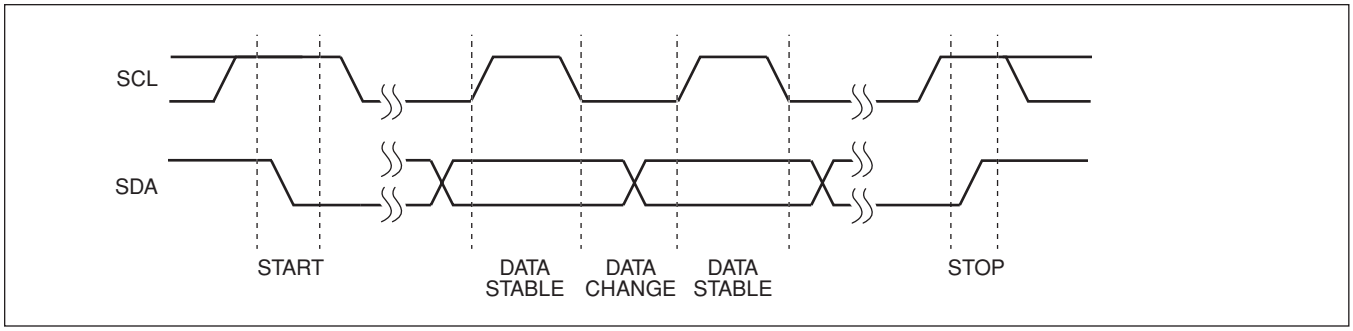


Figure 2. Acknowledge Response from Receiver

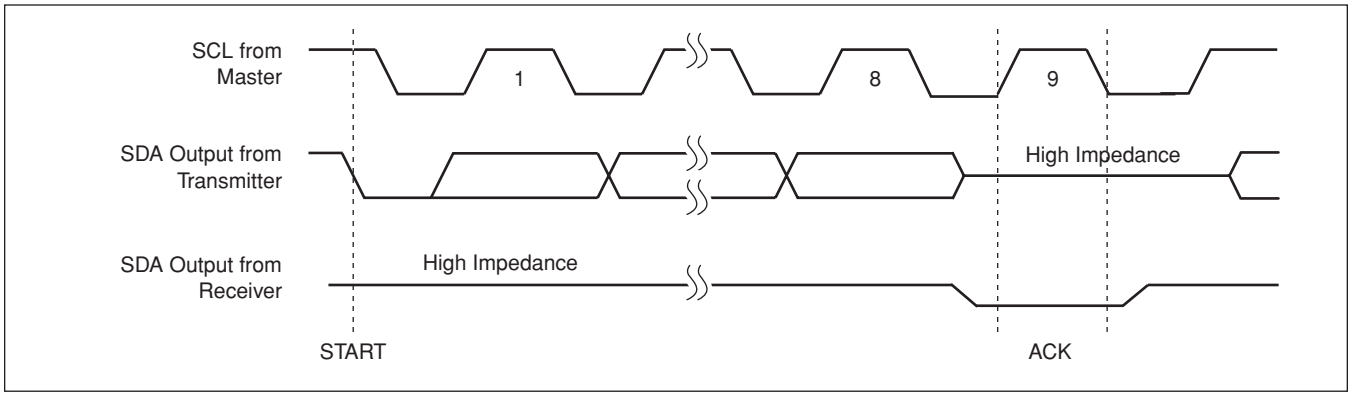
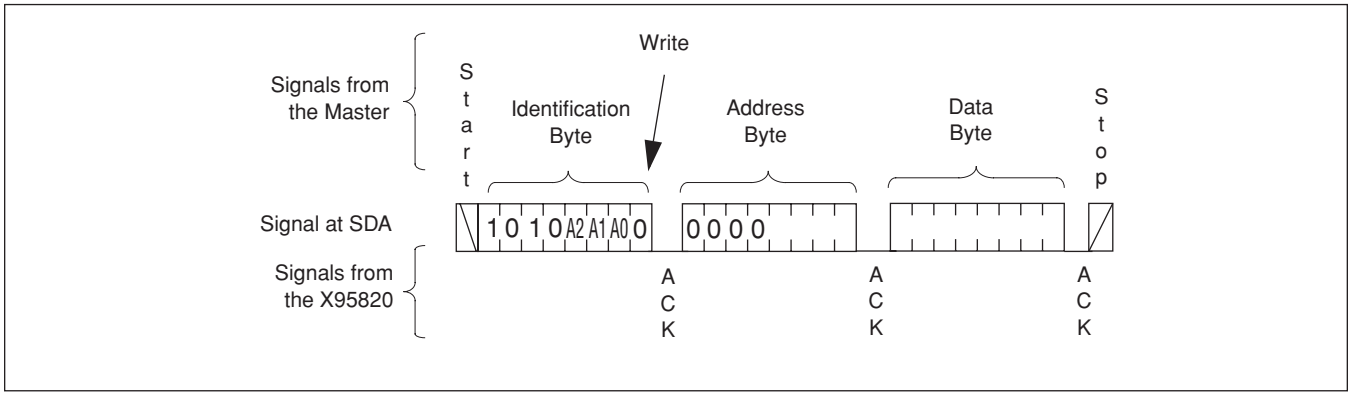


Figure 3. Byte Write Sequence



WRITE OPERATION

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the X95820 responds with an ACK. At this time, if the Data Byte is to be written only to volatile registers, then the device enters its standby state. If the Data Byte is to be written also to non-volatile memory, the X95820 begins its internal write cycle to non-volatile memory. During the internal non-volatile write cycle, the device ignores transitions at the SDA and SCL pins, and the SDA output is at a high impedance state. When the internal non-volatile write cycle is completed, the X95820 enters its standby state. See Figure 3.

The byte at address 00001000 bin (8 decimal) determines if the Data Byte is to be written to volatile and/or non-volatile memory. See “Memory Description” on page 3.

DATA PROTECTION

The $\overline{WP}$ pin has to be at logic HIGH to perform any Write operation to the device. When the $\overline{WP}$ is active (LOW) the device ignores Data Bytes of a Write Operation, does not respond to the Data Bytes with an ACK, and instead, goes to its standby state waiting for a new START condition.

A STOP condition also acts as a protection of non-volatile memory. A valid Identification Byte, Address Byte, and total number of SCL pulses act as a protection of both volatile and non-volatile registers. During a Write sequence, the Data Byte is loaded into an internal shift register as it is received. If the Address Byte is 0, 1, or 8 decimal, the Data Byte is transferred to the appropriate Wiper Register (WR) or to the Access Control Register, at the falling edge of the SCL pulse that loads the last bit (LSB) of the Data Byte. If the Address Byte is between 0 and 6 (inclusive), and the Access Control Register is all zeros (default), then the STOP condition initiates the internal write cycle to non-volatile memory.

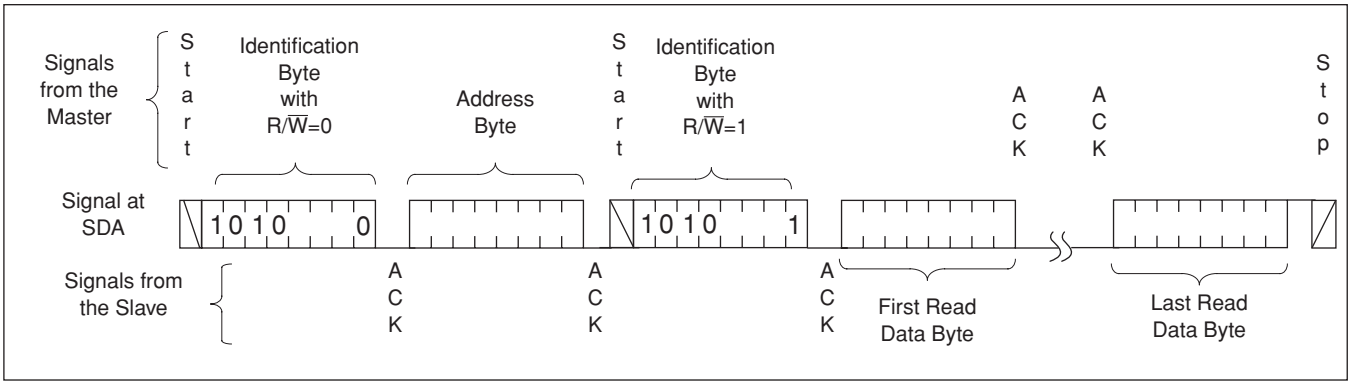
READ OPERATION:

A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 4). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the X95820 responds with an ACK. Then the X95820 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eigth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte. See Figure 4.

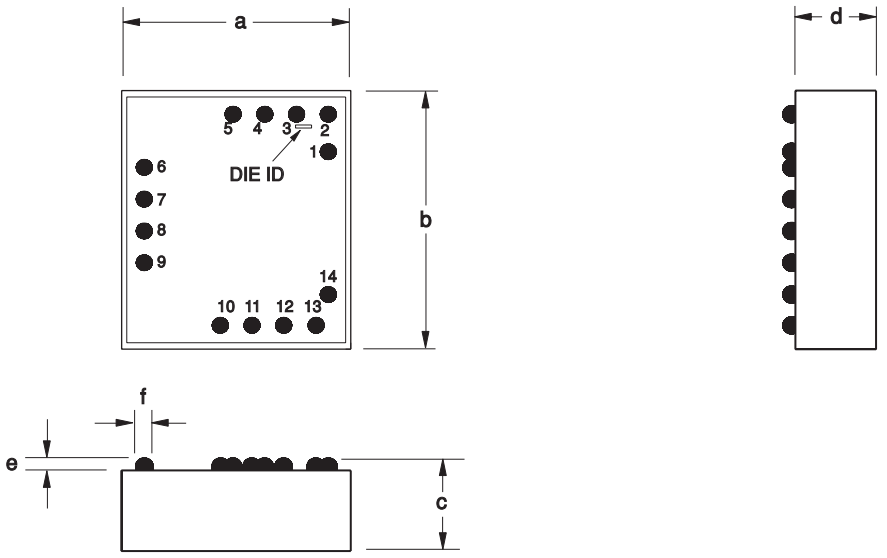
The Data Bytes are from the memory location indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 01Fh (8 decimal) the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.

The byte at address 00001000 bin (8 decimal) determines if the Data Bytes being read are from volatile or non-volatile memory. See “Memory Description” on page 3.

Figure 4. Read Sequence



FCP PACKAGING INFORMATION

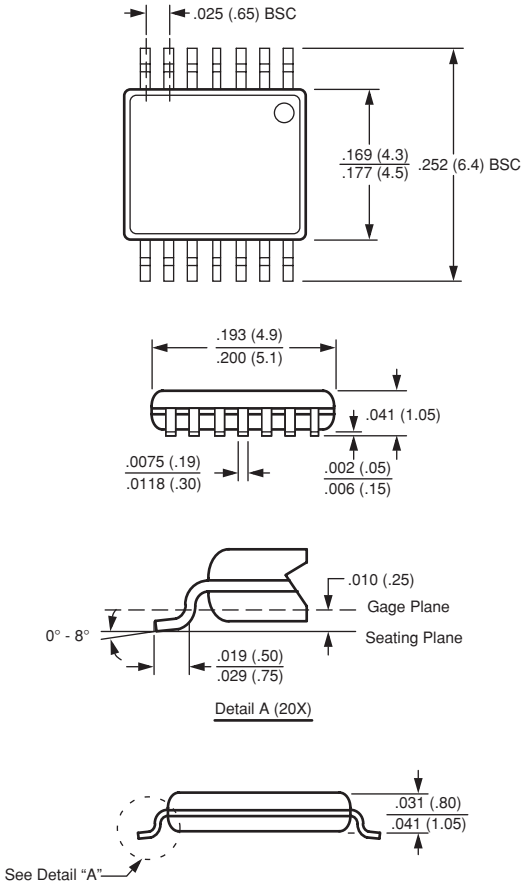


	Symbol	Min.	Nominal	Max
		Millimeters		
Package Width	a	1.760	1.790	1.810
Package Length	b	1.990	2.020	2.050
Package Height	c	0.785	0.825	0.865
Body Thickness	d	0.700	0.725	0.750
Ball Height	e	0.085	0.100	0.115
Ball Diameter	f	0.110	0.125	0.140

	Bump Name	X Coordinate, µm	Y Coordinate, µm
1	Vcc	725.0	535.2
2	$\overline{WP}$	725.0	830.0
3	RH0	475.0	830.0
4	RL0	225.0	830.0
5	RW0	-25.0	830.0
6	A2	-725.0	412.6
7	SCL	-725.0	162.6
8	SDA	-725.0	-88.2
9	vbb!	-725.0	-337.4
10	RW1	-126.2	-830.0
11	RL1	123.8	-830.0
12	RH1	373.8	-830.0
13	A0	629.1	-830.0
14	A1	725.0	-587.6

TSSOP PACKAGING INFORMATION

14-Lead Plastic, TSSOP, Package Code V14



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)