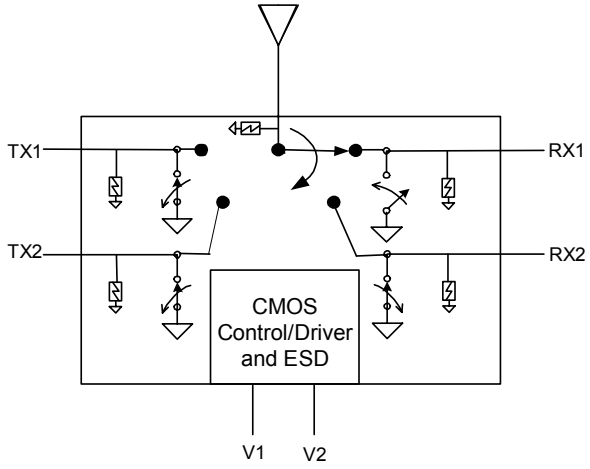
Product Brief

PE42612 Flip Chip

SP4T UltraCMOS™ 2.6 V Switch 100 – 3000 MHz

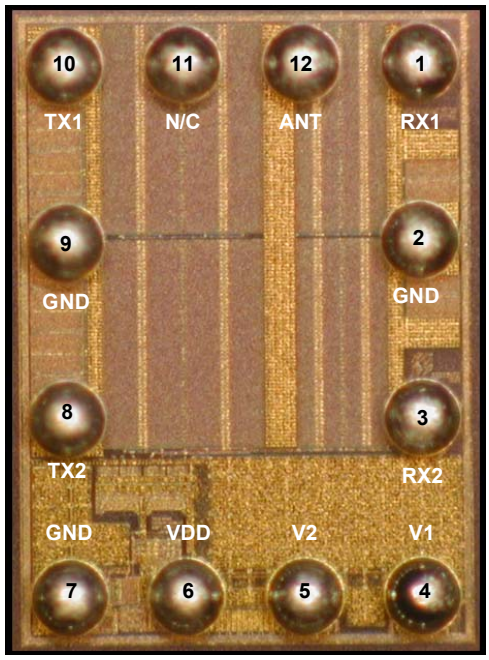
Figure 1. Functional Diagram



Features

- Two pin CMOS logic control inputs
- Supports 1.8 V Control Logic
- Low TX insertion loss: 0.55 dB at 900 MHz, 0.70 dB at 1900 MHz
- Isolation of 39 dB at 900 MHz, 31 dB at 1900 MHz
- Low harmonics $2f_o$ = -82 dBc and $3f_o$ = -74 dBc at 35 dBm input power
- 1500 V HBM ESD tolerance
- Built in CMOS decoder/driver
- RX SAW over voltage protection circuit
- No blocking capacitors required

Figure 2. Die Top View



Product Description

The PE42612 SP4T RF UltraCMOS™ Flip Chip Switch is designed specifically to address the needs of the antenna switch module market for GSM Handsets. On-chip CMOS decode logic is used to facilitate two-pin, low voltage CMOS control inputs. High ESD tolerance of 1500 V at all ports, no blocking capacitor requirements and on-chip SAW filter over-voltage protection devices make this the ultimate in integration and ease of use.

The PE42612 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Table 1. PE42612 Electrical Specifications: Temp = 25°C, V_{DD} = 2.6 V

Parameter	Condition	Min	Typ	Max	Unit
Operational Frequency		100		3000	MHz
Insertion Loss	ANT - TX - 850 / 900 MHz ANT - TX - 1800 / 1900 MHz ANT - RX - 850 / 900 MHz ANT - RX - 1800 / 1900 MHz		0.55 0.7 0.85 1.05	0.65 0.8 1.0 1.2	dB dB dB dB
Isolation	TX - RX - 850 / 900 MHz (TX ON) TX - RX - 1800 / 1900 MHz (TX ON) TX1 - TX2 - 850 / 900 MHz (TX1 ON) TX1 - TX2 - 1800 / 1900 MHz (TX1 ON)	37 29 33 26	39 31 35 28		dB dB dB dB
Return Loss	850 / 900 MHz 1800 / 1900 MHz	18 14	20 16		dB dB
2nd Harmonic[1,2]	35 dBm TX Input Power - 850 / 900 MHz 33 dBm TX Input Power - 1800 / 1900 MHz		-82 -89	-78 -82	dBc dBc
3rd Harmonic[1,2]	35 dBm TX Input Power - 850 / 900 MHz 33 dBm TX Input Power - 1800 / 1900 MHz		-74 -68	-69 -65	dBc dBc
Switching time	(10-90%) (90-10%) RF		2	3	µs

Notes: 1. Measured in Pulsed Wave Mode.
2. Assumes RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005

Table 2. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Units
Temperature range	T_{OP}	-40		+85	°C
V_{DD} Supply Voltage	V_{DD}	2.4	2.6	2.95	V
I_{DD} Power Supply Current (V_{DD} = 2.6 V)	I_{DD}		11	25	µA
TX input power (VSWR ≤ 3:1) 824-915 MHz	P_{IN}			+35	dBm
TX input power (VSWR ≤ 3:1) 1710-1910 MHz				+33	
RX input power (VSWR ≤1:1)	P_{IN}			+20	dBm
Control Voltage High	V_{IH}	1.40			V
Control Voltage Low	V_{IL}			0.40	V
Control Line Current				1	µA

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any DC input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	+150	°C
T_{OP}	Operating temperature range	-40	+85	°C
P_{IN}	TX input power (50 Ω)[3,4] 824-915 MHz		+38	dBm
	TX input power (50 Ω)[3,4] 1710-1910 MHz		+36	
	RX input power (50 Ω)		+23	
P_{IN} (∞:1)	TX input power (VSWR = (∞:1)[3,4] 824-915 MHz		+35	dBm
	TX input power (VSWR = (∞:1)[3,4] 1710-1910 MHz		+33	
V_{ESD}	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		1500	V
	ESD Voltage (MM, JEDEC, JESD22-A114-B)		100	V

Note: 3. Assumes RF input duty cycle of 50% and 4620 µs.
4. V_{DD} within operating range specified in Table 4.

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Functional operation should be restricted to the limits in the DC Electrical Specifications table. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Figure 3. Pin Configuration (Ball-Side Up)

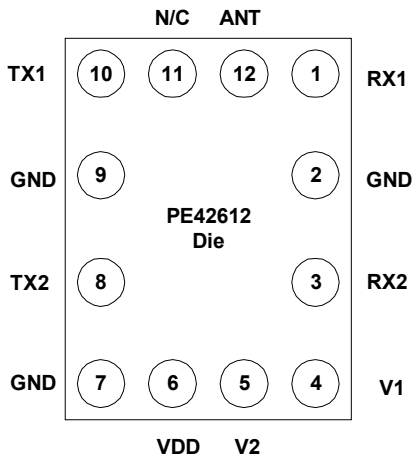


Table 4. Pin Descriptions

Pin No.	Pin Name	Description
1[5]	RX1	RF I/O – RX1
2	GND	Ground
3[5]	RX2	RF I/O – RX2
4	V1	Switch control input, CMOS logic level
5	V2	Switch control input, CMOS logic level
6	VDD	Supply
7	GND	Ground
8[5]	TX2	RF I/O - TX2
9	GND	Ground
10[5]	TX1	RF I/O - TX1
11	N/C	No Connect – Pin to be connected to an electrically isolated low capacitance pad
12[5]	ANT	RF Common – Antenna Input

Note: 5. Blocking capacitors needed only when non-zero DC voltage present.

Table 5. Truth Table

Path	V2	V1
ANT - RX1	0	0
ANT - RX2	0	1
ANT - TX1	1	0
ANT - TX2	1	1

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 6. Ordering Information

Order Code	Die ID	Description	Package	Shipping Method
PE42612-90 (Unitive)	C9817_1	PE42612-DIE-D	Film Frame	Wafer (Gross Die / Wafer Quantity)
PE42612-91 (FCI)	C9817_1	PE42612-DIE-D	Film Frame	Wafer (Gross Die / Wafer Quantity)
PE42612-00	C9817_1	PE42612-DIE-1H	Evaluation Kit	1 / Box

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Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

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