Designer's™ Data Sheet

Fully Isolated TMOS E-FET ™ Power Field Effect Transistor

N–Channel Enhancement–Mode Silicon Gate Isolated TO–220

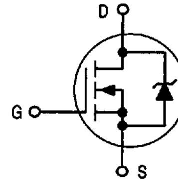
MTA1N60E

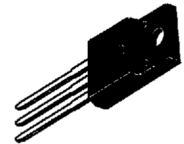
Motorola Preferred Device

**TMOS POWER FET
1.0 AMPERE
600 VOLTS
$R_{DS(on)}$ = 8.0 OHM**

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Version of the MTP2N60E





CASE 221D–02, Style 1
(ISOLATED TO–220 TYPE)

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MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	600	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le$ 10 ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le$ 10 µs)	I_D I_D I_{DM}	1.0 0.8 3.0	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 3.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	45	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.13 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	600 —	— 720	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 600 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 600 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.2 6.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)		$R_{DS(on)}$	—	5.9	8.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 1.0 Adc) (I_D = 0.5 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	— —	9.6 8.4	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 0.5 Adc)		g_{FS}	0.5	0.8	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	224	310	pF
Output Capacitance		C_{oss}	—	27	40	
Reverse Transfer Capacitance		C_{rss}	—	6.0	10	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 300 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8.8	20	ns
Rise Time		t_r	—	6.8	14	
Turn–Off Delay Time		$t_{d(off)}$	—	15	30	
Fall Time		t_f	—	20	40	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	7.1	11	nC
		Q_1	—	1.7	—	
		Q_2	—	3.2	—	
		Q_3	—	3.9	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 1.0 Adc, V_{GS} = 0 Vdc) (I_S = 1.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.82 0.7	1.4 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 1.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	464	—	ns
		t_a	—	36	—	
		t_b	—	428	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.629	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_D	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

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TYPICAL ELECTRICAL CHARACTERISTICS

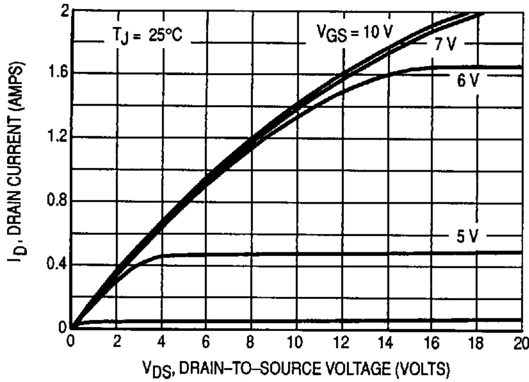

Figure 1. On–Region Characteristics

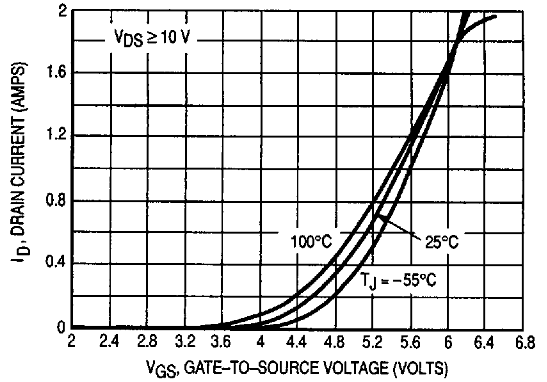

Figure 2. Transfer Characteristics

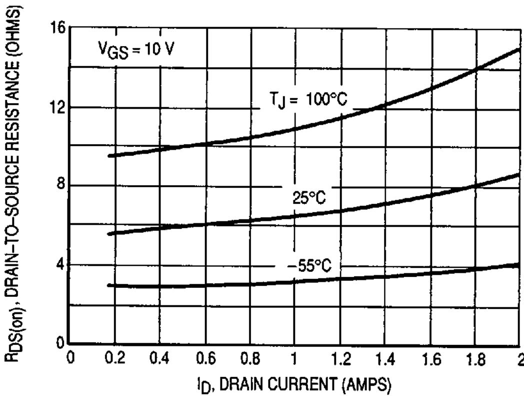

Figure 3. On–Resistance versus Drain Current and Temperature

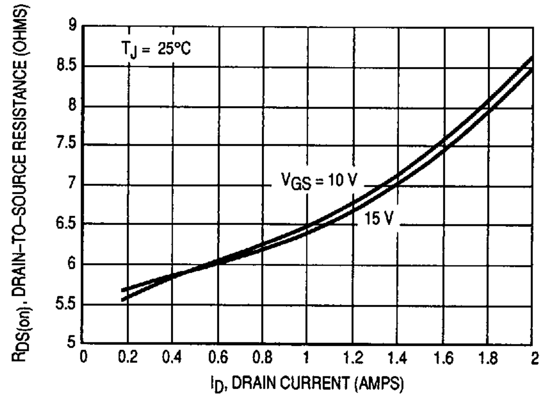

Figure 4. On–Resistance versus Drain Current and Gate Voltage

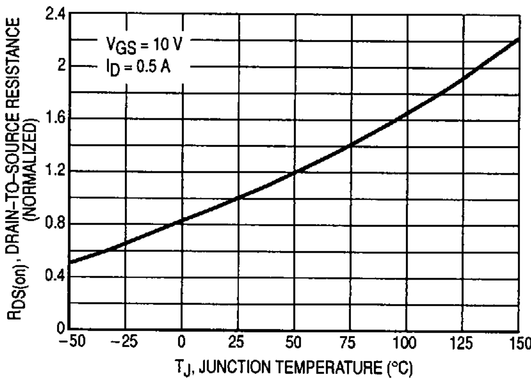

Figure 5. On–Resistance Variation with Temperature

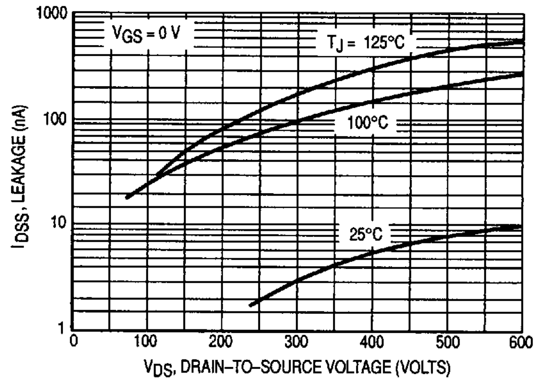

Figure 6. Drain–To–Source Leakage Current versus Voltage

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POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \ln\ [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G\ C_{iss}\ \ln\ (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

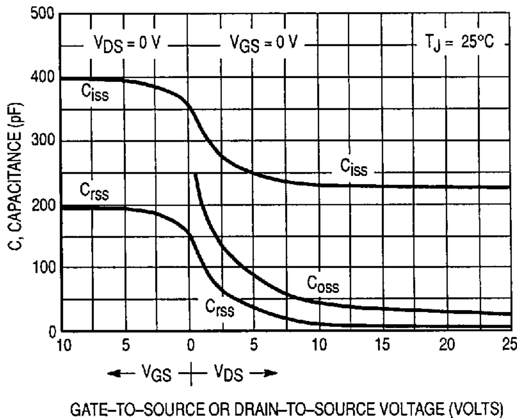

Figure 7a. Capacitance Variation

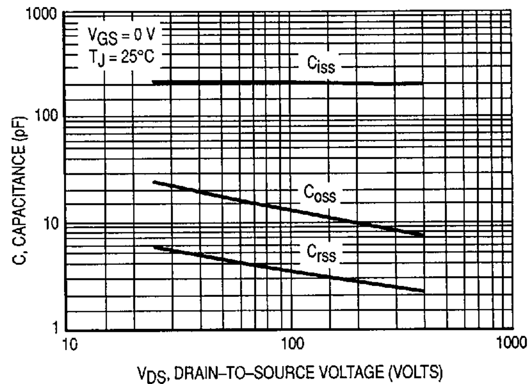

Figure 7b. High Voltage Capacitance Variation

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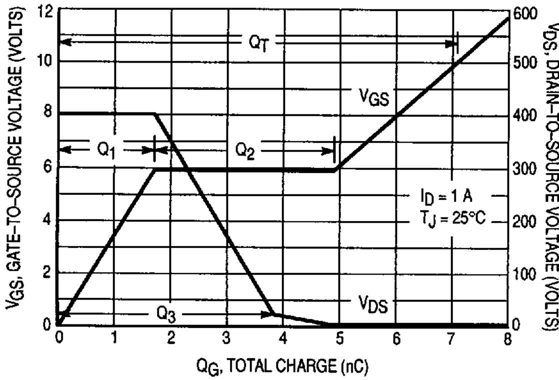

Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

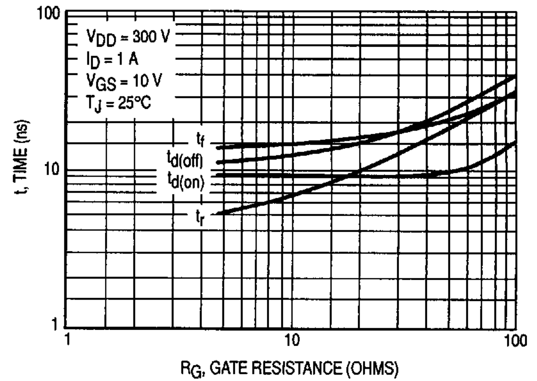

Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

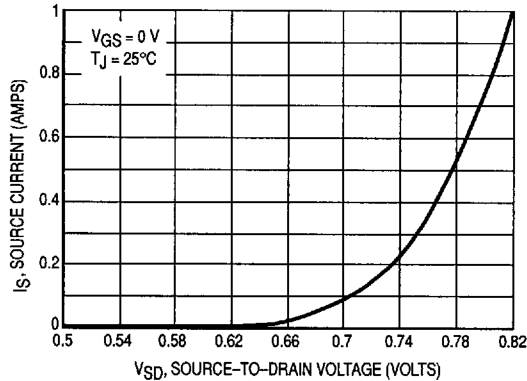

Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

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SAFE OPERATING AREA

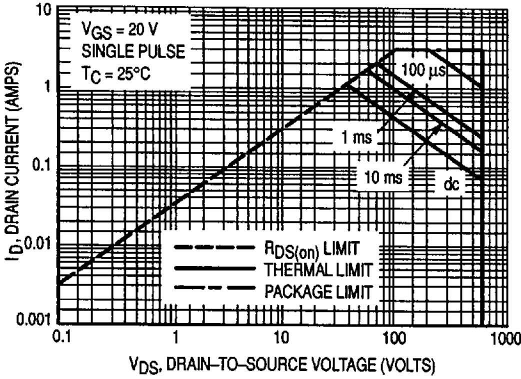

Figure 11. Maximum Rated Forward Biased Safe Operating Area

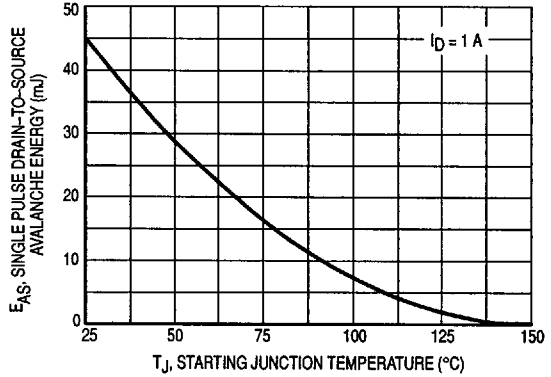

Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

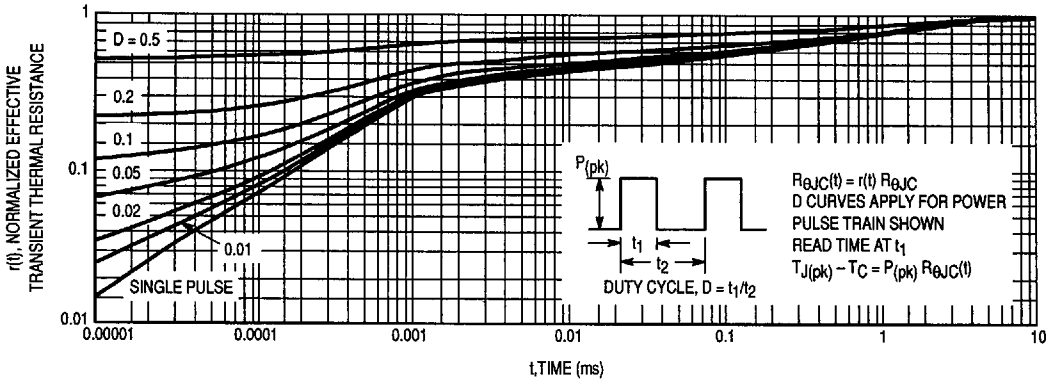

Figure 13. Thermal Response

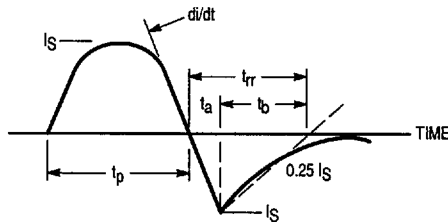

Figure 14. Diode Reverse Recovery Waveform

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Designer's™ Data Sheet

Fully Isolated TMOS E-FET™ High Energy Power FET

N–Channel Enhancement–Mode Silicon Gate

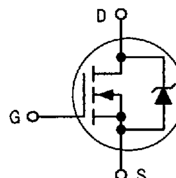
MTA2N60E

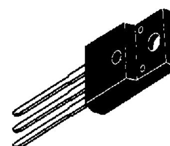
Motorola Preferred Device

TMOS POWER FET
2.0 AMPERES
600 VOLTS
$R_{DS(on)}$ = 2.2 OHMS MAX

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and commutation modes. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Designed to Eliminate the Need for External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Version of the MTP3N60E





CASE 221D–02, Style 1
(ISOLATED TO–220 TYPE)

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	600	Volts
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Volts
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 50$ µs)	V_{GS} V_{GSM}	±20 ±40	Volts
Drain Current — Continuous — Single Pulse ($t_p \le 10$ µs)	I_D I_{DM}	2.0 9.0	Amps
RMS Isolation Voltage (t = 1 second, R.H. ≤ 30%, T_A = 25°C) Per Figure 19 Per Figure 20 Per Figure 21	V_{ISO1} V_{ISO2} V_{ISO3}	4500 3500 1500	Volts
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS ($T_J \le 150$°C)

Rating	Symbol	Value	Unit
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 75 V, V_{GS} = 10 V, L = 64 mH, R_G = 25 Ω, Peak I_L = 4.0 A) (See Figures 16, 17 and 18)	E_{AS}	290	mJ

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.7 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μAdc) Temperature Coefficient (positive)		$V_{(BR)DSS}$	600 —	— 480	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 600 V, V_{GS} = 0) (V_{DS} = 480 V, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	— —	0.25 1.0	mA
Gate–Body Leakage Current — Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Gate–Body Leakage Current — Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (negative)		$V_{GS(th)}$	2.0 —	2.8 8.5	4.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)		$R_{DS(on)}$	—	1.9	2.2	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 V) (I_D = 3.0 Adc) (I_D = 1.5 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	— —	7.0 7.5	Vdc
Forward Transconductance (V_{DS} ≥ 15 V, I_D = 1.5 A)		g_{FS}	1.5	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz) See Figures 14 and 15	C_{iss}	—	800	—	pF
Reverse Transfer Capacitance		C_{rss}	—	19	—	
Output Capacitance		C_{oss}	—	105	—	
SWITCHING CHARACTERISTICS (T_J = 100°C)						
Turn–On Delay Time	(V_{DS} = 300 V, I_D = 3.0 A, V_{GS} = 10 V, R_g = 12 Ω) See Figure 7	$t_{d(on)}$	—	16	—	ns
Rise Time		t_r	—	27	—	
Turn–Off Delay Time		$t_{d(off)}$	—	32	—	
Fall Time		t_f	—	25	—	
Gate Charge	(V_{DS} = 400 V, I_D = 3.0 A, V_{GS} = 10 Vdc) See Figures 5 and 6	Q_T	—	24	31	nC
		Q_1	—	4.0		
		Q_2	—	10	—	
		Q_3	—	8.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS*						
Forward On–Voltage	(I_S = 3.0 A, V_{GS} = 0)	V_{SD}	—	1.0	1.4	Vdc
	(I_S = 3.0 A, V_{GS} = 0, T_J = 125°C)		—	0.9	—	
Reverse Recovery Time	(I_S = 3.0 A, V_{GS} = 0, dI_S/dt = 100 A/μs)	t_{rr}	—	350	—	ns
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	
ISOLATION CAPACITANCE						
Isolation Capacitance, Drain–to–Heatsink		C_{iso}	—	15	—	pF

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

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TYPICAL ELECTRICAL CHARACTERISTICS

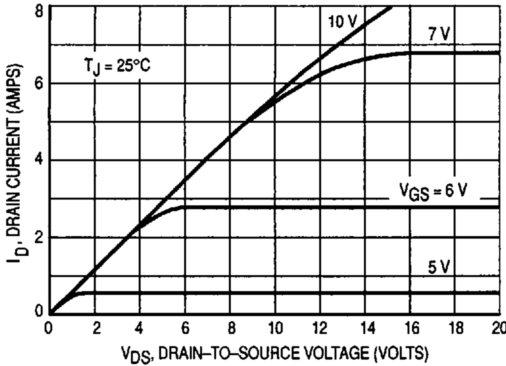

Figure 1. On–Region Characteristics

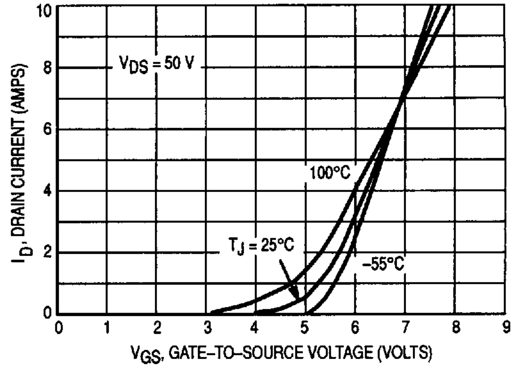

Figure 2. Transfer Characteristics

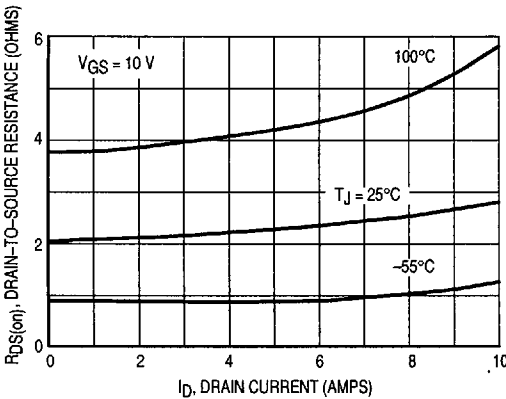

Figure 3. On–Resistance versus Drain Current

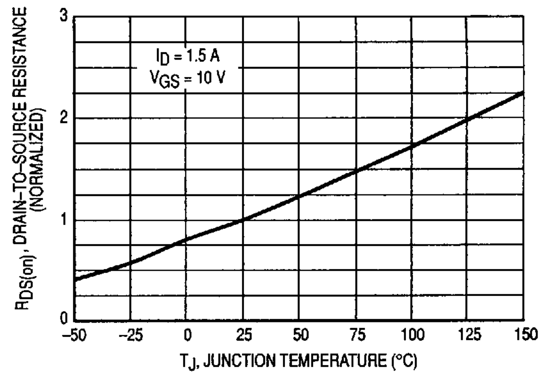

Figure 4. On–Resistance Variation With Temperature

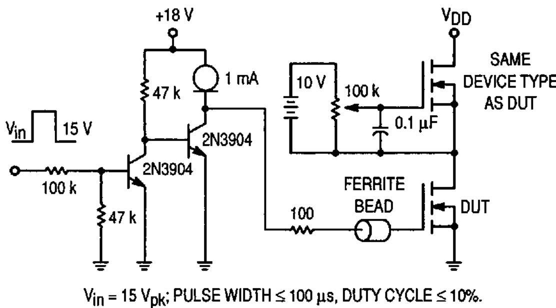

Figure 5. Gate Charge Test Circuit

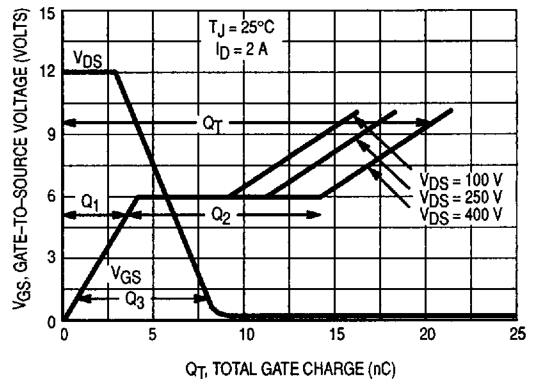

Figure 6. Gate Charge versus Gate–to–Source Voltage

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SAFE OPERATING AREA INFORMATION

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance–General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, BV_{DSS}. The switching SOA shown in Figure 9 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

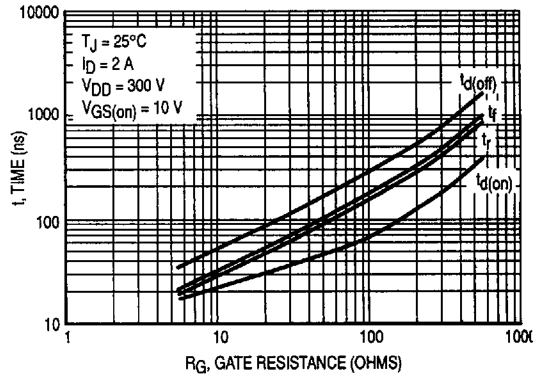

Figure 7. Resistive Switching Time Variation versus Gate Resistance

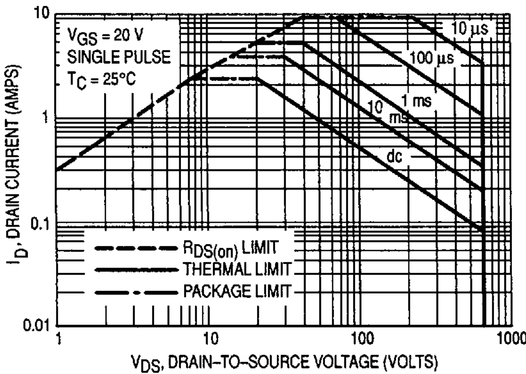

Figure 8. Maximum Rated Forward Biased Safe Operating Area

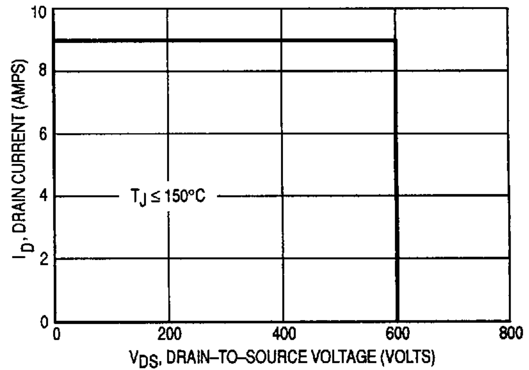

Figure 9. Maximum Rated Switching Safe Operating Area

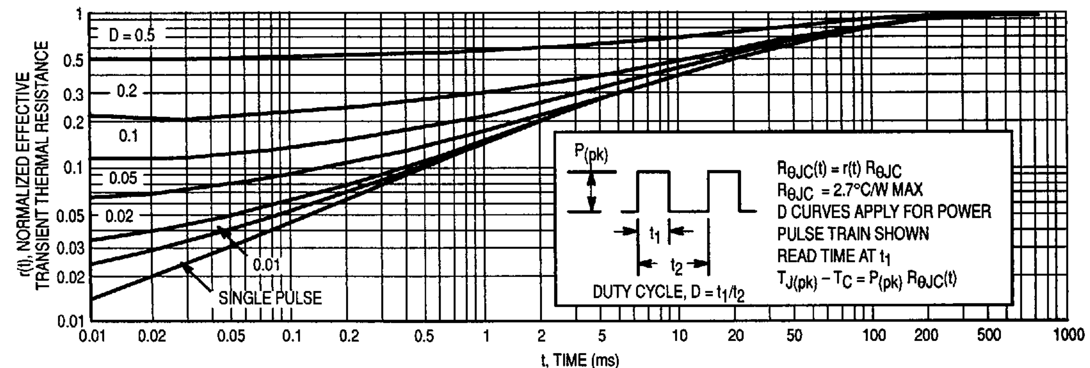

Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source–drain current versus re–applied drain voltage when the source–drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half–bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source–drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/µs.

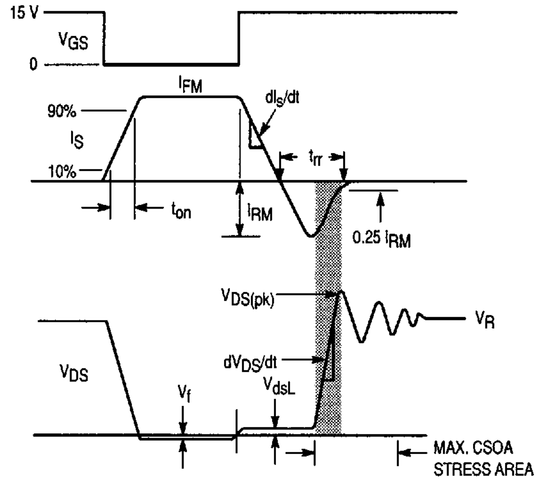

Figure 11. Commutating Waveforms

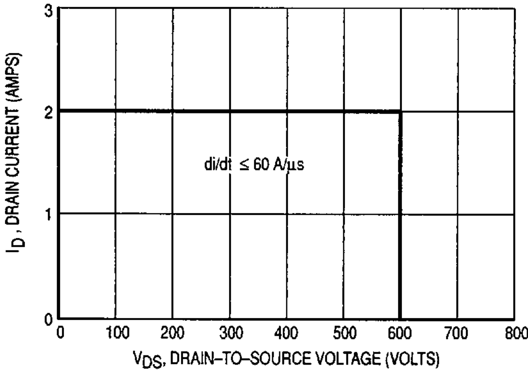

Figure 12. Commutating Safe Operating Area (CSOA)

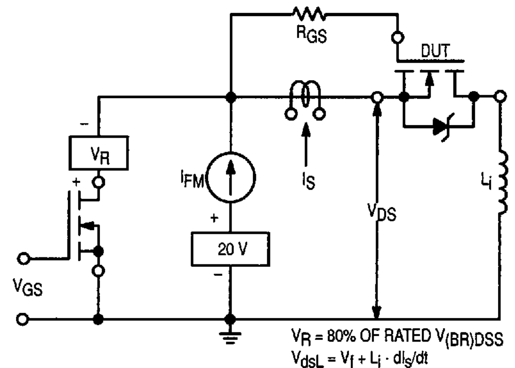

Figure 13. Commutating Safe Operating Area Test Circuit

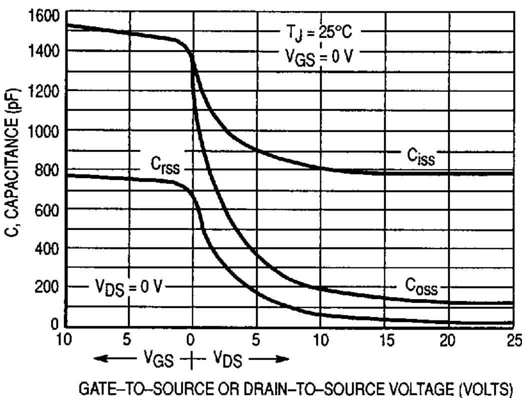

Figure 14. Low Voltage Capacitance Variation

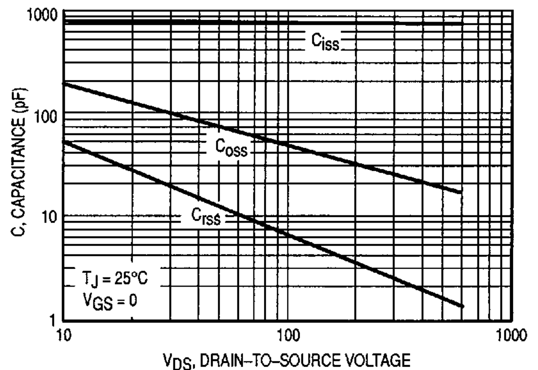

Figure 15. High Voltage Capacitance Variation

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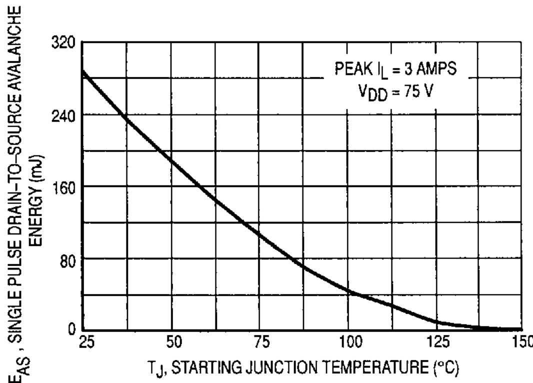

Figure 16. Maximum Avalanche Energy versus Starting Junction Temperature

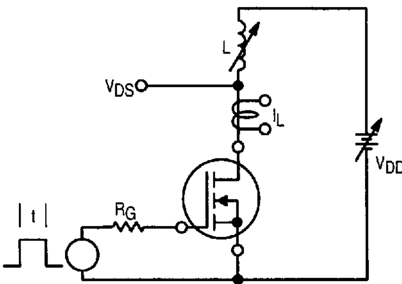

Figure 17. Unclamped Inductive Switching Test Circuit

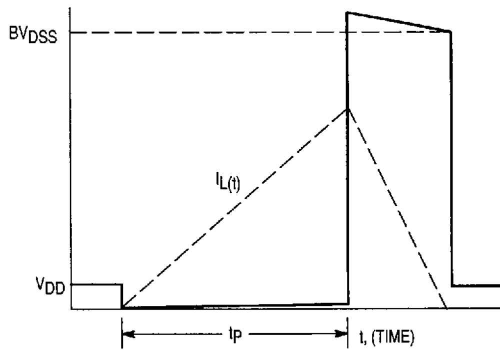

Figure 18. Unclamped Inductive Switching Waveforms

TEST CONDITIONS FOR ISOLATION TESTS*

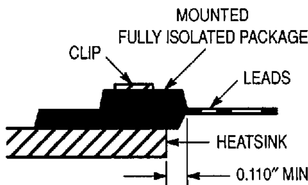

Figure 19. Clip Mounting Position for Isolation Test Number 1

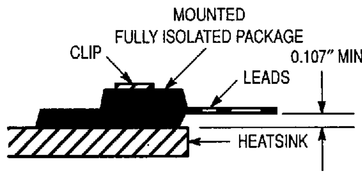

Figure 20. Clip Mounting Position for Isolation Test Number 2

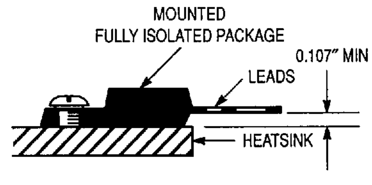

Figure 21. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together.

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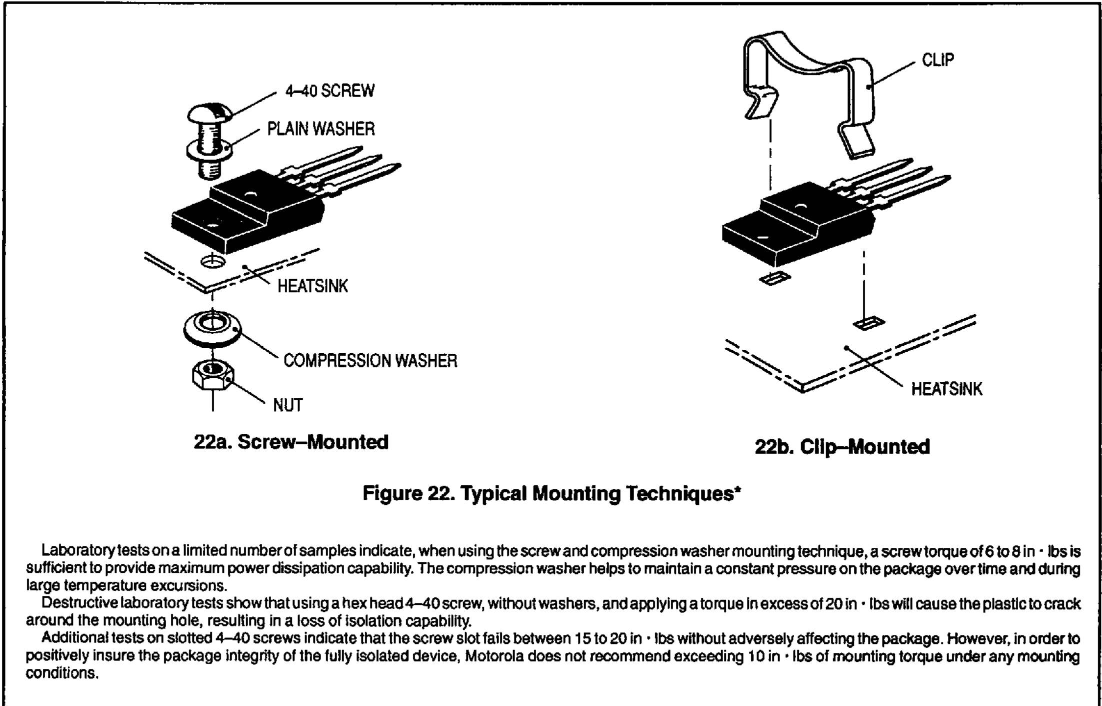
MOUNTING INFORMATION**



22a. Screw–Mounted

22b. Clip–Mounted

Figure 22. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively insure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

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