



DOCUMENT NUMBER AND REVISION  
**VL-FS-MDLS16119D-01 REV. A**  
**(MDLS16119D-LV-DIE IC)**

DOCUMENT TITLE:  
**SPECIFICATION**  
**OF**  
**LCD MODULE TYPE**

CUSTOMER	
MODEL NUMBER	<b>MDLS16119D-01</b>
CUSTOMER APPROVAL	
DATE	

DEPARTMENT	NAME	SIGNATURE	DATE
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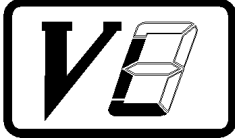
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A	2002.10.11	Based on the Test Specification: VL-TS-MDLS16119D-XX REV. B, 2002.02.01)	PHILIP CHENG	TOM LEE



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### Specification of LCD Module Type Item No.: MDLS16119D-01

#### 1. General Description

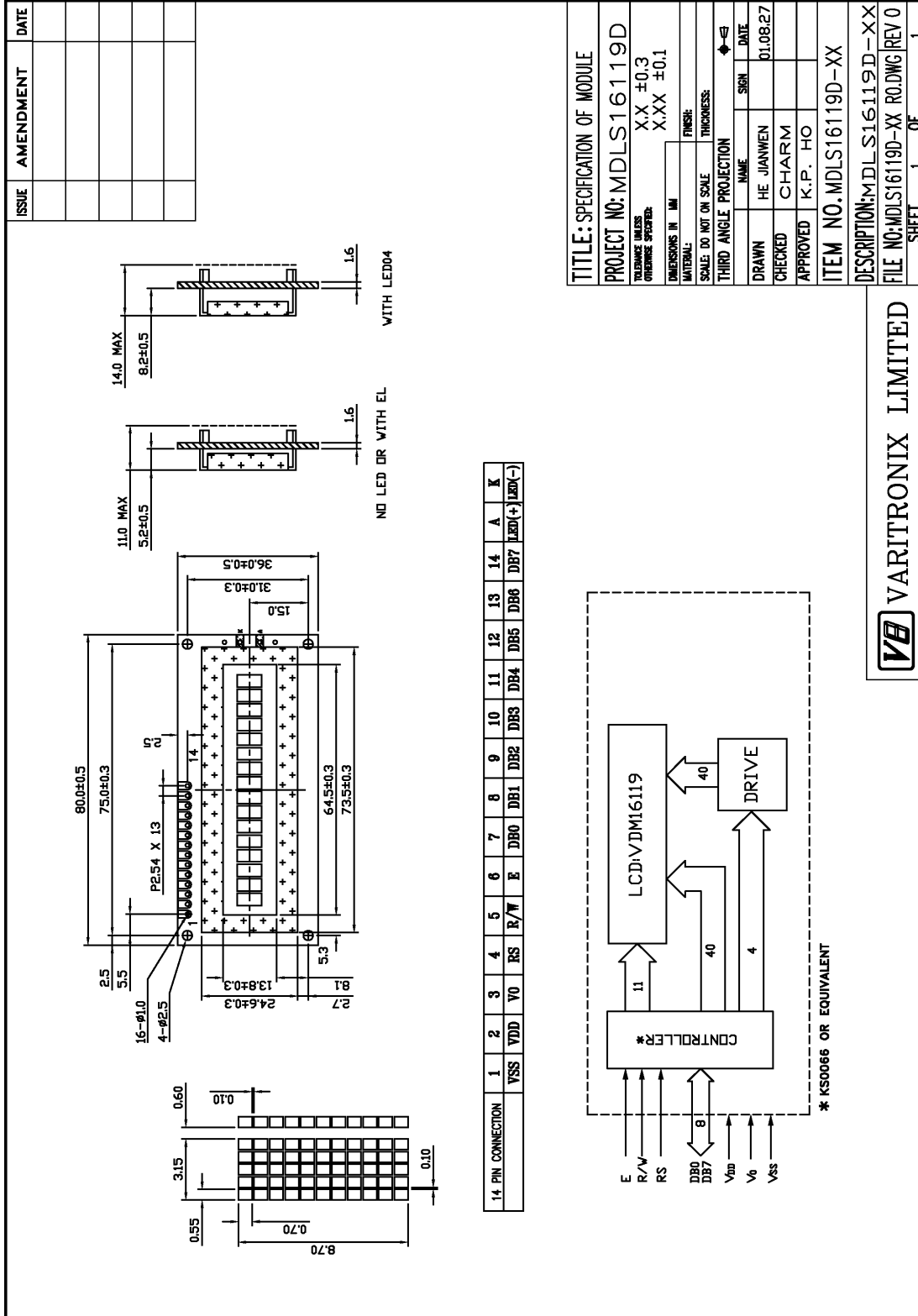
- 16 characters (5 x 11 dots) x 1 line STN Positive Yellow Reflective LCD Character Module.
- Viewing Angle: 6 o'clock direction.
- Driving duty: 1/16 duty, 1/4 bias.
- 'NOVATEK' NT3881DH-01/AI (die form) LCD Controller and Driver or equivalent.
- 'SAMSUNG' KS0065B-PCC (die form) LCD Segment Driver or equivalent.

#### 2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	80.0(W) x 36.0(H) x 11.0 MAX.(D)	mm
Effective viewing area	64.5(W) x 13.8(H)	mm
Display format	16 characters x 1 line	-
Character size	3.15(W) x 8.70(H) (5 x 11 dots)	mm
Character spacing	0.60(W)	mm
Character pitch	3.75(W)	mm
Dot size	0.55(W) x 0.70(H)	mm
Dot spacing	0.10(W) x 0.10(H)	mm
Dot pitch	0.65(W) x 0.80(H)	mm
Weight	TBD	grams



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Figure 1: Outline Drawing



### 3. Absolute Maximum Ratings

#### 3.1 Electrical Maximum Ratings(Ta = 25 °C)

Table 2

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD - VSS	-0.3	+7.0	V
Power Supply voltage (LCD drive)	VLCD =VDD - V0	-0.3	+13.5	V
Input voltage	V <sub>in</sub>	-0.3	VDD+0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

#### 3.2 Environmental Condition

Table 3

Item	Operating Temperature (T <sub>opr</sub> )		Storage Temperature (T <sub>stg</sub> )		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s <sup>2</sup> = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions



#### 4. Electrical Specifications

##### 4.1 Interface signals

Table 4

Pin No.	Symbol	Description
1	VSS	Ground
2	VDD	Power supply for logic.
3	V0	Power supply for LCD driver.
4	RS	Register Select Input : "High" for Data register (for read and write). "Low" for Instruction register (for write), Busy flag, address counter (for read).
5	R/W	Read/Write signal: 'High' for Read mode. 'Low' for Write mode.
6	E	Enable. Start signal for data read /write.
7	DB0	Data input/output (LSB)
8	DB1	Data input/output
9	DB2	Data input/output
10	DB3	Data input/output
11	DB4	Data input/output
12	DB5	Data input/output
13	DB6	Data input/output
14	DB7	Data input/output (MSB)
A	LED(+)	Anode of backlight (OPTIONAL).
K	LED(-)	Cathode of backlight (OPTIONAL).



## 4.2 Typical Electrical Characteristics

At  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = 5V \pm 5\%$ ,  $V_{SS} = 0V$ .

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	$V_{DD} - V_{SS}$		4.75	5.0	5.25	V
Supply voltage (LCD)	$V_{DD} - V_0$	$V_{DD} = 5V$ , Note 1.	4.2	4.4	4.6	V
Input signal voltage 1 for E,DB0-DB7,R/W,RS.	$V_{IH1}$	"H" level	2.2	-	$V_{DD}$	V
	$V_{IL1}$	"L" level	-0.3	-	0.8	V
Input signal voltage 2 for OSC1.	$V_{IH2}$	"H" level	$V_{DD} - 1.0$	-	$V_{DD}$	V
	$V_{IL2}$	"L" level	$V_{SS}$	-	1.0	V
Supply Current (Logic & LCD)	IDD	Character mode, Note 1	-	0.8	1.2	mA
		Checker board mode, Note 1	-	1.4	2.1	mA
Supply Current (LCD)	I0	Character mode, Note 1	-	0.5	0.7	mA
		Checker board mode, Note 1	-	0.5	0.7	mA

Note (1) : There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.





### 4.3 Timing Specifications

At  $T_a = 0\text{ }^{\circ}\text{C}$  to  $+50\text{ }^{\circ}\text{C}$  ,  $V_{DD} = 5V \pm 5\%$  ,  $V_{SS} = 0V$ .

Refer to Fig. 2 , the bus timing diagram for write mode.

Table 6

Parameter	Symbol	Min.	Max.	Unit	Remarks
Enable cycle time	$t_{CYCE}$	500	-	ns	
Enable "High" level pulse width	$t_{WHE}$	300	-	ns	
Enable rise time	$t_{RE}$	-	25	ns	
Enable fall time	$t_{FE}$	-	25	ns	
RS, R/W set-up time	$t_{AS}$	60	-	ns	8-bit operation mode
		100			4-bit operation mode
RS, R/W address hold time	$t_{AH}$	10	-	ns	
Data output delay	$t_{DS}$	100	-	ns	
Data hold time	$t_{DHR}$	10	-	ns	

Refer to Fig. 3 , the bus timing diagram for read mode .

Table 7

Parameter	Symbol	Min.	Max.	Unit	Remarks
Enable cycle time	$t_{CYCE}$	500	-	ns	
Enable "High" level pulse width	$t_{WHE}$	300	-	ns	
Enable rise time	$t_{RE}$	-	25	ns	
Enable fall time	$t_{FE}$	-	25	ns	
RS, R/W set-up time	$t_{AS}$	60	-	ns	8-bit operation mode
		100			4-bit operation mode
RS, R/W address hold time	$t_{AH}$	10	-	ns	
Read data output delay	$t_{RD}$	-	190	ns	
Read data hold time	$t_{DHR}$	20	-	ns	

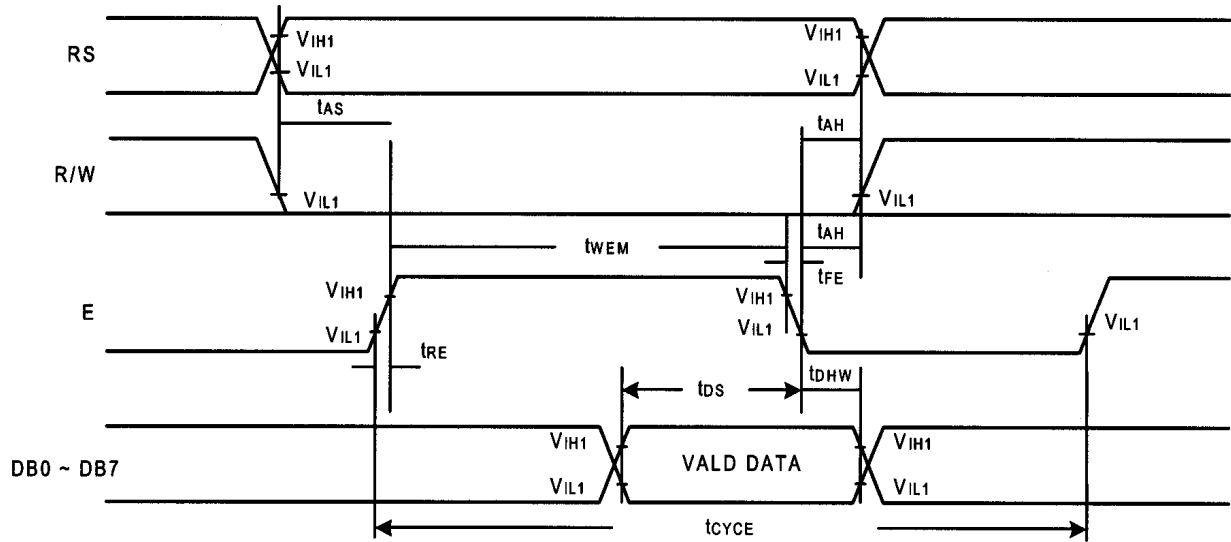


Figure 2: Bus write operation sequence (Writing data from MPU to NT3881).

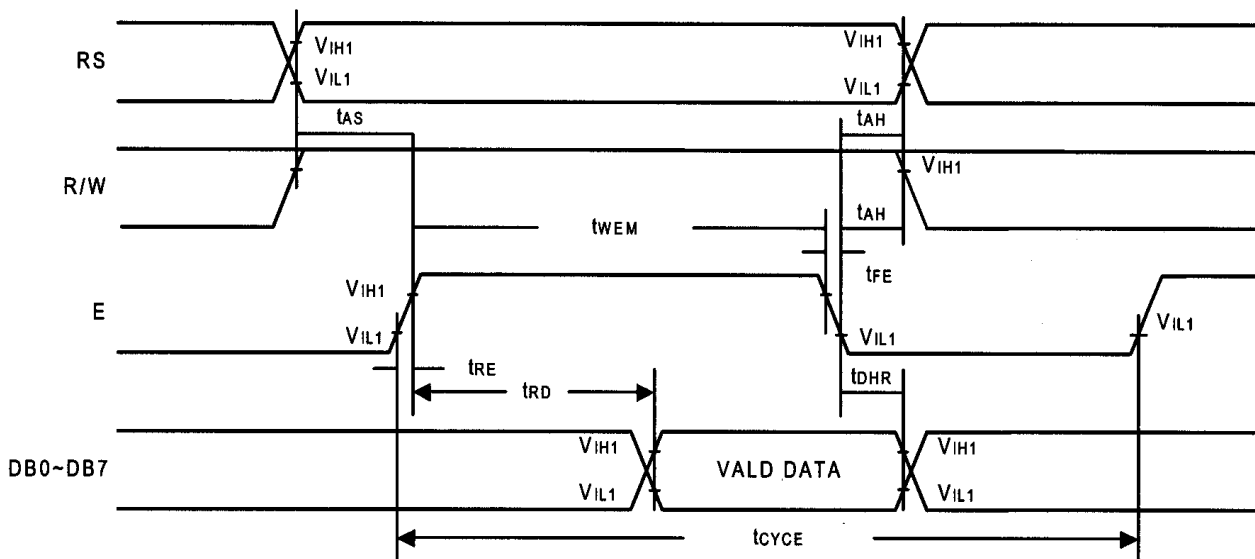


Figure 3: Bus read operation sequence (Reading out data from NT3881 to MPU).



#### 4.4 Timing Diagram of VDD against V0.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.

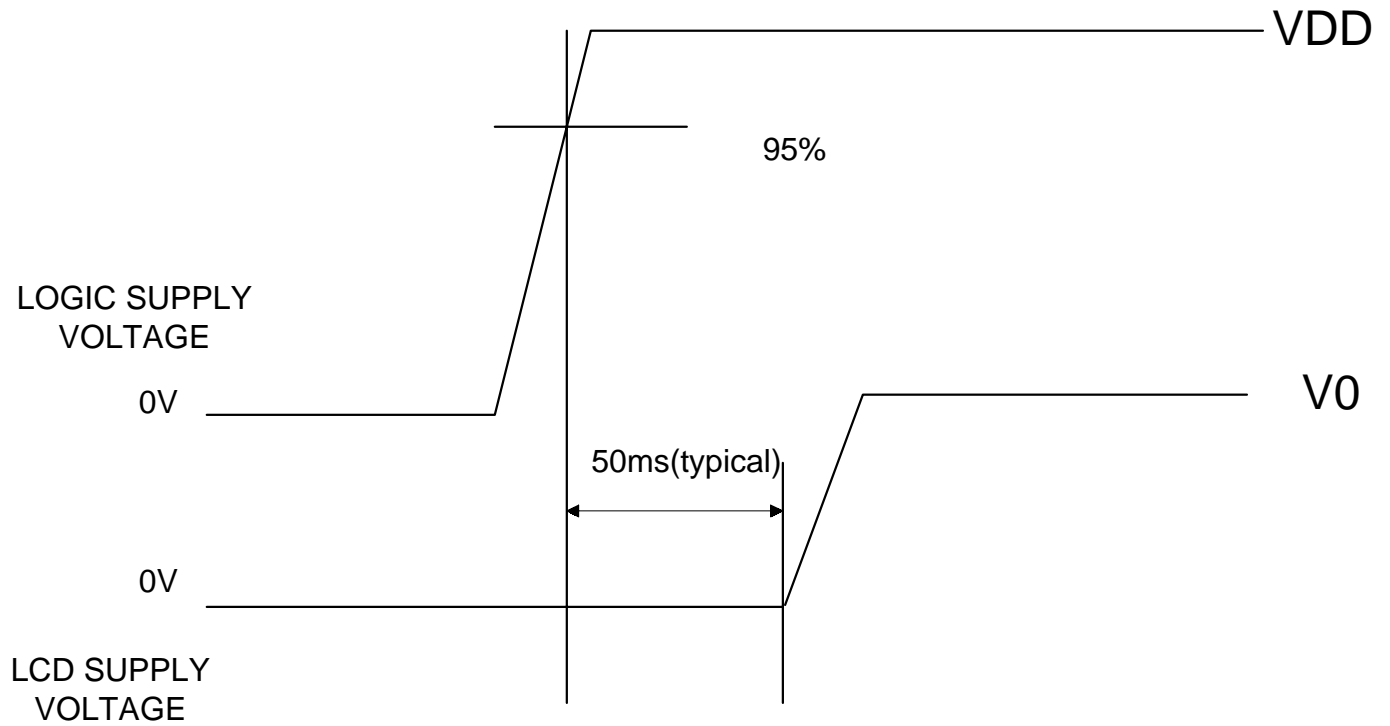


Figure 4: Timing diagram of VDD against V0.



**4.5 Correspondence between Character Codes and Character Patterns**  
**(NOVATEK Standard NT3881D-01)**

		Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)																	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F		
Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	0	CG RAM (1)			0	a	P	`	P					一	夕	三	o	p	
	1	CG RAM (2)		!	1	A	Q	a	9					。	ア	チ	△	ä	9
	2	CG RAM (3)		"	2	B	R	b	r					「	イ	ツ	×	ρ	θ
	3	CG RAM (4)		#	3	C	S	c	s					」	ウ	テ	テ	ε	ω
	4	CG RAM (5)		\$	4	D	T	d	t					、	イ	ト	ト	μ	Ω
	5	CG RAM (6)		%	5	E	U	e	u					。	オ	ナ	1	δ	ü
	6	CG RAM (7)		&	6	F	V	f	v					ヲ	カ	ニ	ヨ	ρ	Σ
	7	CG RAM (8)		'	7	G	W	g	w					ア	十	又	ラ	9	π
	8	CG RAM (1)		(	8	H	X	h	x					イ	ク	本	リ	γ	×
	9	CG RAM (2)		)	9	I	Y	i	y					ウ	ケ	リ	ル	-	γ
	A	CG RAM (3)		*	:	J	Z	j	z					エ	コ	ン	レ	j	〒
	B	CG RAM (4)		+	;	K	C	k	c					オ	サ	ヒ	ロ	*	斤
	C	CG RAM (5)		,	<	L	¥	l	l					カ	シ	フ	ワ	φ	円
	D	CG RAM (6)		-	=	M	I	m	3					ユ	ズ	△	ン	ト	÷
	E	CG RAM (7)		.	>	N	^	n	→					ヨ	セ	ホ	°	ん	
	F	CG RAM (8)		/	?	O	_	o	+					ウ	リ	マ	°	ö	

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