

# IS41LV32256



## 256K x 32 (8-Mbit) EDO DYNAMIC RAM 3.3V, 100/83/66 MHz

SEPTEMBER 2000

### FEATURES

- 262,144-word by 32-bit organization
- Single +3.3V  $\pm$  0.3V power supply
- Four  $\overline{\text{CAS}}$  inputs for Byte Write and Byte Read control
- Refresh modes:  $\overline{\text{RAS}}$ -Only,  $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  (CBR), and Hidden
- 512-cycle refresh in 8 ms
- Fast Page Mode with Extended Data Out
- 100-pin PQFP, TQFP package

### DESCRIPTION

The *ISSI* IS41LV32256 is organized in a 262,122 x 32-bit CMOS Dynamic Random Access Memory. Four  $\overline{\text{CAS}}$  signals facilitate execution of Byte Read and Byte Write operations. A very fast EDO cycle time of 10 ns allows an operating frequency of 100 MHz and makes the IS41LV32256 an ideal frame buffer memory for graphics applications.

The IS41LV32256 is compatible with JEDEC standard SGRAMs. This 8-Mbit EDO memory offers a significantly lower latency and a faster memory cycle than the SGRAM. *ISSI's* IS41LV32256 3.3V 256K x 32 device is pin/voltage compatible with all standard SGRAM parts.

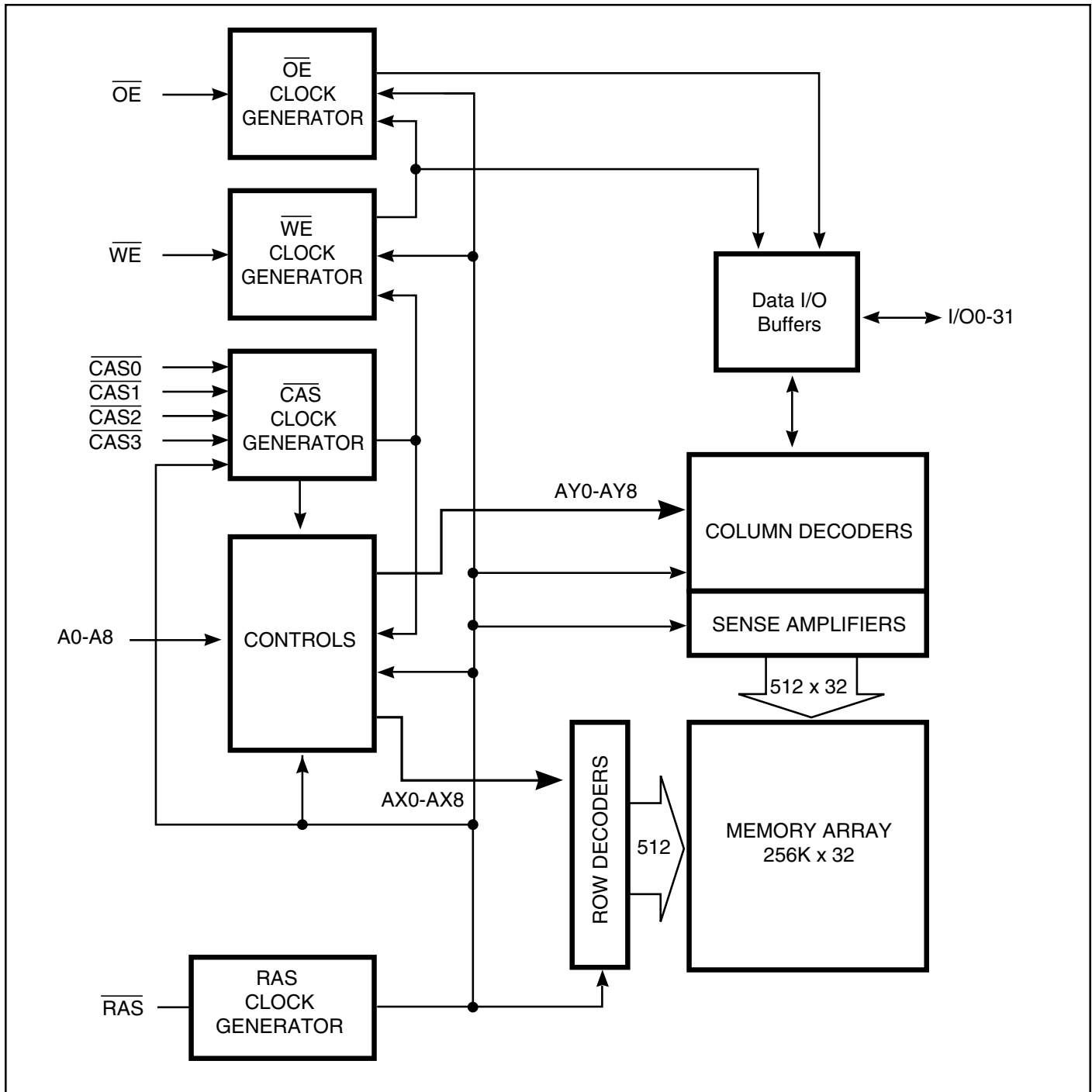
The IS41LV32256 is available in a 100-pin PQFP and TQFP package.

### KEY TIMING PARAMETERS

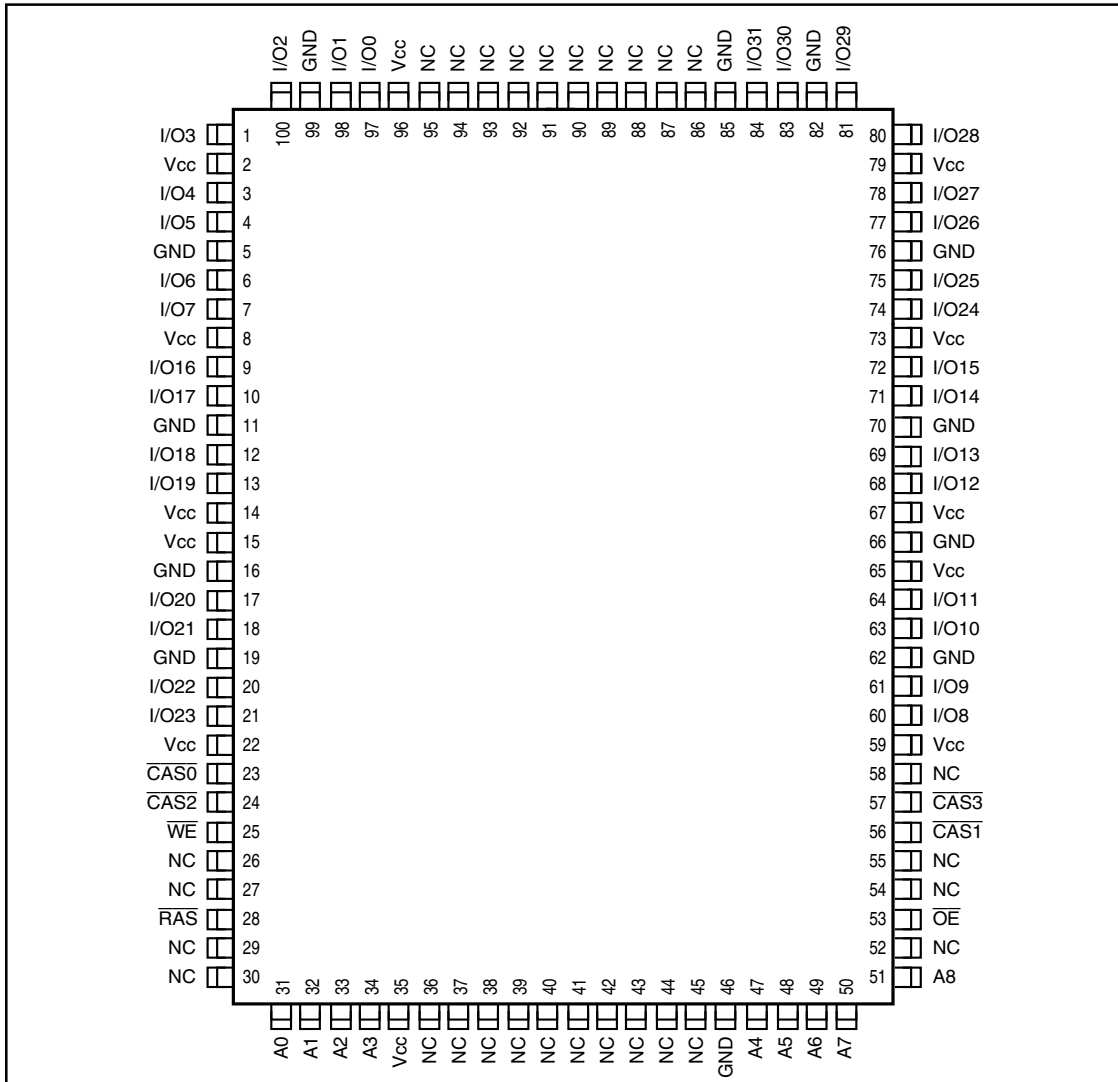
Parameter	-28	-30	-35	Unit
Max. $\overline{\text{RAS}}$ Access Time ( $t_{\text{RAC}}$ )	28	30	35	ns
Max. $\overline{\text{CAS}}$ Access Time ( $t_{\text{CAC}}$ )	9	9	10	ns
Max. Column Address Access Time ( $t_{\text{AA}}$ )	15	16	18	ns
Max. $\overline{\text{OE}}$ Access Time ( $t_{\text{OE}}$ )	9	9	10	ns
Min. Read/Write Cycle Time ( $t_{\text{RC}}$ )	48	53	60	ns
Min. EDO Cycle Time ( $t_{\text{PC}}$ )	12	12	15	ns

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FUNCTIONAL BLOCK DIAGRAM



**PIN CONFIGURATIONS**  
**100-Pin PQFP, TQFP**



**PIN DESCRIPTIONS**

A0-A8	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS0}}$	Column Address Strobe for First Byte (I/O0-I/O7)
$\overline{\text{CAS1}}$	Column Address Strobe for Second Byte (I/O8-I/O15)
$\overline{\text{CAS2}}$	Column Address Strobe for Third Byte (I/O16-I/O23)
$\overline{\text{CAS3}}$	Column Address Strobe for Fourth Byte (I/O24-I/O31)
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
I/O0-I/O31	Data Inputs/Outputs
Vcc	+3.3V Supply
GND	Ground
NC	No Connection: This pin should be left unconnected or tied to ground.

## TRUTH TABLE

Function	$\overline{\text{RAS}}$	$\overline{\text{CAS0}}$	$\overline{\text{CAS1}}$	$\overline{\text{CAS2}}$	$\overline{\text{CAS3}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Address	I/O
Standby	H	H	H	H	H	X	X	X	High-Z
Read: Double Word	L	L	L	L	L	H	L	ROW/COL	DOUT
Read: 1st Byte	L	L	H	H	H	H	L	ROW/COL	I/O0-7=DOUT; I/O8-31=High-Z
Read: 2nd Byte	L	H	L	H	H	H	L	ROW/COL	I/O0-7=High-Z; I/O8-15=DOUT; I/O16-31=High-Z
Read: 3rd Byte	L	H	H	L	H	H	L	ROW/COL	I/O0-15=High-Z; I/O16-23=DOUT; I/O24-31=High-Z
Read: 4th Byte	L	H	H	H	L	H	L	ROW/COL	I/O0-23=High-Z; I/O24-31=DOUT
Write: Double Word (Early)	L	L	L	L	L	L	X	ROW/COL	DIN
Write: 1st Byte (Early)	L	L	H	H	H	L	X	ROW/COL	I/O0-7=DIN; I/O8-31=X
Write: 2nd Byte (Early)	L	H	L	H	H	L	X	ROW/COL	I/O0-8=X; I/O8-15=DIN; I/O16-31=X
Write: 3rd Byte (Early)	L	H	H	L	H	L	X	ROW/COL	I/O0-15=X; I/O16-23=DIN; I/O24-31=X
Write: 4th Byte (Early)	L	H	H	H	L	L	X	ROW/COL	I/O0-23=X; I/O24-31=DIN
Read-Write <sup>(1,2)</sup>	L	L	L	L	L	H $\emptyset$ L	L $\emptyset$ H	ROW/COL	DOUT $\emptyset$ DIN
Fast-Page-Mode Read: EDO <sup>(2)</sup> 1st Cycle:	L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	H	L	ROW/COL	DOUT
Subsequent Cycles:	L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	H	L	COL	DOUT
Fast-Page-Mode Read: High-Z <sup>(2)</sup> 1st Cycle:	L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	H	H $\emptyset$ L	ROW/COL	DOUT
Subsequent Cycles:	L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	H	H $\emptyset$ L	COL	DOUT
Fast-Page-Mode Write: (Early) <sup>(1)</sup> 1st Cycle:	L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	L	X	ROW/COL	DIN
Subsequent Cycles:	L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	L	X	COL	DIN
Fast-Page-Mode Read-Write <sup>(1,2)</sup> 1st Cycle:	L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	L $\emptyset$ H	ROW/COL	DOUT $\emptyset$ DIN
Subsequent Cycles:	L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	H $\emptyset$ L	L $\emptyset$ H	COL	DOUT $\emptyset$ DIN
Hidden Refresh Read <sup>(2)</sup>	L $\emptyset$ H $\emptyset$ L	L	L	L	L	H	L	ROW/COL	DOUT
Hidden Refresh Write <sup>(1)</sup>	L $\emptyset$ H $\emptyset$ L	L	L	L	L	L	X	ROW/COL	DIN $\emptyset$ High-Z
$\overline{\text{RAS}}$ -Only Refresh	L	H	H	H	H	X	X	ROW	High-Z
CBR Refresh <sup>(3)</sup>	H $\emptyset$ L	L	L	L	L	X	X	X	High-Z

**Notes:**

1. BYTE WRITE may be executed with  $\overline{\text{CAS0}}$ ,  $\overline{\text{CAS1}}$ ,  $\overline{\text{CAS2}}$  or  $\overline{\text{CAS3}}$  active.
2. BYTE READ may be executed with  $\overline{\text{CAS0}}$ ,  $\overline{\text{CAS1}}$ ,  $\overline{\text{CAS2}}$  or  $\overline{\text{CAS3}}$  active.
3. Only one  $\overline{\text{CAS}}$  signal ( $\overline{\text{CAS0}}$ ,  $\overline{\text{CAS1}}$ ,  $\overline{\text{CAS2}}$  or  $\overline{\text{CAS3}}$ ) must be active.

## POWER-ON

The initial application of the  $V_{CC}$  supply requires a 200- $\mu$ s wait followed by a minimum of any eight initialization cycles containing a  $\overline{\text{RAS}}$  clock. During Power-On, the  $V_{CC}$  current is dependent on the input levels of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ . It is recommended that  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  track with  $V_{CC}$  or be held at a valid  $V_{IH}$  during Power-On to avoid current surges.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameters	Rating	Unit
$t_A$	Ambient Temperature Under Bias	-1.0 to +80	°C
$t_{STG}$	Storage Temperature	-50 to +125	°C
$V_T$	Voltage Relative to GND	-1.0 to +5.5	V
$I_{OUT}$	Data Output Current	50	mA
$P_D$	Power Dissipation	1.0	W

### Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup> ( $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ )

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{CC}$	Power Supply	3.0	3.3	3.6	V
$V_{IH}$	Input High Voltage	2.4	—	$V_{CC} + 0.5$	V
$V_{IL}$	Input Low Voltage	-0.5	—	0.4	V

### Note:

1. Voltages are referenced to GND.

## CAPACITANCE<sup>(1,2)</sup>

Symbol	Parameter	Max.	Unit
$C_{IN}$	Input Capacitance	5	pF
$C_{IO}$	Data Input/Output Capacitance	7	pF

### Notes:

1. Capacitance is sampled and 100% tested.
2. Test conditions:  $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{CC} = 3.3\text{V}$ .

**DC CHARACTERISTICS** ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ )

Symbol	Parameter	Condition	-28		-30		-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
$V_{IH}$	Input HIGH (Logic 1) Voltage, All Inputs	—	2.0	$V_{CC} + 0.5$	2.0	$V_{CC} + 0.5$	2.0	$V_{CC} + 0.5$	V
$V_{IL}$	Input LOW (Logic 1) Voltage, All Inputs	—	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -2\text{ mA}$	2.4	$V_{CC}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2\text{ mA}$	0	0.4	0	0.4	0	0.4	V
$I_{LI}$	Input Leakage Current	$0\text{V} < V_{IN} < V_{CC}$	-10	10	-10	10	-10	10	$\mu\text{A}$
$I_{LO}$	Output Leakage Current	$0\text{V} < V_{OUT} < 3.6\text{V}$ ; Output Disable	-10	10	-10	10	-10	10	$\mu\text{A}$
$I_{CC1}$	Average Power Supply Current (Operating) <sup>(2,3,15,16)</sup>	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ Cycling; $t_{RC} = \text{Min.}$	—	250	—	250	—	240	mA
$I_{CC2}$	Power Supply Current (Standby)	$\overline{\text{RAS}}$ , $\overline{\text{CAS}} = V_{IH}$	—	2.5	—	2.5	—	2.5	mA
$I_{CC3}$	Average Power Supply Current ( $\overline{\text{RAS}}$ -Only Refresh) <sup>(2,3,15,16)</sup>	$\overline{\text{RAS}} = \text{Cycling}$ ; $\overline{\text{CAS}} = V_{IH}$ ; $t_{RC} = \text{Min.}$	—	250	—	250	—	240	mA
$I_{CC4}$	Average Power Supply Current (Fast Page Mode) <sup>(2,3,15,18)</sup>	$\overline{\text{RAS}} = V_{IL}$ ; $\overline{\text{CAS}} = \text{Cycling}$ ; $t_{PC} = \text{Min.}$	—	230	—	230	—	220	mA
$I_{CC5}$	Average Power Supply Current ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh) <sup>(2,3,15,16)</sup>	$\overline{\text{RAS}} = \text{Cycling}$ ; $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$	—	250	—	250	—	240	mA
$I_{CC6}$	CMOS Standby Current	$\overline{\text{RAS}}$ , $\overline{\text{CAS}} = V_{CC} - 0.2\text{V}$	—	600	—	600	—	600	$\mu\text{A}$

**AC CHARACTERISTICS**<sup>(1,2,3,4,5,6)</sup> (Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-28		-30		-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Random READ or WRITE Cycle Time	48	—	53	—	60	—	ns
$t_{RAC}$	Access Time from $\overline{\text{RAS}}$ <sup>(6, 7)</sup>	—	28	—	30	—	35	ns
$t_{CAC}$	Access Time from $\overline{\text{CAS}}$ <sup>(6, 8, 15)</sup>	—	9	—	9	—	10	ns
$t_{AA}$	Access Time from Column-Address <sup>(6)</sup>	—	15	—	16	—	18	ns
$t_{RAS}$	$\overline{\text{RAS}}$ Pulse Width	28	10K	30	10K	35	10K	ns
$t_{RP}$	$\overline{\text{RAS}}$ Precharge Time	17	—	18	—	20	—	ns
$t_{CAS}$	$\overline{\text{CAS}}$ Pulse Width <sup>(26)</sup>	5	10K	5	10K	6	10K	ns
$t_{CP}$	$\overline{\text{CAS}}$ Precharge Time <sup>(9, 25)</sup>	5	—	5	—	5	—	ns
$t_{CSH}$	$\overline{\text{CAS}}$ Hold Time <sup>(21)</sup>	28	—	30	—	35	—	ns
$t_{RCD}$	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time <sup>(10, 20)</sup>	10	19	10	21	11	28	ns
$t_{ASR}$	Row-Address Setup Time	0	—	0	—	0	—	ns
$t_{RAH}$	Row-Address Hold Time	6	—	6	—	7	—	ns
$t_{ASC}$	Column-Address Setup Time <sup>(20)</sup>	0	—	0	—	0	—	ns
$t_{CAH}$	Column-Address Hold Time <sup>(20)</sup>	5	—	5	—	6	—	ns
$t_{AR}$	Column-Address Hold Time (referenced to $\overline{\text{RAS}}$ )	21	—	22	—	25	—	ns
$t_{RAD}$	$\overline{\text{RAS}}$ to Column-Address Delay Time <sup>(11)</sup>	8	13	8	15	9	16	ns
$t_{RAL}$	Column-Address to $\overline{\text{RAS}}$ Lead Time	15	—	16	—	18	—	ns
$t_{RPC}$	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	0	—	0	—	0	—	ns
$t_{RSH}$	$\overline{\text{RAS}}$ Hold Time <sup>(27)</sup>	7	—	7	—	8	—	ns

(Continued)

**AC CHARACTERISTICS**<sup>(1,2,3,4,5,6)</sup> (Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-28		-30		-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
tCLZ	CAS to Output in Low-Z <sup>(15, 29)</sup>	3	—	3	—	3	—	ns
tCRP	CAS to RAS Precharge Time <sup>(21)</sup>	5	—	5	—	5	—	ns
tOD	Output Disable Time <sup>(19, 28, 29)</sup>	3	15	3	15	3	15	ns
tOE	Output Enable Time <sup>(15, 16)</sup>	—	9	—	9	—	10	ns
tOEH	OE HIGH Hold Time from CAS HIGH	10	—	10	—	10	—	ns
tOEP	OE HIGH Pulse Width	10	—	10	—	10	—	ns
tOES	OE LOW to CAS HIGH Setup Time	5	—	5	—	5	—	ns
tRCS	Read Command Setup Time <sup>(17, 20)</sup>	0	—	0	—	0	—	ns
tRRH	Read Command Hold Time (referenced to RAS) <sup>(12)</sup>	0	—	0	—	0	—	ns
tRCH	Read Command Hold Time (referenced to CAS) <sup>(12, 17, 21)</sup>	0	—	0	—	0	—	ns
twCH	Write Command Hold Time <sup>(17, 27)</sup>	5	—	5	—	5	—	ns
twCR	Write Command Hold Time (referenced to RAS) <sup>(17)</sup>	21	—	22	—	24	—	ns
tWP	Write Command Pulse Width <sup>(17)</sup>	5	—	5	—	6	—	ns
tWPZ	WE Pulse Widths to Disable Outputs	10	—	10	—	10	—	ns
tRWL	Write Command to RAS Lead Time <sup>(17)</sup>	7	—	7	—	8	—	ns
tcWL	Write Command to CAS Lead Time <sup>(17, 21)</sup>	5	—	5	—	8	—	ns
twCS	Write Command Setup Time <sup>(14, 17, 20)</sup>	0	—	0	—	0	—	ns
tdHR	Data-in Hold Time (referenced to RAS)	21	—	22	—	24	—	ns
tACH	Column-Address Setup Time to CAS Precharge during WRITE Cycle	15	—	15	—	15	—	ns
tOEH	OE Hold Time from WE during READ-MODIFY-WRITE cycle <sup>(18)</sup>	5	—	5	—	6	—	ns
tDS	Data-In Setup Time <sup>(15, 22)</sup>	0	—	0	—	0	—	ns
tdH	Data-In Hold Time <sup>(15, 22)</sup>	5	—	5	—	6	—	ns
tRWC	READ-MODIFY-WRITE Cycle Time	73	—	73	—	80	—	ns
tRWD	RAS to WE Delay Time during READ-MODIFY-WRITE Cycle <sup>(14)</sup>	40	—	40	—	45	—	ns
tcWD	CAS to WE Delay Time <sup>(14, 20)</sup>	18	—	18	—	20	—	ns
tAWD	Column-Address to WE Delay Time <sup>(14)</sup>	24	—	25	—	30	—	ns
tPC	EDO Page Mode READ or WRITE Cycle Time <sup>(24)</sup>	12	—	12	—	15	—	ns
tRASP	RAS Pulse Width in EDO Page Mode	28	100K	30	100K	35	100K	ns
tCPA	Access Time from CAS Precharge <sup>(15)</sup>	—	17	—	18	—	21	ns
tPRWC	EDO Page Mode READ-WRITE Cycle Time <sup>(24)</sup>	34	—	35	—	40	—	ns
tCHO	Data Output Hold after CAS LOW	3	—	3	—	3	—	ns
tOFF	Output Buffer Turn-Off Delay from CAS or RAS <sup>(13, 15, 19, 29)</sup>	3	7	3	7	3	15	ns
tWHZ	Output Disable Delay from WE	3	10	3	10	3	15	ns

(Continued)

**AC CHARACTERISTICS**<sup>(1,2,3,4,5,6)</sup> (Recommended Operating Conditions unless otherwise noted.)

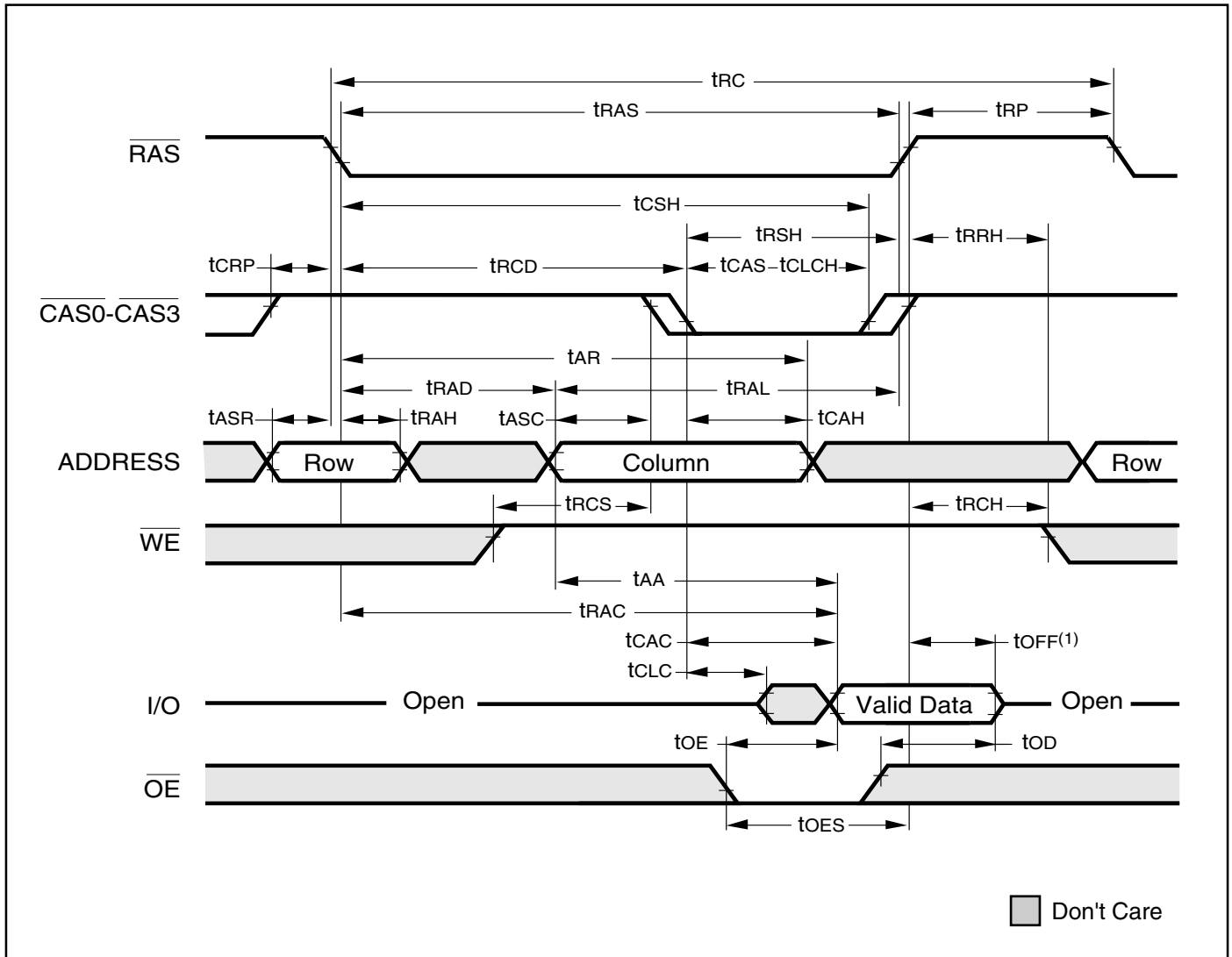
Symbol	Parameter	-28		-30		-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>CLCH</sub>	Last $\overline{\text{CAS}}$ going LOW to First $\overline{\text{CAS}}$ returning HIGH <sup>(23)</sup>	10	—	10	—	10	—	ns
t <sub>CSR</sub>	$\overline{\text{CAS}}$ Setup Time (CBR REFRESH) <sup>(30, 20)</sup>	5	—	5	—	8	—	ns
t <sub>CHR</sub>	$\overline{\text{CAS}}$ Hold Time (CBR REFRESH) <sup>(30, 21)</sup>	7	—	7	—	8	—	ns
t <sub>ORD</sub>	$\overline{\text{OE}}$ Setup Time prior to $\overline{\text{RAS}}$ during HIDDEN REFRESH Cycle	0	—	0	—	0	—	ns
t <sub>REF</sub>	Refresh Period (512 Cycles)	—	8	—	8	—	8	ms
t <sub>r</sub>	Transition Time (Rise or Fall) <sup>(2, 3)</sup>	1	50	1	50	1	50	ns

**Notes:**

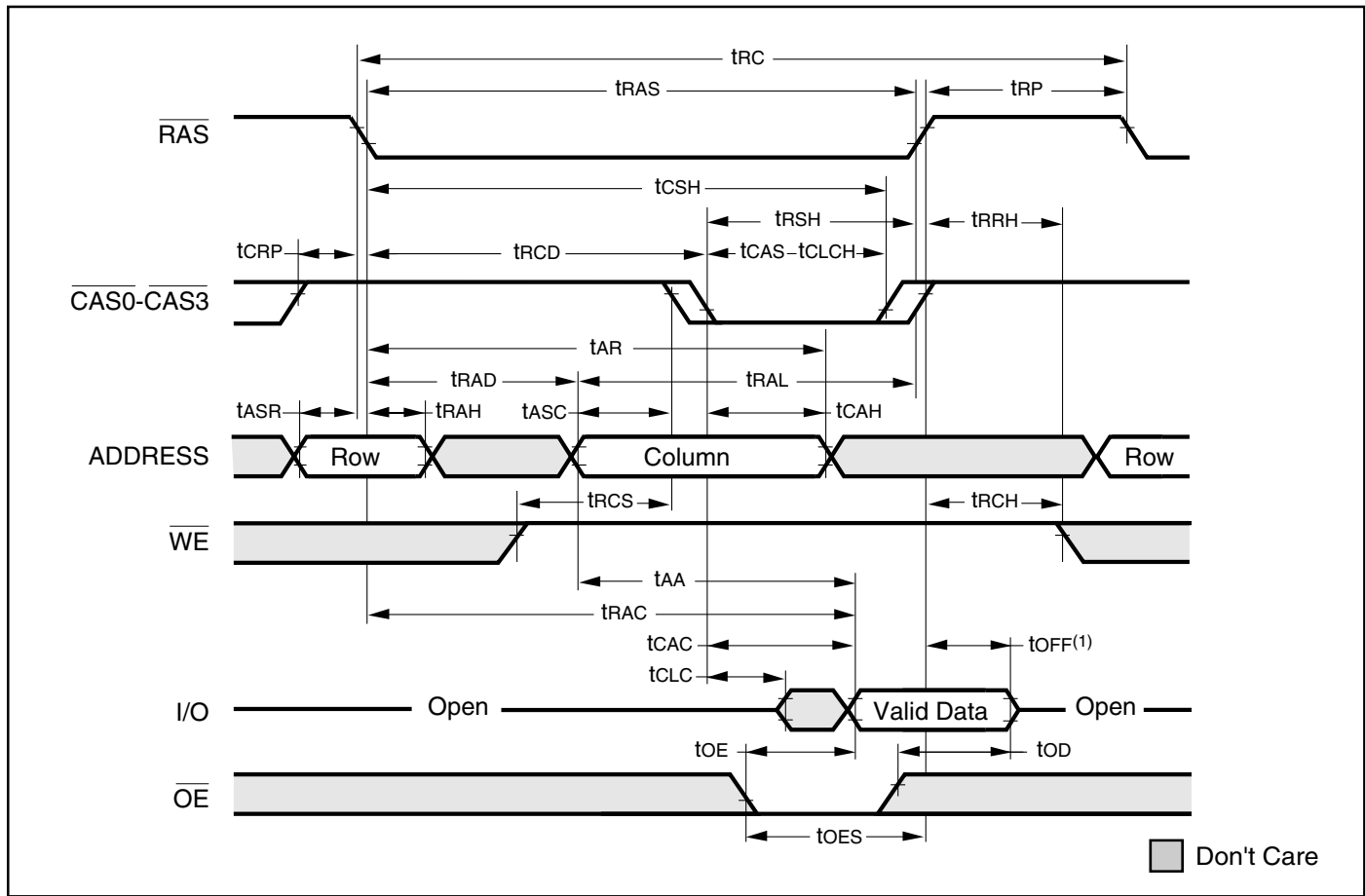
- An initial pause of 200  $\mu\text{s}$  is required after power-up followed by eight  $\overline{\text{RAS}}$  refresh cycle ( $\overline{\text{RAS}}$ -Only or CBR) before proper device operation is assured. The eight  $\overline{\text{RAS}}$  cycles wake-up should be repeated any time the t<sub>REF</sub> refresh requirement is exceeded.
- V<sub>IH</sub> (MIN) and V<sub>IL</sub> (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>) and assume to be 1 ns for all inputs.
- In addition to meeting the transition rate specification, all input signals must transit between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>) in a monotonic manner.
- If  $\overline{\text{CAS}}$  and  $\overline{\text{RAS}} = \text{V}_{\text{IH}}$ , data output is High-Z.
- If  $\overline{\text{CAS}} = \text{V}_{\text{IL}}$ , data output may contain data from the last valid READ cycle.
- Measured with a load equivalent to one TTL gate and 50 pF.
- Assumes that t<sub>RCD</sub> - t<sub>RCD</sub> (MAX). If t<sub>RCD</sub> is greater than the maximum recommended value shown in this table, t<sub>RAC</sub> will increase by the amount that t<sub>RCD</sub> exceeds the value shown.
- Assumes that t<sub>RCD</sub> • t<sub>RCD</sub> (MAX).
- If  $\overline{\text{CAS}}$  is LOW at the falling edge of  $\overline{\text{RAS}}$ , data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer,  $\overline{\text{CAS}}$  and  $\overline{\text{RAS}}$  must be pulsed for t<sub>CP</sub>.
- Operation with the t<sub>RCD</sub> (MAX) limit ensures that t<sub>RAC</sub> (MAX) can be met. t<sub>RCD</sub> (MAX) is specified as a reference point only; if t<sub>RCD</sub> is greater than the specified t<sub>RCD</sub> (MAX) limit, access time is controlled exclusively by t<sub>CAC</sub>.
- Operation within the t<sub>RAD</sub> (MAX) limit ensures that t<sub>RCD</sub> (MAX) can be met. t<sub>RAD</sub> (MAX) is specified as a reference point only; if t<sub>RAD</sub> is greater than the specified t<sub>RAD</sub> (MAX) limit, access time is controlled exclusively by t<sub>AA</sub>.
- Either t<sub>RCH</sub> or t<sub>RRH</sub> must be satisfied for a READ cycle.
- t<sub>OFF</sub> (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V<sub>OH</sub> or V<sub>OL</sub>.
- t<sub>WCS</sub>, t<sub>RWD</sub>, t<sub>AWD</sub> and t<sub>CWD</sub> are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If t<sub>WCS</sub> • t<sub>WCS</sub> (MIN), the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If t<sub>RWD</sub> • t<sub>RWD</sub> (MIN), t<sub>AWD</sub> • t<sub>AWD</sub> (MIN) and t<sub>CWD</sub> • t<sub>CWD</sub> (MIN), the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until  $\overline{\text{CAS}}$  and  $\overline{\text{RAS}}$  or  $\overline{\text{OE}}$  go back to V<sub>IH</sub>) is indeterminate.  $\overline{\text{OE}}$  held HIGH and  $\overline{\text{WE}}$  taken LOW after  $\overline{\text{CAS}}$  goes LOW result in a LATE WRITE ( $\overline{\text{OE}}$ -controlled) cycle.
- Output parameter (I/O) is referenced to corresponding  $\overline{\text{CAS}}$  input, I/O0-I/O7 by  $\overline{\text{LCAS}}$  and I/O8-I/O15 by  $\overline{\text{UCAS}}$ .
- During a READ cycle, if  $\overline{\text{OE}}$  is LOW then taken HIGH before  $\overline{\text{CAS}}$  goes HIGH, I/O goes open. If  $\overline{\text{OE}}$  is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
- Write command is defined as  $\overline{\text{WE}}$  going low.
- LATE WRITE and READ-MODIFY-WRITE cycles must have both t<sub>OD</sub> and t<sub>OEH</sub> met ( $\overline{\text{OE}}$  HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if  $\overline{\text{CAS}}$  remains LOW and  $\overline{\text{OE}}$  is taken back to LOW after t<sub>OEH</sub> is met.
- The I/Os are in open during READ cycles once t<sub>OD</sub> or t<sub>OFF</sub> occur.
- The first  $\chi\overline{\text{CAS}}$  edge to transition LOW.
- The last  $\chi\overline{\text{CAS}}$  edge to transition HIGH.
- These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in EARLY WRITE cycles and  $\overline{\text{WE}}$  leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
- Last falling  $\chi\overline{\text{CAS}}$  edge to first rising  $\chi\overline{\text{CAS}}$  edge.
- Last rising  $\chi\overline{\text{CAS}}$  edge to next cycle's last rising  $\chi\overline{\text{CAS}}$  edge.
- Last rising  $\chi\overline{\text{CAS}}$  edge to first falling  $\chi\overline{\text{CAS}}$  edge.
- Each  $\chi\overline{\text{CAS}}$  must meet minimum pulse width.
- Last  $\chi\overline{\text{CAS}}$  to go LOW.
- I/Os controlled, regardless  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ .
- The 3 ns minimum is a parameter guaranteed by design.
- Enables on-chip refresh and address counters.



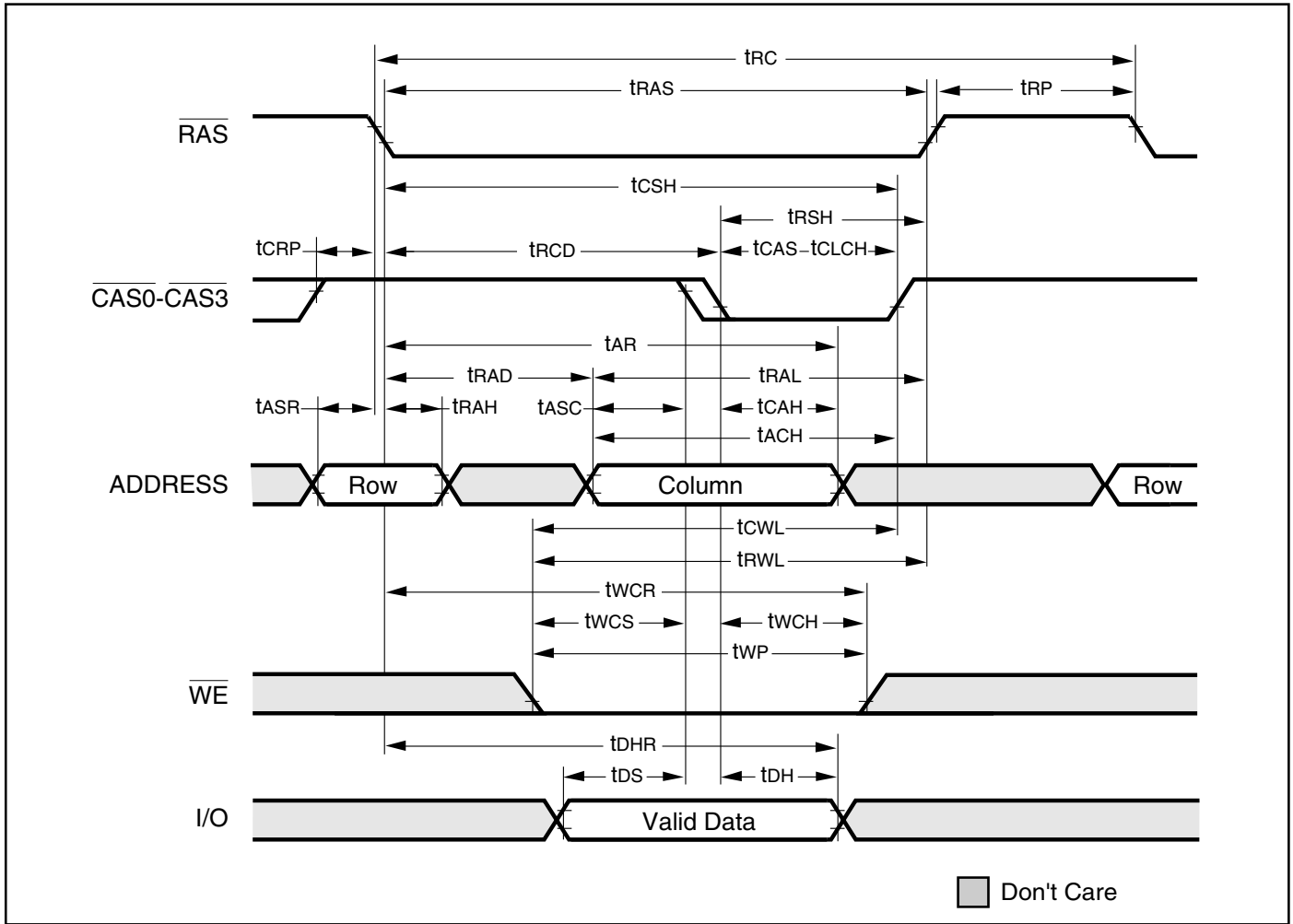
**READ CYCLE** (Outputs Controlled by  $\overline{\text{RAS}}$ )



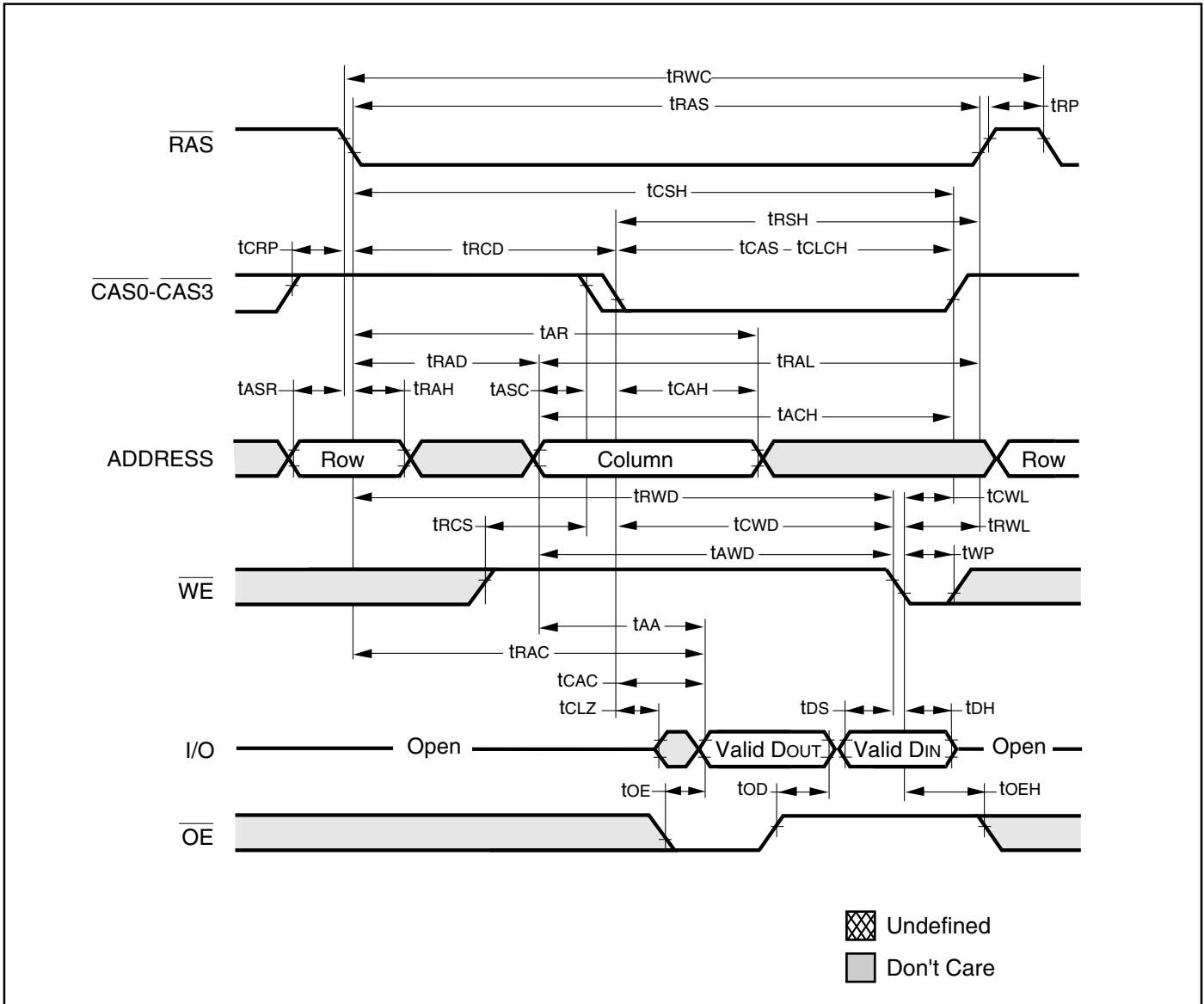
**READ CYCLE** (Outputs Controlled by  $\overline{\text{CAS}}$ )



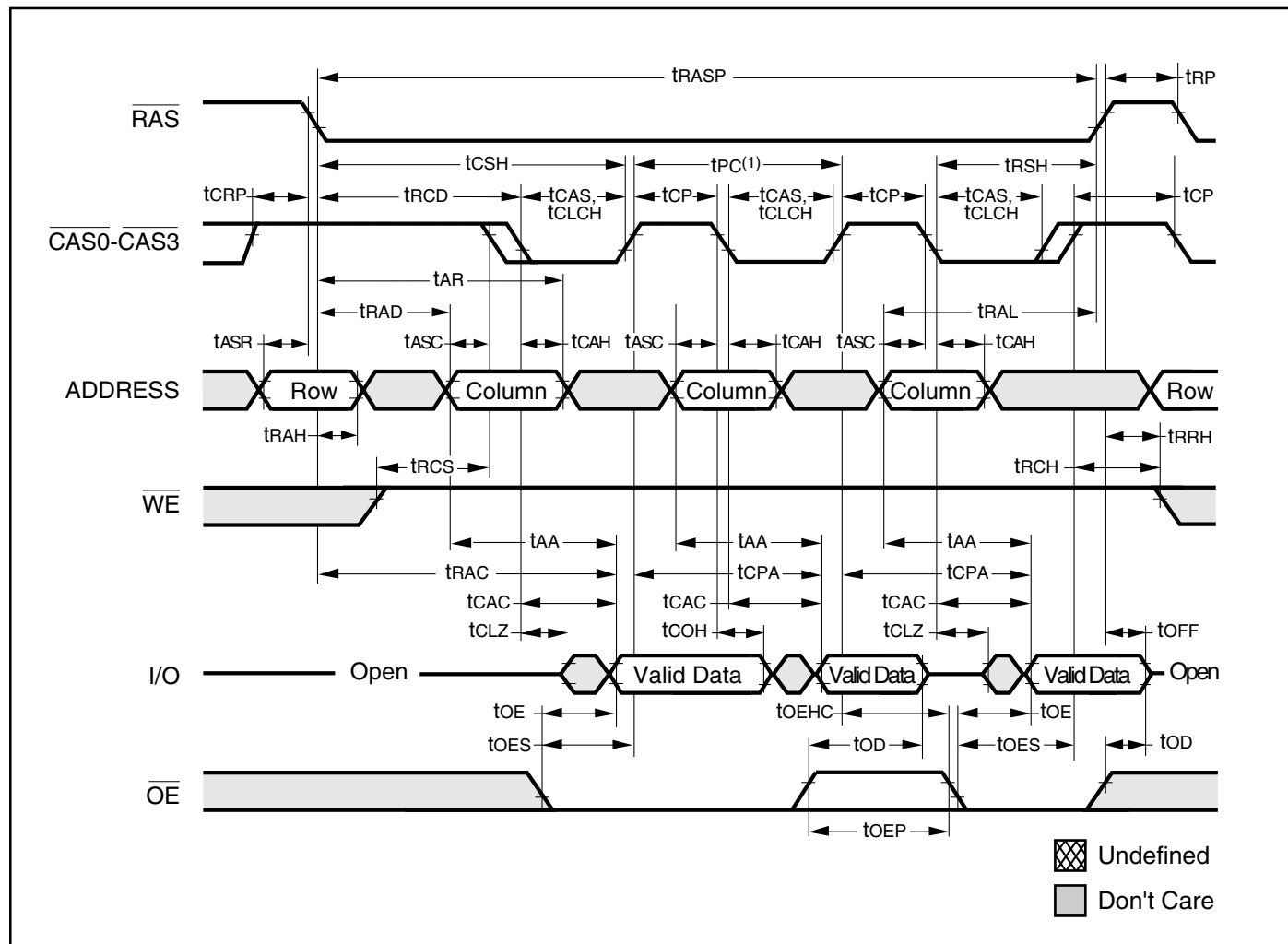
**EARLY WRITE CYCLE ( $\overline{OE}$  = DON'T CARE)**



READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)



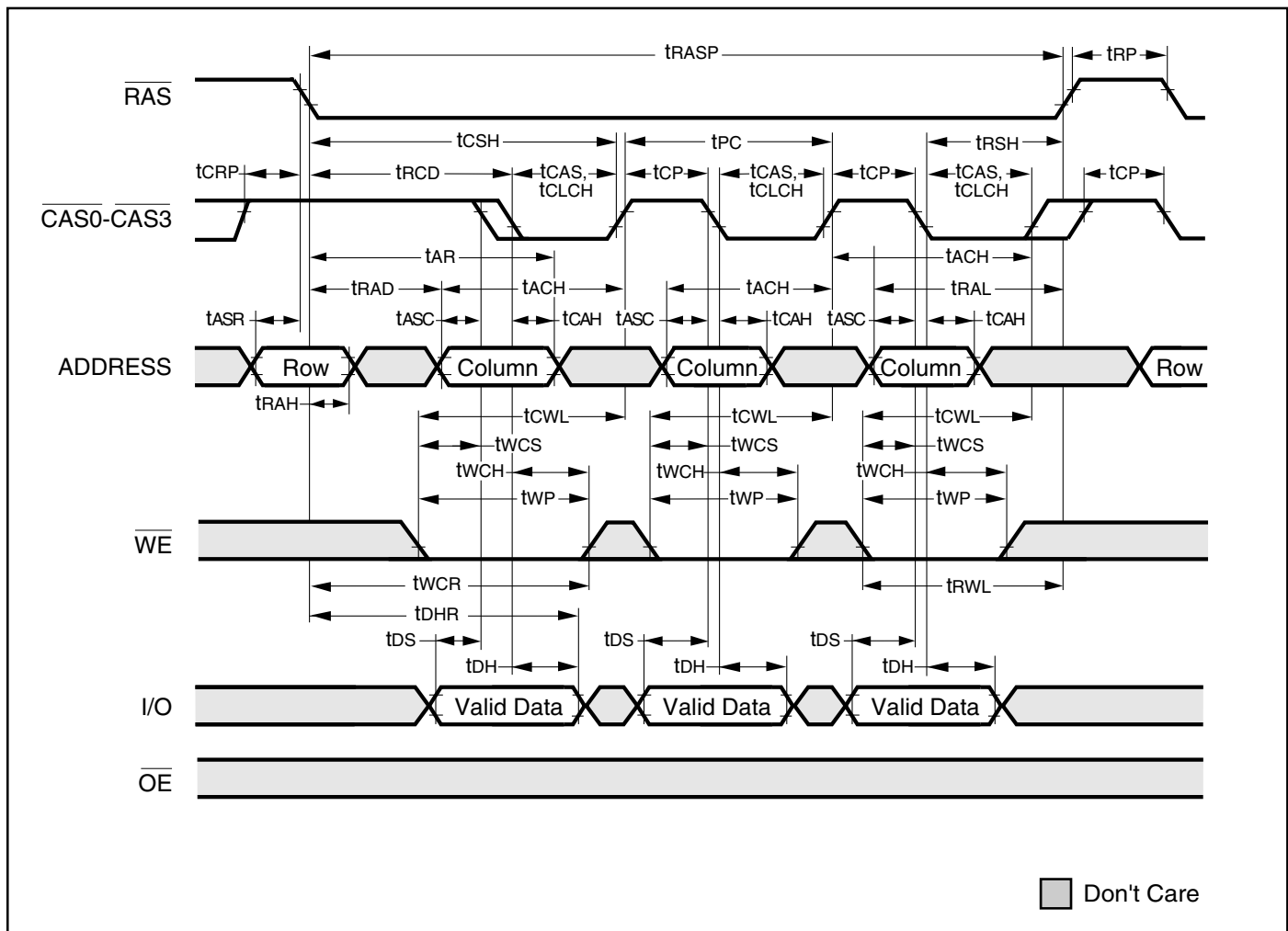
EDO-PAGE-MODE READ CYCLE



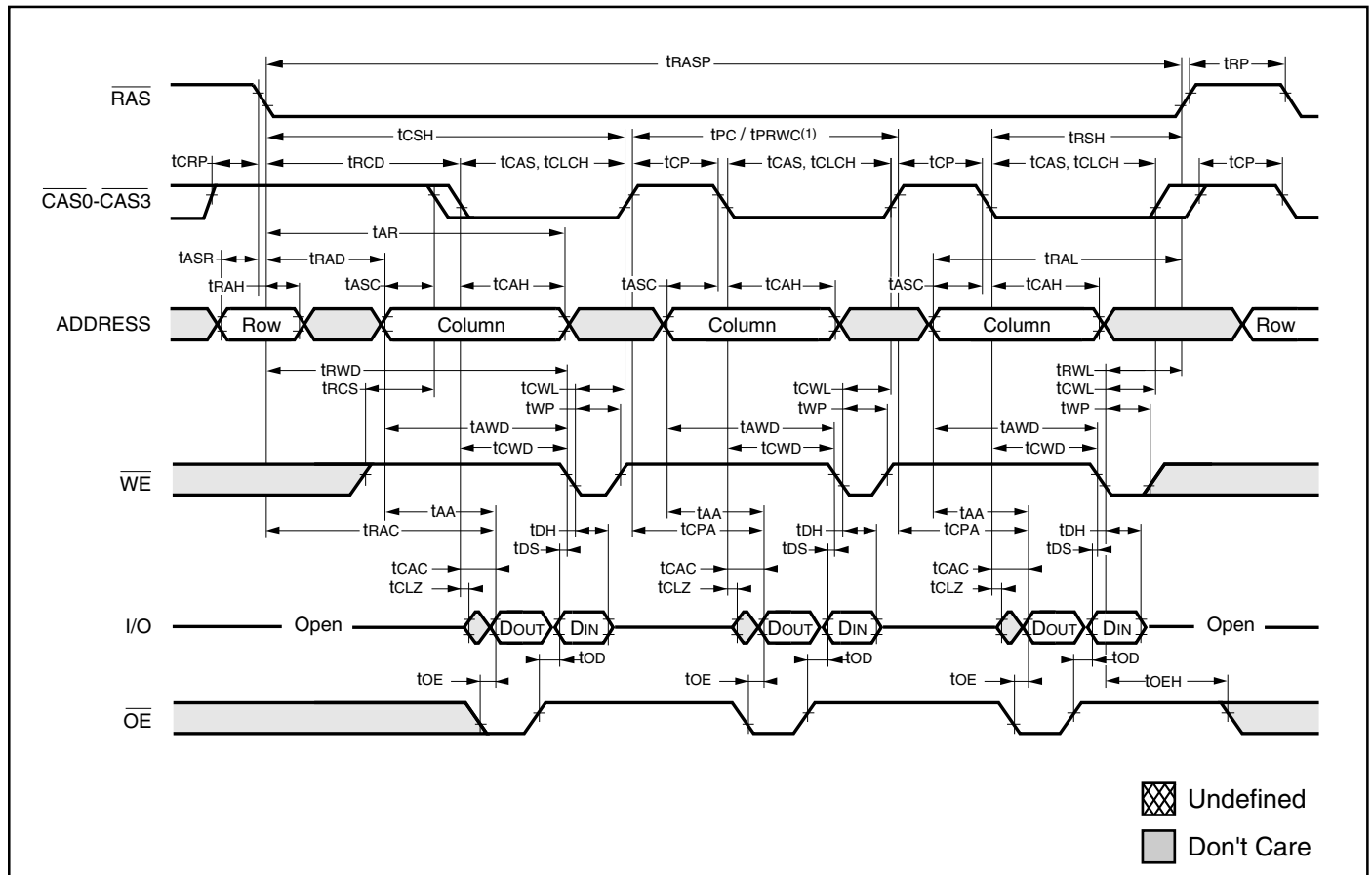
Note:

1.  $t_{\text{PC}}$  can be measured from falling edge of  $\overline{\text{CAS}}$  to falling edge of  $\overline{\text{CAS}}$ , or from rising edge of  $\overline{\text{CAS}}$  to rising edge of  $\overline{\text{CAS}}$ . Both measurements must meet the  $t_{\text{PC}}$  specifications.

EDO-PAGE-MODE EARLY-WRITE CYCLE



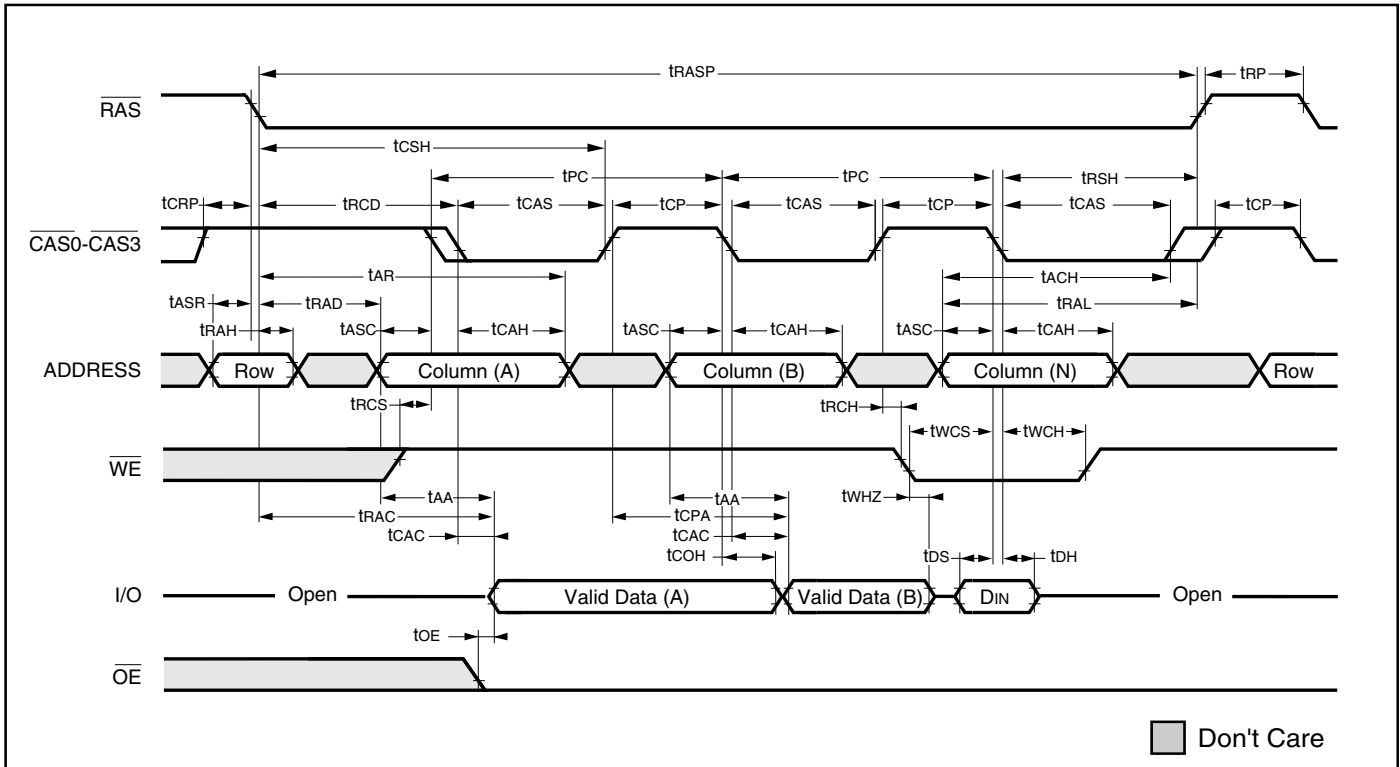
**EDO-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY WRITE Cycles)**



**Note:**

1.  $t_{PC}$  can be measured from falling edge of  $\overline{CAS}$  to falling edge of  $\overline{CAS}$ , or from rising edge of  $\overline{CAS}$  to rising edge of  $\overline{CAS}$ . Both measurements must meet the  $t_{PC}$  specifications.

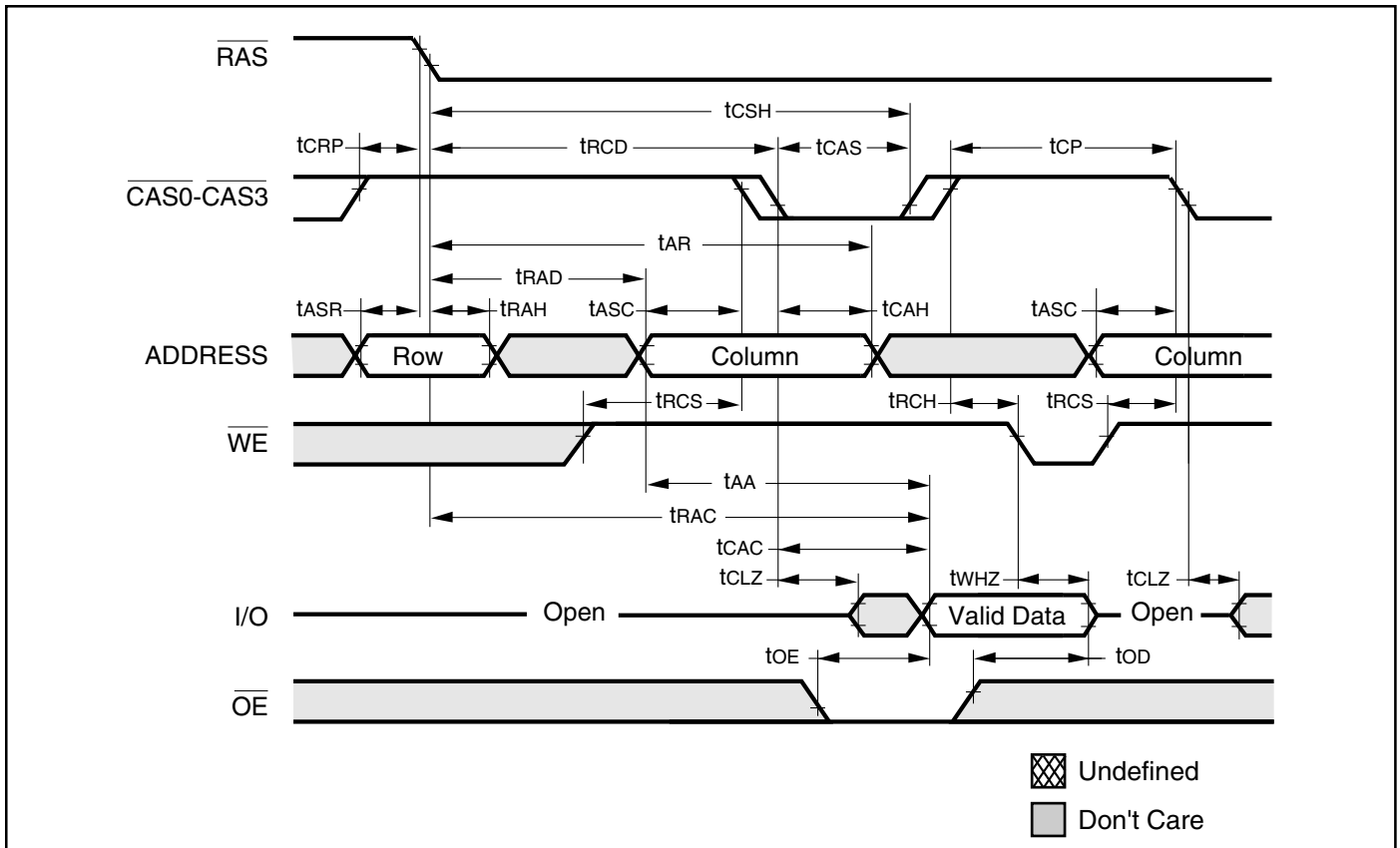
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE (Pseudo READ-MODIFY WRITE)



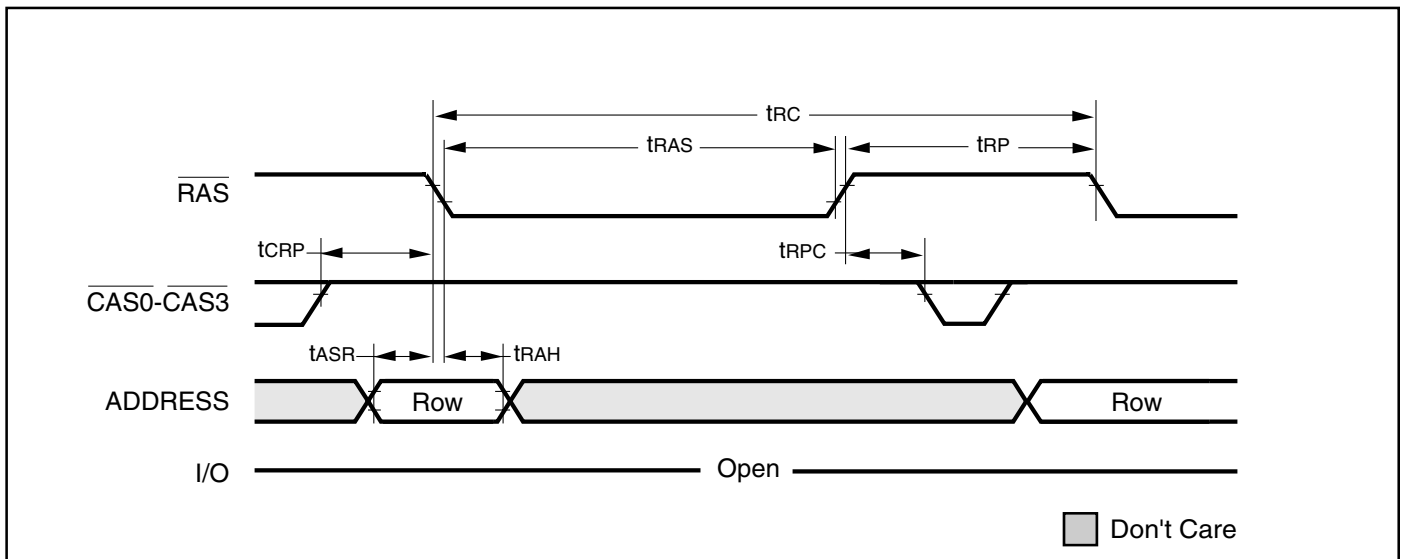


AC WAVEFORMS

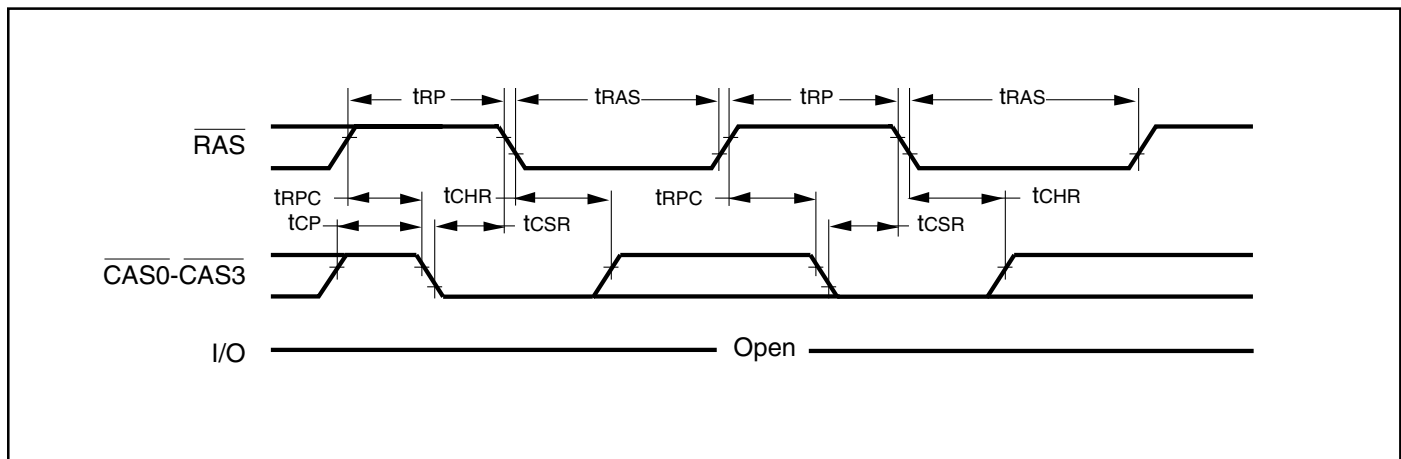
READ CYCLE (With  $\overline{WE}$ -Controlled Disable)



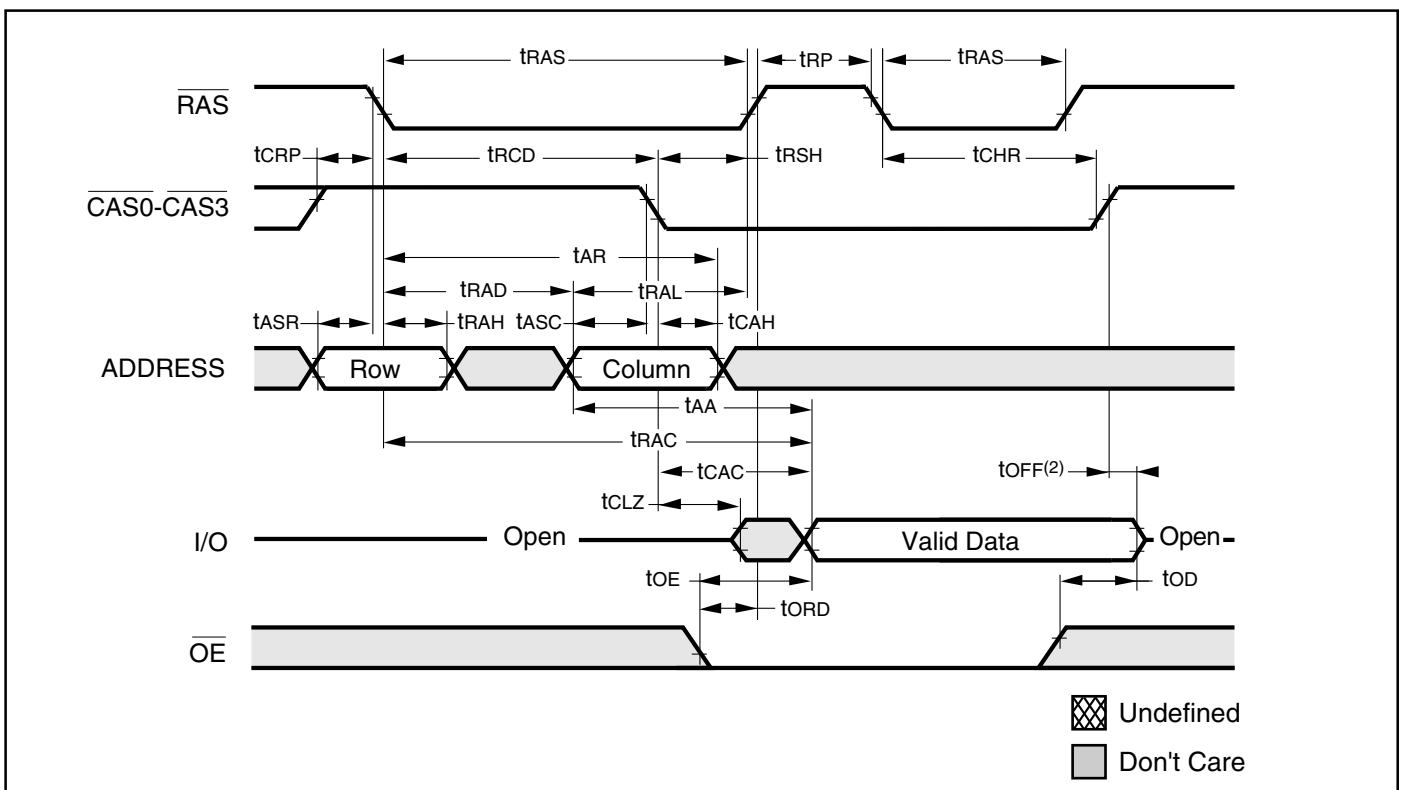
$\overline{RAS}$ -ONLY REFRESH CYCLE ( $\overline{OE}$ ,  $\overline{WE}$  = DON'T CARE)



**CBR REFRESH CYCLE** (Addresses;  $\overline{WE}$ ,  $\overline{OE}$  = DON'T CARE)



**HIDDEN REFRESH CYCLE** ( $\overline{WE}$  = HIGH;  $\overline{OE}$  = LOW)<sup>(1)</sup>



**Notes:**

1. A Hidden Refresh may also be performed after a Write Cycle. In this case,  $\overline{WE}$  = LOW and  $\overline{OE}$  = HIGH.
2.  $t_{off}$  is referenced from rising edge of RAS or CAS, whichever occurs last.

**ORDERING INFORMATION****Commercial Range: 0·C to 70·C**

<b>Speed (ns)</b>	<b>Order Part No.</b>	<b>Package</b>
28	IS41LV32256-28PQ	PQFP
	IS41LV32256-28TQ	TQFP
30	IS41LV32256-30PQ	PQFP
	IS41LV32256-30TQ	TQFP
35	IS41LV32256-35PQ	PQFP
	IS41LV32256-35TQ	TQFP

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