

IRFPS38N60LPbF

HEXFET® Power MOSFET

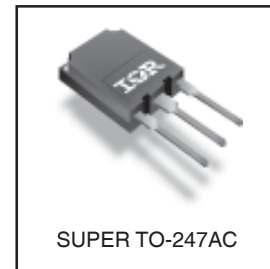
Applications

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control applications
- Lead-Free

V _{DSS}	R _{DS(on) typ.}	T _{rr typ.}	I _D
600V	120mΩ	170ns	38A

Features and Benefits

- SuperFast body diode eliminates the need for external diodes in ZVS applications.
- Lower Gate charge results in simpler drive requirements.
- Enhanced dv/dt capabilities offer improved ruggedness.
- Higher Gate voltage threshold offers improved noise immunity.



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	38	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	24	
I _{DM}	Pulsed Drain Current ①	150	
P _D @ T _C = 25°C	Power Dissipation	540	W
	Linear Derating Factor	4.3	W/°C
V _{GS}	Gate-to-Source Voltage	±30	V
dv/dt	Peak Diode Recovery dv/dt ②	13	V/ns
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	1.1(10)	N•m (lbf•in)

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	38	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	150		
V _{SD}	Diode Forward Voltage	—	—	1.5	V	T _J = 25°C, I _S = 38A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	170	250	ns	T _J = 25°C, I _F = 38A
		—	420	630		T _J = 125°C, di/dt = 100A/μs ④
Q _{rr}	Reverse Recovery Charge	—	830	1240	nC	T _J = 25°C, I _S = 38A, V _{GS} = 0V ④
		—	2600	3900		T _J = 125°C, di/dt = 100A/μs ④
I _{RRM}	Reverse Recovery Current	—	9.1	14	A	T _J = 25°C
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

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International
IR Rectifier

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.41	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	120	150	mΩ	$V_{GS} = 10V, I_D = 23A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	$V_{DS} = 600V, V_{GS} = 0V$
		—	—	2.0	mA	$V_{DS} = 480V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -30V$
R_G	Internal Gate Resistance	—	1.2	—	Ω	$f = 1MHz, \text{open drain}$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	20	—	—	S	$V_{DS} = 50V, I_D = 23A$
Q_g	Total Gate Charge	—	—	320	nC	$I_D = 38A$
Q_{gs}	Gate-to-Source Charge	—	—	85	nC	$V_{DS} = 480V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	160	nC	$V_{GS} = 10V, \text{See Fig. 7 \& 15 } \textcircled{4}$
$t_{d(on)}$	Turn-On Delay Time	—	44	—	ns	$V_{DD} = 300V$
t_r	Rise Time	—	130	—		$I_D = 38A$
$t_{d(off)}$	Turn-Off Delay Time	—	92	—		$R_G = 4.3\Omega$
t_f	Fall Time	—	69	—		$V_{GS} = 10V, \text{See Fig. 11a \& 11b } \textcircled{4}$
C_{iss}	Input Capacitance	—	7990	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	740	—		$V_{DS} = 25V$
C_{riss}	Reverse Transfer Capacitance	—	72	—		$f = 1.0MHz, \text{See Fig. 5}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	350	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 480V \textcircled{5}$
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	260	—		

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	680	mJ
I_{AR}	Avalanche Current ①	—	38	A
E_{AR}	Repetitive Avalanche Energy ①	—	54	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.22	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.91mH$, $R_G = 25\Omega$, $I_{AS} = 38A$, $dv/dt = 13V/ns$. (See Figure 12a)
- ③ $I_{SD} \leq 38A$, $di/dt \leq 630A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$.

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
 $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

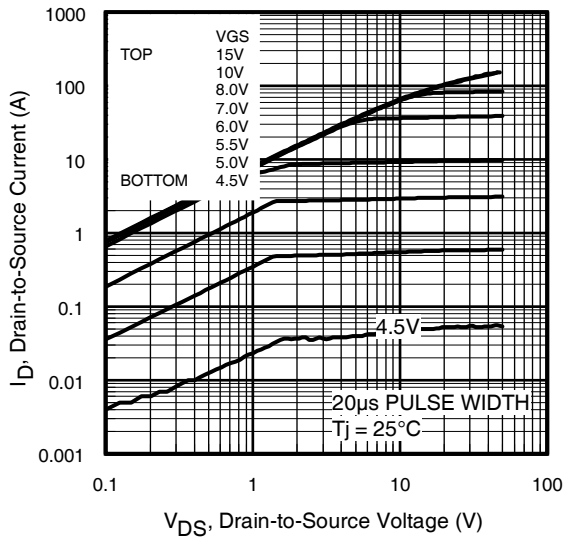


Fig 1. Typical Output Characteristics

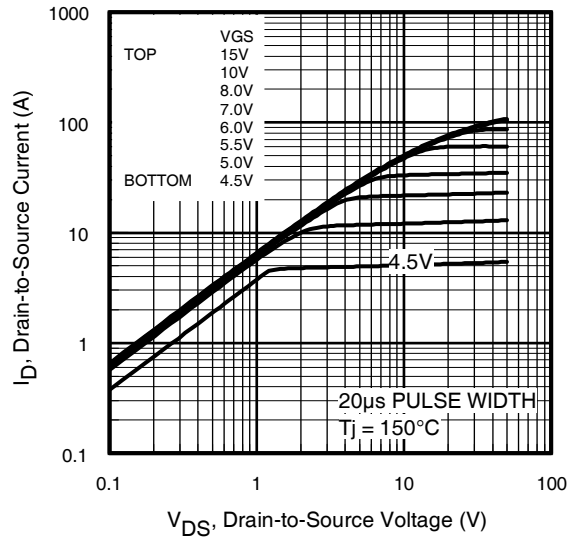


Fig 2. Typical Output Characteristics

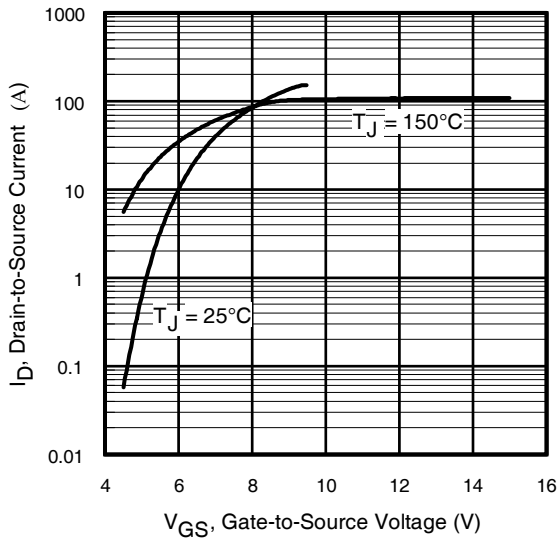


Fig 3. Typical Transfer Characteristics

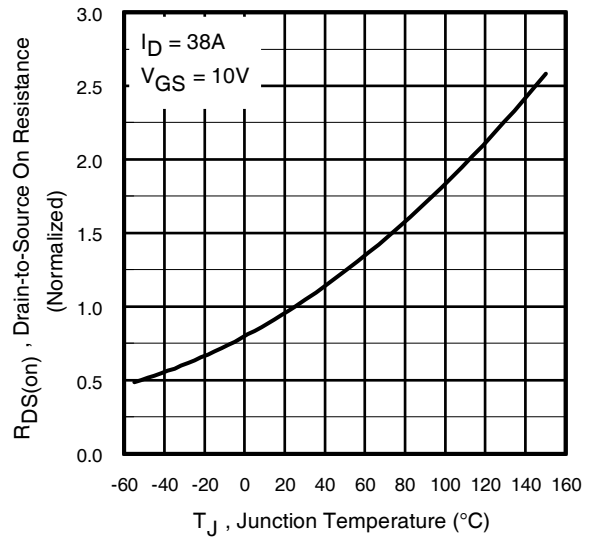


Fig 4. Normalized On-Resistance vs. Temperature

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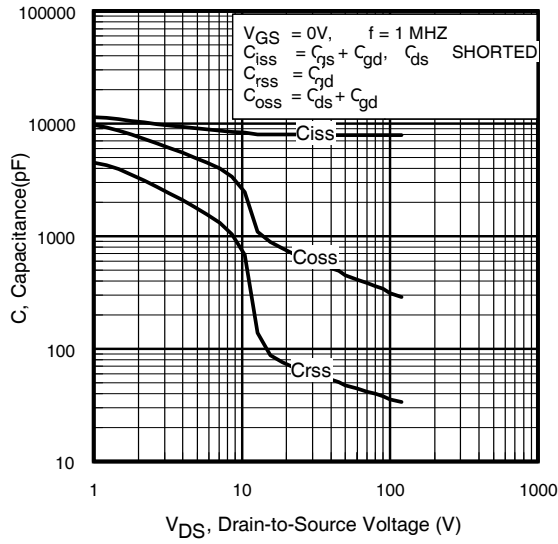


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

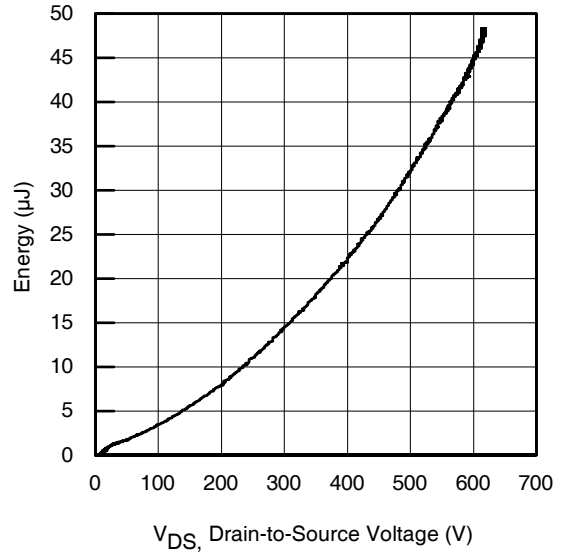


Fig 6. Typ. Output Capacitance Stored Energy vs. V_{DS}

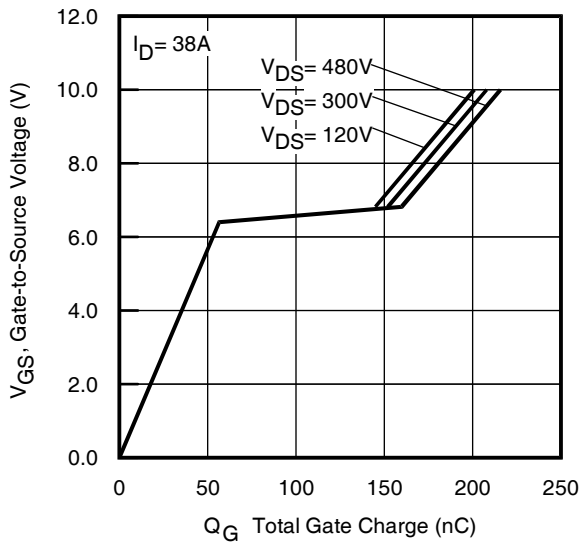


Fig 7. Typical Gate Charge vs. Gate-to-Source Voltage

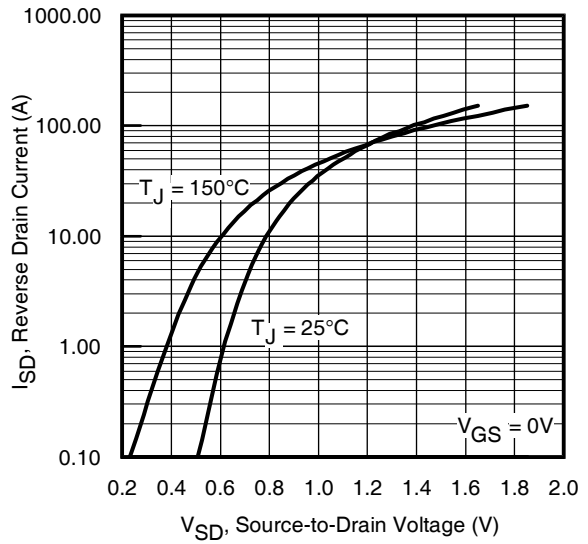


Fig 8. Typical Source-Drain Diode Forward Voltage

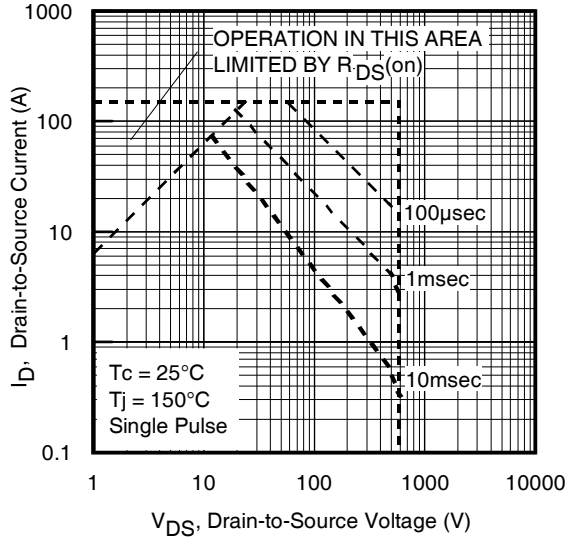


Fig 9. Maximum Safe Operating Area

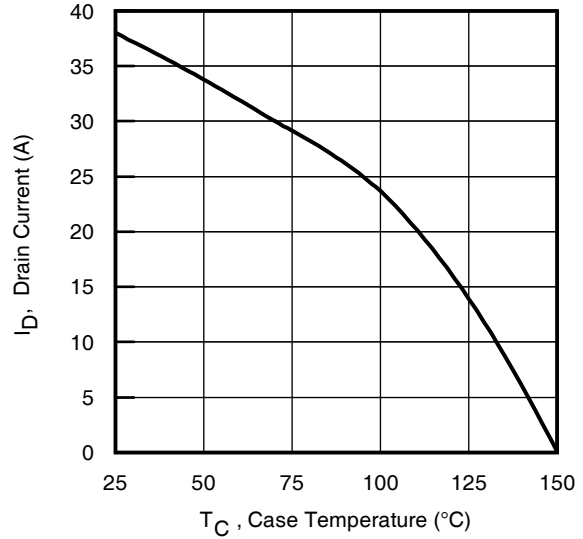


Fig 10. Maximum Drain Current vs. Case Temperature

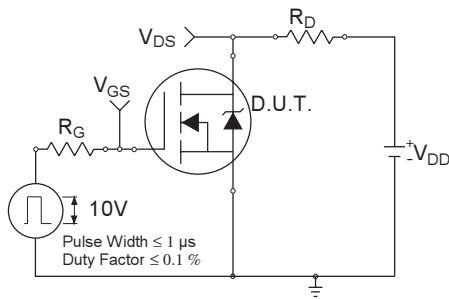


Fig 11a. Switching Time Test Circuit

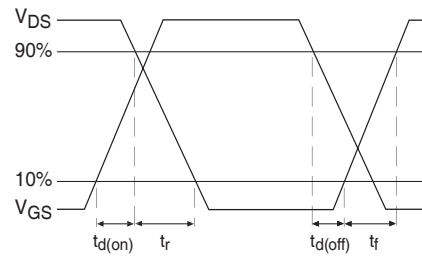


Fig 11b. Switching Time Waveforms

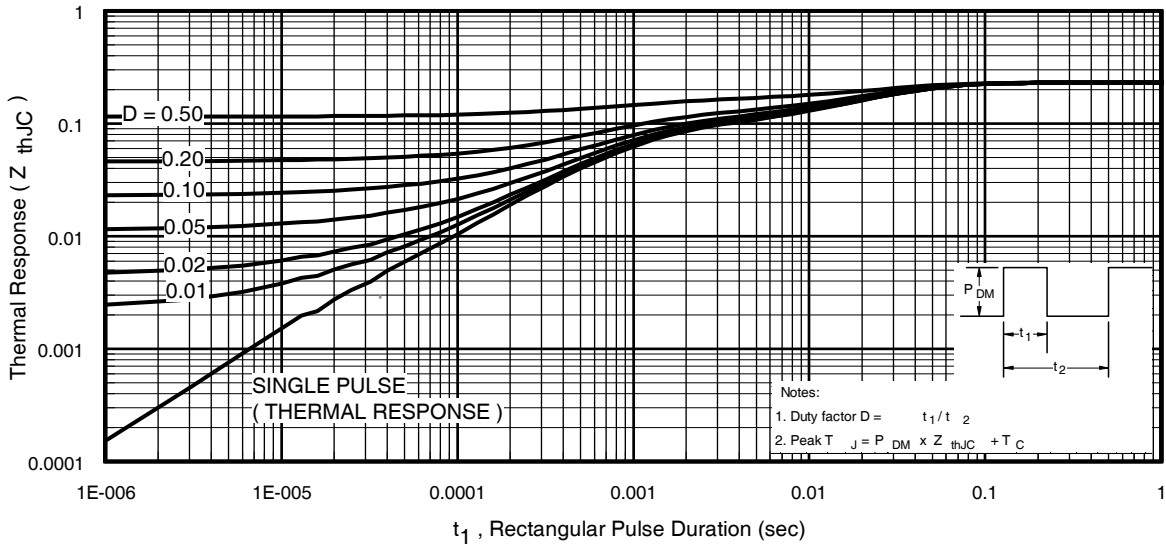


Fig 12. Maximum Effective Transient Thermal Impedance, Junction-to-Case

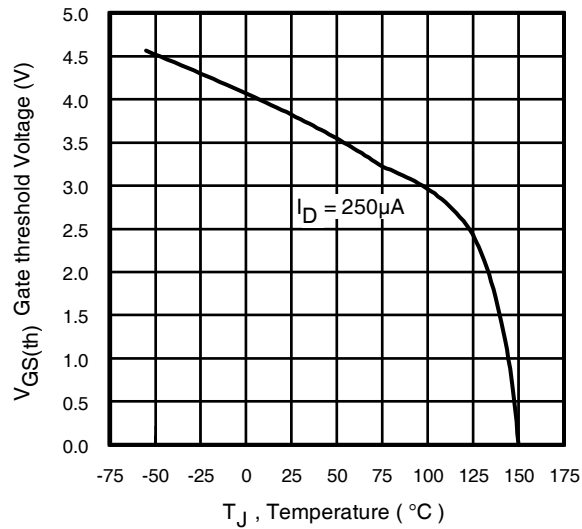


Fig 13. Threshold Voltage vs. Temperature

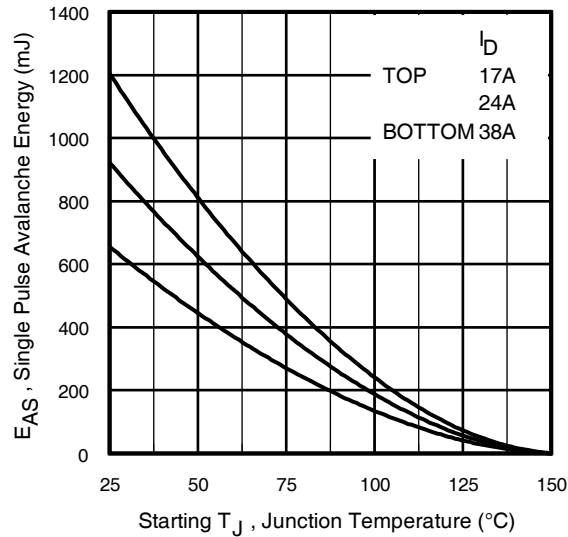


Fig 14a. Maximum Avalanche Energy vs. Drain Current

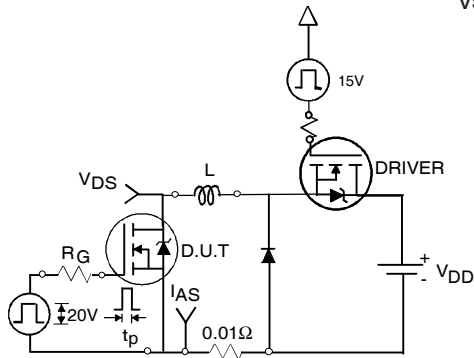


Fig 14b. Unclamped Inductive Test Circuit

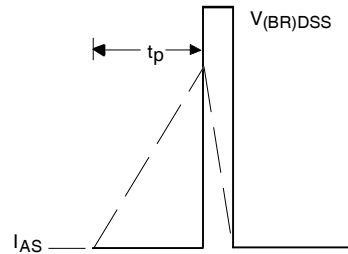


Fig 14c. Unclamped Inductive Waveforms

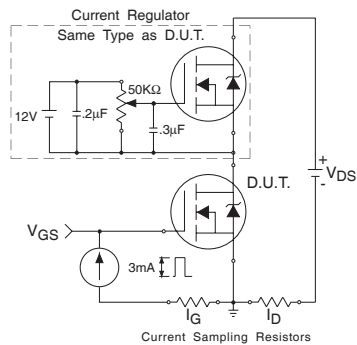


Fig 15a. Gate Charge Test Circuit

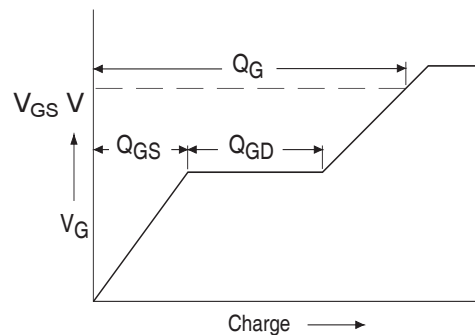
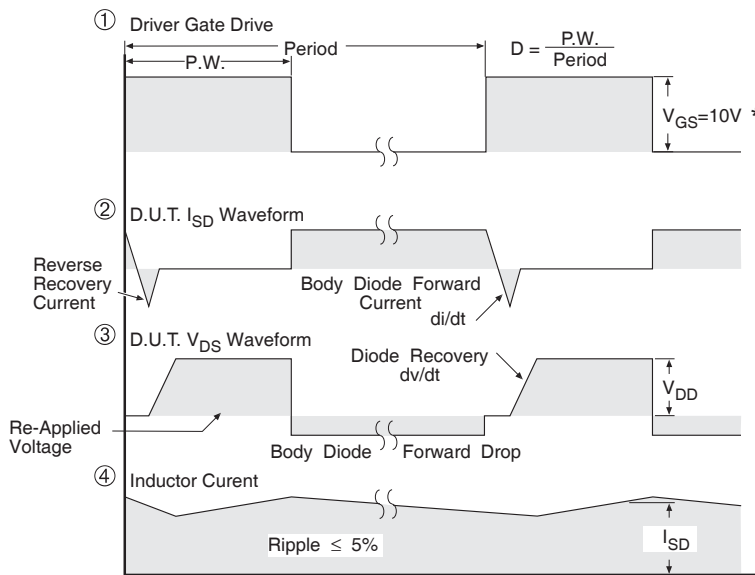
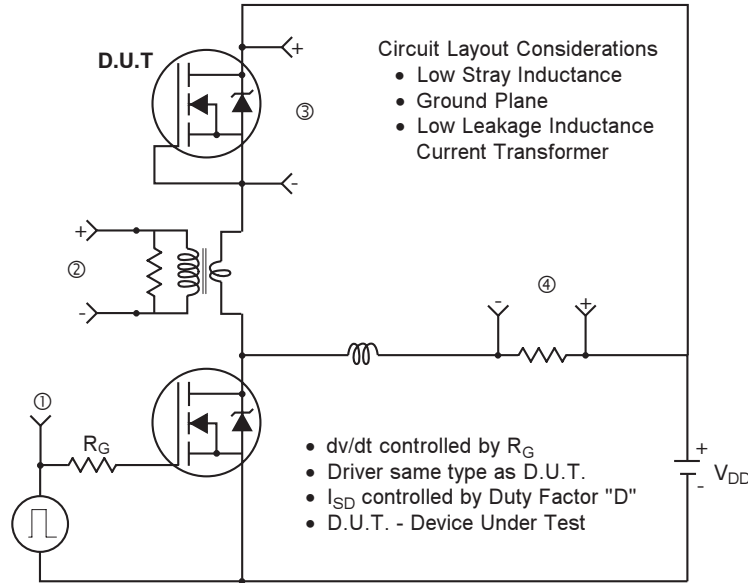


Fig 15b. Basic Gate Charge Waveform

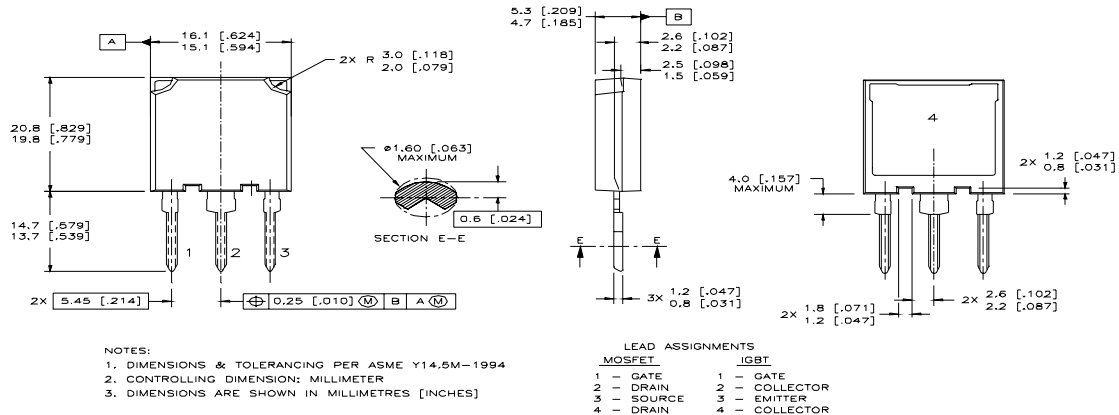
Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

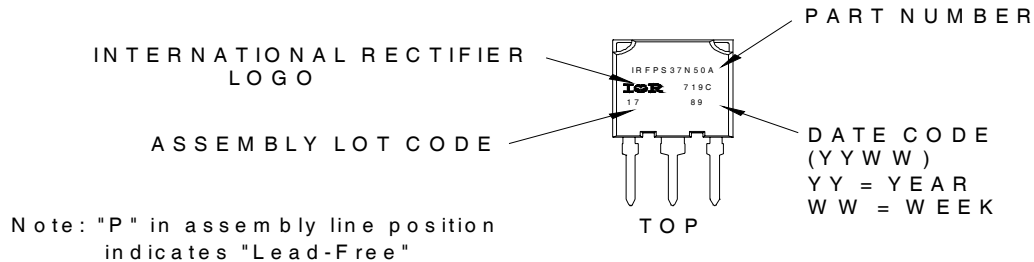
Fig 16. For N-Channel HEXFET® Power MOSFETs

Case Outline and Dimensions — Super-247



Super-247 (TO-274AA) Part Marking Information

EXAMPLE: THIS IS AN IRFPS37N50A WITH
 ASSEMBLY LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



Super TO-247AC package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.