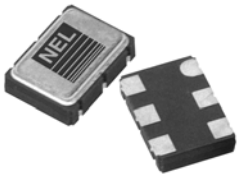
Rev. A



LVDS UHF VCXO
SD-A3DBXXX Series

Description

The **SD-A3DBXXX Series** of voltage controlled crystal oscillators (VCXO) provides ultra high frequency with LVDS complementary outputs. The outputs can be Tri-stated for test automation or combining multiple clocks. The device is based on low noise analog harmonic multiplication for higher frequencies, and packaged in a miniature, low profile leadless ceramic SMD package with 6 gold plated pads.

Applications and Features

- Wide frequency range – 38.0MHz to 640.000MHz
- Fiber Channel; 10 GbE; Infiniband; Network Processors; SOHO Routing
- High Reliability - NEL HALT/HASS qualified for crystal oscillator start-up conditions
- Low Phase Noise, Low Jitter
- High shock resistance, to 1000g
- Ultra High Frequency
- Absolute Pull Range (APR) to ±100 ppm
- Grounded lid and internal by-pass capacitor reduce EMI
- RoHS Compliant, Lead Free Construction

Creating a Part Number

SD - A 3DB X X X - FREQ

Package Code
SD 6 pad 5x7mm SMD

Input Voltage
A 3.3V±5%

Enable Option
H Enable High
L Enable Low

Absolute Pull Range, ppm
E ±20
F ±32
G ±50
H ±100
9 Customer specific

Temperature Range, °C
A 0 to 50
B 0 to 70
C -20 to 70
D -40 to 85
9 Customer specific

NEL FREQUENCY CONTROLS, INC.
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SD-A3DBXXX Series Continued
LVDS UHF VCXO

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Operating Temperature Range	To	-40 to +85	ºC
Storage Temperature Range	Tst	-50 to +90	ºC
Supply Voltage	Vcc	-0.5 to 4.5	V
Enable/Disable Voltage	Ven/dis	0 to Vcc	V

Electrical Parameters

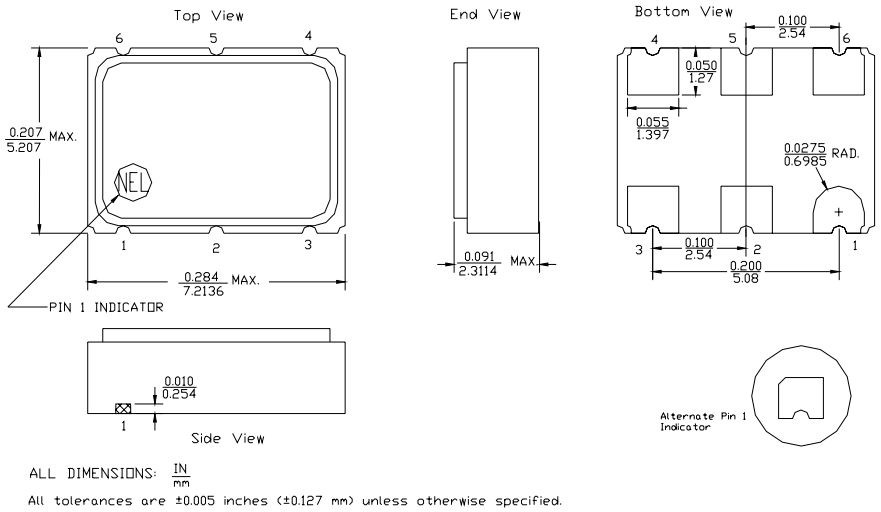
Parameter		Symb	Conditions, Note		MIN	TYP	MAX	Unit
Nominal Frequency		Fo			38		640	MHz
Supply Voltage		Vcc	Code A		3.135	3.3	3.465	V
Supply current		Icc				80	100	mA
Output Logic Type						LVDS		
Load			At receiving end between the outputs		90	100	110	Ohm
Output Levels		Vod	Differential amplitude		247	330	454	mV
			Amplitude error				50	mV
		Vof	Offset Voltage		1.125	1.25	1.375	V
			Offset Voltage error				50	mV
Duty Cycle (Symmetry)			At outputs crossing, room temperature		45/55	50/50	55/45	%
Rise/Fall Time		Tr/Tf	20 to 80, 80 to 20 %			0.5	0.7	ns
Jitter	Integrated	J	Integrated from Phase Noise, 12 KHz to 20 MHz , RMS			0.3		ps
	Wavecrest characterized		Random period,	<320 M >320 M		2.5 2.5		ps
			Accumul., pk-to-pk	<320 M >320 M		30 43		ps
			Deterministic	<320 M >320 M		6 18		ps
Sub-Harmonics				<320 M >320 M		-50 -35		dBc
Phase Noise		£(Δf)	212.5 MHz	@ 10 Hz @100 Hz @1 KHz @10KHz @100KHz @>1MHz		-65 -95 -125 -140 -145 -148		dBc/Hz
Frequency Stability		ΔF/F	Overall, including initial calibration, temperature, aging 10 years, shock and vibration @ Vc=Vcc/2			30		ppm
Control Voltage Range		Vc			0V		Vcc	V
Setability		Vcs	Vc to set F at Fo; T, Vcc, load - nominal, as shipped		0.4 Vcc	0.5 Vcc	0.6 Vcc	V
Absolute Pull Range		APR	Over all conditions, see part # creation		20,32, 50,100			ppm
Input Impedance		Zin	@ Fmod < 100 Khz		10			KOhm
Modulation Bandwidth			At Vc = Vcc/2, -3dB		10			KHz
Enable High Option Pin 2 Enabled Pin 2 Disabled			CMOS logic 1 or N/C CMOS logic 0		0.7 Vcc 0		Vcc 0.3 Vcc	V
Enable Low Option Pin 2 Disabled Pin 2 Enabled			CMOS logic 1 or N/C CMOS logic 0		0.7 Vcc 0		Vcc 0.3 Vcc	V

SD-A3DBXXX Series Continued

LVDS UHF VCXO

Electrical Connection

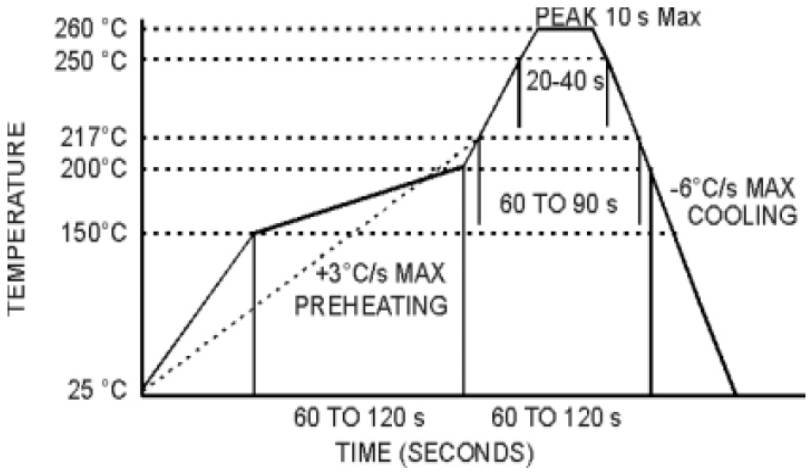
Pin	Connection
1	Vco
2	Enable
3	V_{EE}
4	Output
5	Output Complement
6	V_{CC}



Environmental and Mechanical Characteristics

Operating temp. range	see part # table
Mechanical Shock	Per MIL-STD-202, Method 213, Cond. E
Thermal Shock	Per MIL-STD-883, Method 1011, Cond. A
Vibration	Per MIL-STD-883, Method 2007, Cond. A
Hermetic Seal	Leak rate less than $1x10^{-8}$ atm.cc/s of helium
Soldering conditions	See MAX reflow profile below

Maximum Reflow Profile



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