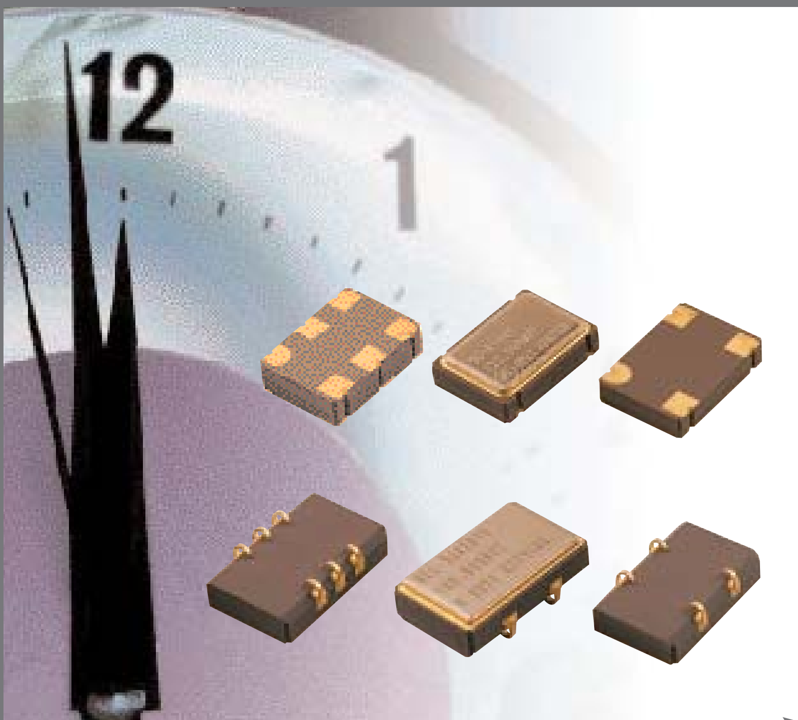
NEL
Frequency Controls, Inc.

4-Gbit Fibre Channel Frequency Control Design Packet



Benefits of choosing NEL

- DPECL Specialization
- High Reliability HALT/HASS Verification
- Full Product Characterization
- Leading Edge Technology: RF, Digital, Module
- Lowest Cost Solution
- Sub-System Module Expertise
- Short Lead Time
- Quick Delivery from our state of the art facility in the US
- ISO 9001:2000 Registered

Contents

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NEL FREQUENCY CONTROLS, INC.
357 Beloit St., P.O. Box 457 • Burlington, WI 53105-0457
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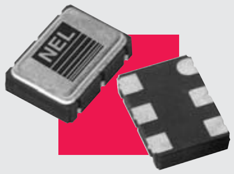
SD-A2980 Series



Size, mm
7.2 x 5.2 x 2.3

I/O
6 pads

Supply Voltage
3.3

Frequency Range
80.0-540.0 MHz

For the most up to date specifications on each NEL product, log on to our website—www.nelfc.com

Differential Positive ECL (DPECL 3.3V)
SD-A2980 Series

Frequency Range: 80.0-540.0 MHz

Description

The SD-A2980 Series of quartz crystal oscillators provide DPECL compatible signals. Systems designers may now specify space-saving, cost-effective packaged PECL oscillators to meet their timing requirements.

Features

- High Reliability - NEL HALT/HASS qualified for crystal oscillator start-up conditions
- Low jitter - Wavecrest jitter characterization available
- Wide frequency range—80.0 MHz to 540.0 MHz
- User specified tolerance available
- Will withstand vapor phase temperatures of 253°C for 4 minutes maximum
- Space-saving alternative to discrete component oscillators
- High shock resistance, to 1000g
- 3.3 Volt operation
- Metal lid electrically connected to ground to reduce EMI
- Overtone technology
- High Q crystal actively tuned oscillator circuit
- No internal PLL avoids cascading PLL problems
- High frequencies due to proprietary design
- Gold plated pads

Creating a Part Number

SD - A298X - FREQ

Package Code
SD 6 pad 7.2x5.2x2.3 mm SMD

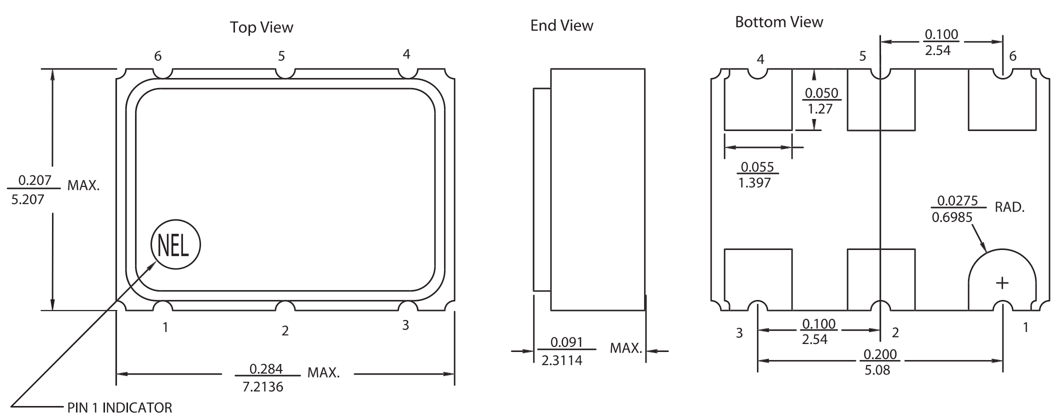
Input Voltage

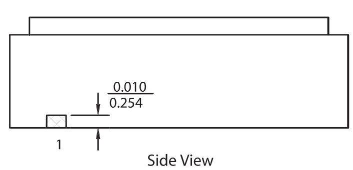
Code	Specification
A	3.3 V
	5 V

Tolerance/Performance

0	±100 ppm 0-70°C
1	±50 ppm 0-70°C
7	±25 ppm 0-70°C
9	Customer Specific
A	±20 ppm 0-70°C
B	±50 ppm -40 to +85°C
C	±100 ppm -40 to +85°C

Drawing Specifications





Electrical Connection

Pin	Connection
1	Enable/Disable
2	N.C.
3	V_{EE} /Ground
4	Output
5	/Output
6	V_{CC}

Dimensions shown in inches and millimeters.

Differential Positive ECL (DPECL 3.3V)
SD-A2980 Series

Frequency Range: 80.0-540.0 MHz

Operating Conditions and Output Characteristics

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max
Frequency	—	—	80.0 MHz	—	540.0 MHz
Duty Cycle	—	@V_{CC} -1.29 V	45/55%	—	55/45%
Logic 0(2)	V_{OL}	—	1.35 V	—	1.70 V
Logic 1(2)	V_{OH}	—	2.28 V	—	2.56 V
Rise & Fall Time	t_r, t_f	20-80% V_O, with 50 ohm load to V_{CC} -2V	—	—	1 nsec
Jitter, RMS(3)	—	—	—	—	3 psec
Enable Voltage(5)	—	with V_{EE} = 0V	2.0 V	—	—
Disable Voltage	—	with V_{EE} = 0V	—	—	0.8 V
Frequency Stability(1)	dF/F	Overall conditions including: voltage, calibration, temp., 10 yr aging, shock, vibration	-100 ppm	—	+100 ppm

General Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max
Supply Voltage	V_{CC}	—	3.15 V	3.3 V	3.45 V
Supply Current	I_{CC}	50 ohm termination to 2.00 V below V_{CC}	0.0 mA	—	80 mA
Output Current	I_O	Low level Output Current	0.0 mA	—	±50.0 mA
Operating Temperature	T_A	—	0ºC	—	70ºC
Storage Temperature	T_S	—	-55ºC	—	125ºC
Power Dissipation	P_D	—	—	—	276 mW
Lead Temperature	T_L	Soldering, 10 sec.	—	—	300ºC
Load	50 ohm to V_{CC} -2V or Thevenin Equivalent, Bias Required				
Start-up Time	t_S	—	—	2 ms	10 ms

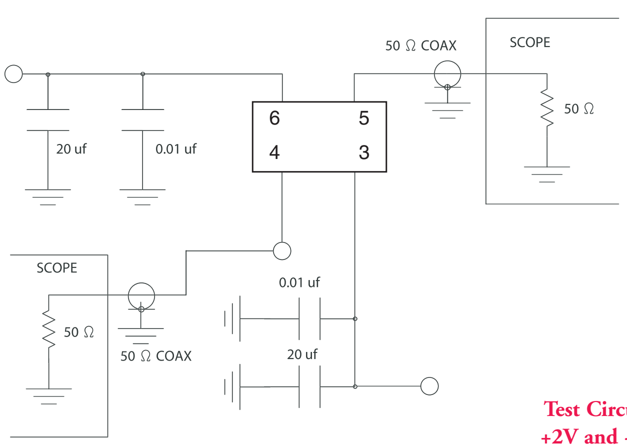
Environmental and Mechanical Characteristics

Mechanical Shock	Per MIL-STD-202, Method 213, Condition E
Thermal Shock	Per MIL-STD-833, Method 1011, Condition A
Vibration	0.060" double amplitude 10 Hz to 55 Hz, 35g's 55 Hz to 2000 Hz
Soldering Condition	300ºC for 10 seconds
Hermetic Seal	Leak rate less than 1 x 10^{-8} atm.cc/sec of helium

Footnotes:

1) Standard frequency stability (±20, ±25, ±50 ppm & others available).
2) V_{OL}, V_{OH}, referenced to ground (V_{EE}) with V_{CC} = 3.3 V.
3) Jitter performance is frequency dependent. Please contact factory for full Wavecrest characterization. RMS jitter bandwidth of 12 kHz to 20 MHz.
5) Open to enable pin also enables the output.

Test Circuit



Test Circuit uses a split supply of +2V and -1.3V for ease of testing.

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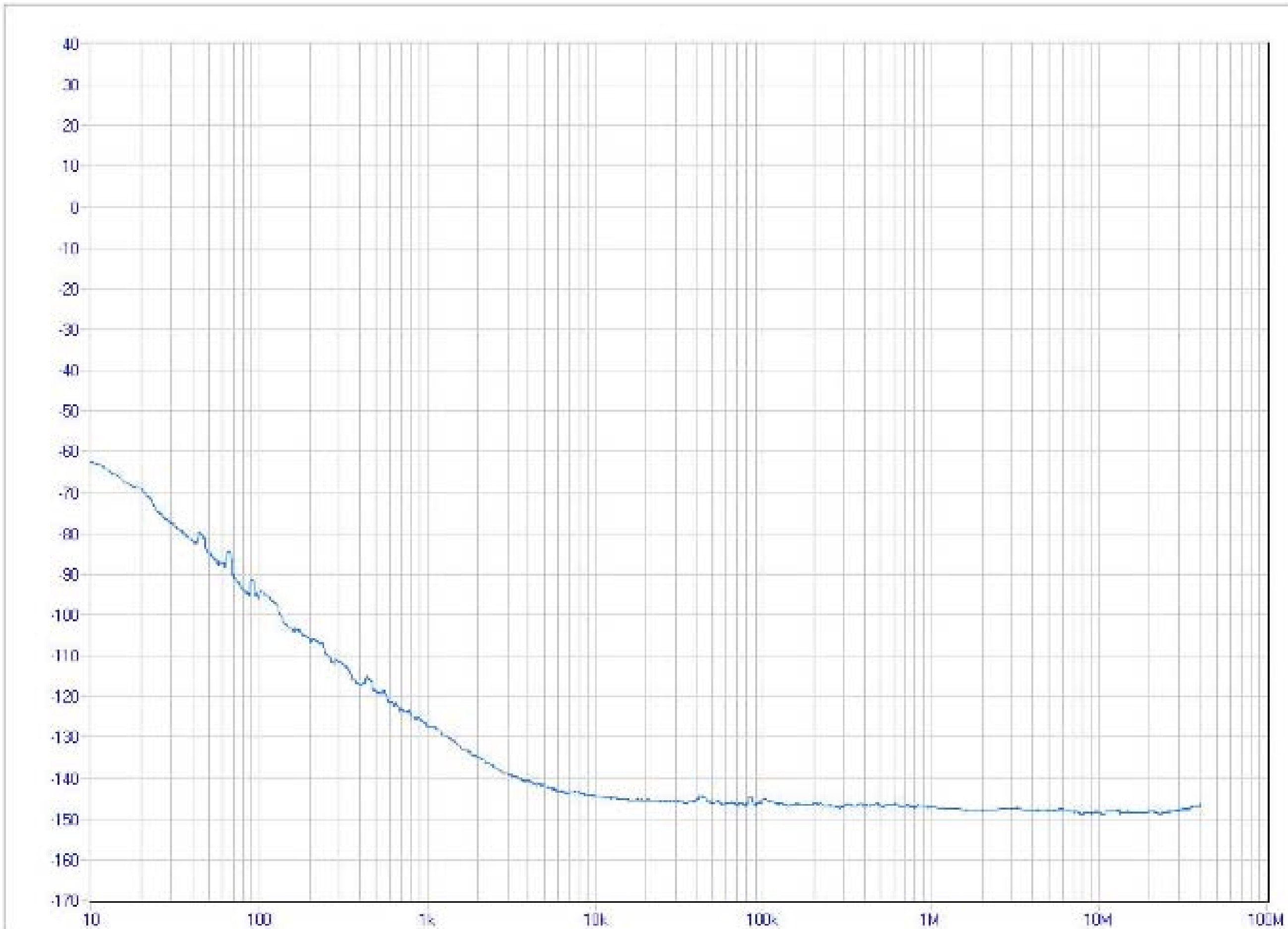
SD-A2980/212.5 MHz Phase Noise



SD-A2980/212.5 MHZ Jitter Data

Visi - [Histogram1]

Tool Edit Action Display View Help

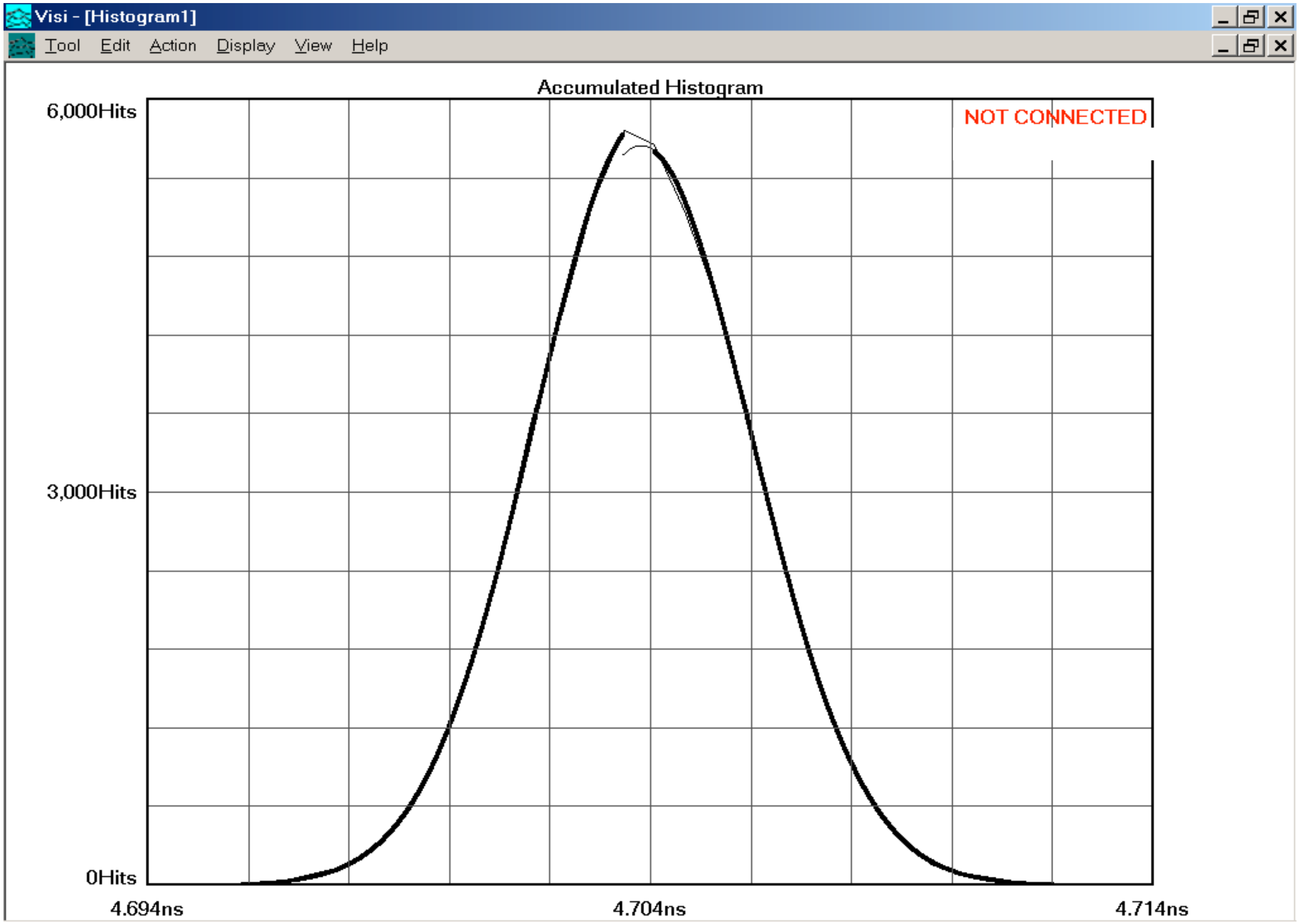
Histogram Summary

	Period	Minimum	Maximum	1-Sigma	Pk-Pk	Hits
Normal	4.70389ns	4.697266ns	4.710083ns	1.997ps	12.817ps	300
Accumulated	4.70372ns	4.695435ns	4.712524ns	2.177ps	17.09ps	51,30

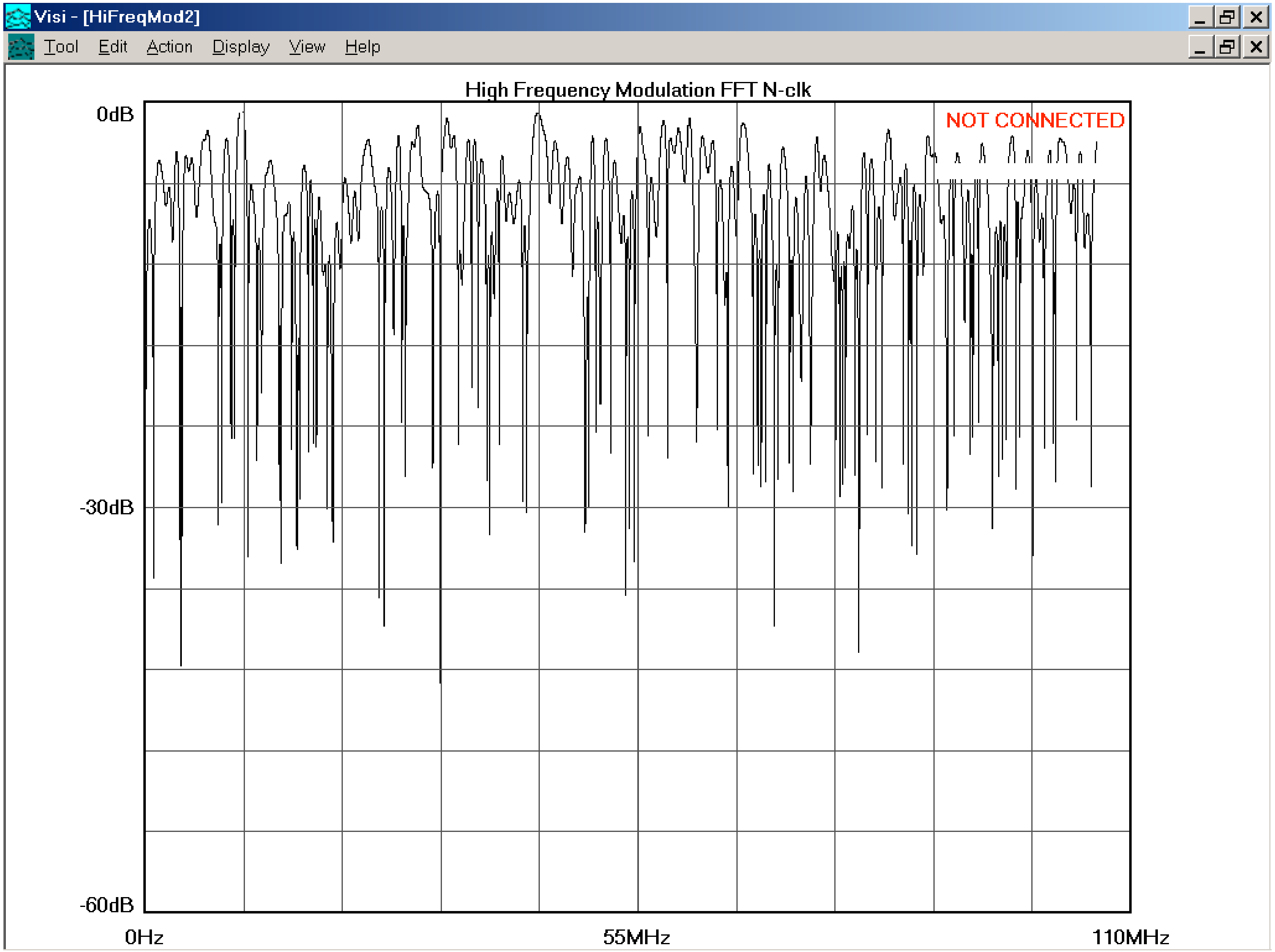
V1:	0.66822V	V2:	0.66822V

Lt-rmsJ	Rt-rmsJ	Avg-rmsJ	DJpk-pk
2.196ps	2.204ps	2.2ps	0s
Goodness-of-fits		#Passes	TJ
2.032196	2.304123	171	30.656ps

SD-A2980/212.5 MHz Jitter Histogram



SD-A2980/212.5 MHz Jitter High Freq. Modulation



Low Jitter, Low Emission Timing Solutions For High Speed Digital Systems

A Design Methodology

NEL
FREQUENCY
CONTROLS, INC.

The Challenges of High Speed Digital Clock Design

Designing clock generation and distribution systems for today's high speed digital electronic devices poses numerous challenges to the design community. At higher speeds, transmission lines and their components behave differently than they do at lower speeds, generating such signal integrity problems as jitter, noise, reflections, and crosstalk if not properly specified and configured. Therefore, when designers approach a project that will have a high speed digital application, they must factor in a variety of signal integrity provisions that are not necessary in lower speed applications.

Key challenges of planning a high speed digital project include:

In high speed applications, the faster the signal moves through the transition region, the less jitter will be produced.

Minimizing timing jitter. It is critical for high speed, high frequency electronics to have low timing jitter. Poor jitter characteristics not only affect data error, but also could cause failures in phase lock loops using this source as a reference. If the source is to be used as a display clock reference, the result will be a blurry display.

As a rule, the faster the signal moves through the transition region, the less system jitter will be produced (see Fig. 1).

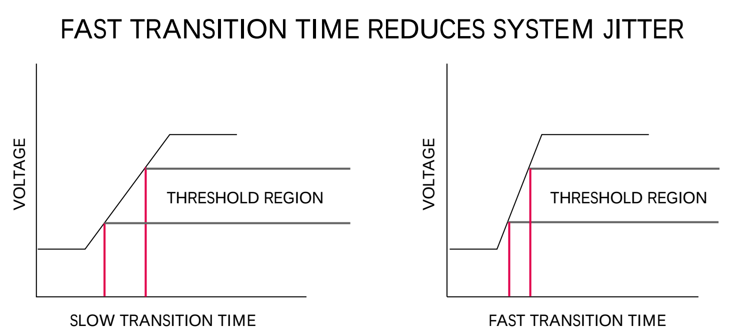


Fig. 1

Reducing emissions. In high speed applications, the likelihood of generating electromagnetic interference (EMI) increases dramatically. FCC regulations regarding EMI noise reduction are becoming more stringent with faster digital speeds. Designers need to address such characteristics as transmission lines, differential signals, signal amplitude, and harmonic content in order to maximize the energy that will be delivered to the load, thus reducing the amount of energy emissions.

Ensuring stability. In general, the higher the specified operating frequency of the electronic system you are designing for, the more critical the clock stability is. Unstable clock performance can cause an increased bit error rate, erroneous data, or missed data in digital systems, whether they are local or wide area systems.

Transmission line impedance matching. The impedance and length of the entire transmission line must be measured and matched with each termination. If impedance matching is overlooked, emissions, crosstalk, and reflections can occur.

Power supply considerations. The prime consideration here is to make sure that the clock is noise-free. Low power supply consumption requirements are also increasing with today's higher speed systems.

An Effective Methodology

The key to achieving optimum system performance in a high speed application starts with an effective design methodology for clock generation and distribution. Put simply, the designer should adopt a methodology that addresses the various clock generation and distribution components as a *complete solution*, not as individual parts. Careful attention to the selection of the appropriate components and circuit distribution method should be given at the outset of the project, keeping in mind the interrelation of the components to one another. Further, it is important to consider the characteristic impedance of all active and passive components at the frequency of operation as the design progresses.

Proper selection of the following clock generation and distribution components is essential (see Fig. 2):

1. The crystal oscillator and its output logic

2. The clock driver, which in some cases will contain enable functions

3. Translators to CMOS at 5V or 3V supply

4. The transmission line (twisted pair, coax, PCB traces)

This white paper is intended to help you make informed decisions about these clock generation and distribution components as you approach your next high speed digital system design.

Clock Generation and Distribution Component Considerations

1 Crystal Oscillator and Logic Selection

Selecting the appropriate crystal oscillator is of the utmost importance in a high speed application, since it will provide the clock reference for the entire clock distribution system.

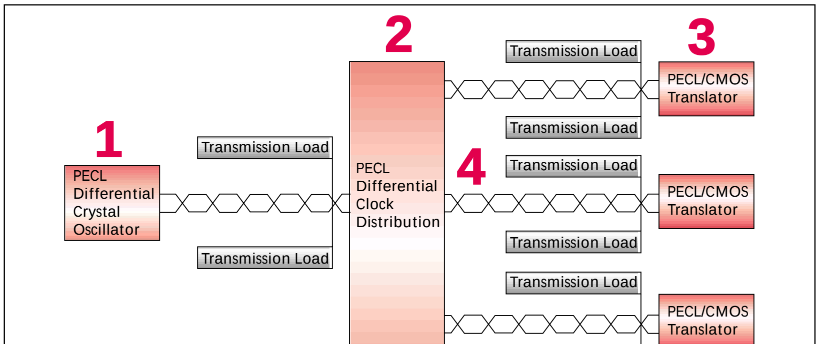


Fig. 2

An effective methodology for achieving optimum system performance addresses the various clock generation and distribution components as a complete solution. Careful selection of the appropriate components should take place at the outset of the project, keeping in mind the components' interrelation to one another.

Stringent crystal oscillator applications typically require a frequency stability of ±20 ppm, fast rise and fall times of less than 600 picoseconds, low characteristic jitter, and a Positive Emitter Coupled Logic (PECL) differential output. The frequency stability will provide a reliable system reference, while fast rise and fall times of the waveform will result in low system jitter. (Although saturating the transition with fast rise and fall times can introduce unwanted noise, this noise will be cancelled out by the use of differential signals.)

Logic Selection: PECL Advantages

Using a PECL logic output provides critical advantages over CMOS logic output technology in high speed applications. Unlike CMOS technology, PECL technology features a differential output, which is essential for reducing emissions. Yet, like CMOS, PECL obtains its operating power from a positive power supply (rather than the negative power supply voltage that powers ECL logic technology), enabling the necessary compatibility with CMOS logic interfaces at the load points.

In addition, PECL technology allows voltage compensation for further rejection of noise on the positive voltage supply. All modern PECL devices contain on-chip bandgap regulators that provide voltage compensation for noise margins with variations in the supply voltage, as well as in junction and ambient temperatures. Because PECL circuits consist of supply-regulated current sources which are switched via steering logic to load resistors, the designer benefits in two ways:

1) the supply current remains unchanged with operating frequency

2) AC performance remains unchanged with voltage, temperature, and frequency

Residual sensitivities of less than 1mV/V for levels, threshold and noise margins with respect to supply voltage may be achieved.

For junction temperatures, residual sensitivities of less than 0.1mV/C are achieved for the same parameters.

Crystal Oscillator Quality

In addition to ensuring low jitter in the waveform, designers should be sure that jitter is minimized in the oscillator itself. This is achieved by selecting an oscillator containing a very high Q crystal. Further, the crystal should be tuned to the oscillator circuit for optimization by the oscillator manufacturer. Use of a PLL synthesizer in the oscillator design should be avoided, since jitter is created by the noise in the phase lock loop.

Other Oscillator Considerations

In PECL systems, all oscillator circuits should have the power supply well decoupled at the oscillator. PECL devices need to have this addressed aggressively, since PECL is referenced only to the most positive side of the power supply. Thus, for PECL the Vcc needs to be as noise-free as possible. Because oscillator characteristics do change with load impedance and load bias voltage, it is important to specify the actual load being used and communicate this to the oscillator vendor.

The chosen oscillator should have a tight symmetry of at least 45% minimum and 55% maximum, and should produce repeatable waveforms to ensure signal consistency. A ground plane should be used (see "Design Subtleties" section).

2 Clock Driver/Distribution Considerations

The clock driver should be a PECL differential device—with differential inputs to receive the oscillator signals, and differential outputs to distribute the signals on the PCB. If clock gating is desired, there should be an Enable pin, probably single ended.

Another aspect of clock driving should be structural symmetry of the device, which will reflect in better overall signal integrity.

Regeneration buffering may be required when trace length and / or attenuation demand it. It is important to structure regeneration such that received signals have settled out and are not still on their rising or falling edge. Otherwise further attenuation may be generated rather than signal buffering.

3 Translator Requirements

If CMOS is to be driven, PECL-to-CMOS conversions will be needed. A dedicated translator should be used for each application-specific point. It is important to locate each translator as close to the load point as possible in order to maintain good signal integrity.

4 Transmission Line Considerations

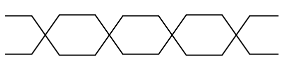
For any high speed and high frequency clock distribution system, properly configured and terminated transmission lines are a requirement. Following are some of the basic characteristics required for a good transmission line.

- The source, transmission line, and load impedances need to match as closely as possible to minimize losses in the transmission line.
- The transmission line should be free of discontinuities which can cause poor performance.
- The transmission line should not have stubs or branches which can result in poor performance.
- The load must be at the opposite end of the transmission line from the source.
- The source must be capable of driving the transmission line impedance.

Differential Schemes

A differential transmission scheme should be adopted which makes use of the differential nature of both the output of PECL drivers and the input of PECL receivers.

The differentially transmitted signals will have a very large common mode rejection range (to capacitively and inductively coupled noise signals) and will be insensitive to supply voltage and temperature variations. The resulting transmission system will be quite immune to external noise sources, and will therefore minimize emissions.



The differential output provided by PECL technology rejects common mode noise in the transmission line, thereby minimizing emissions.

Termination and Layout

Proper terminations are necessary to maximize power transfer while preventing signal reflections (bouncebacks) and noise.

Termination methods cause an undue amount of confusion. The following tips can help avoid confusion and will help meet the requirements of complex digital systems.

1. Print the highest impedance level line that can be manufactured on the PCB with reasonable repeatability. Usually this will be 100 ohms, and it will reduce the power demand for termination, if compared to a 50 ohm scheme, by a factor of two.
2. If group delay is a concern, run the two traces on the top of the PCB, or within the PCB (propagation delay is a function of dielectric constant).
3. The width between each output trace should be five times the width of each trace, in order to minimize crosstalk. Route the traces directly to the various tap points—stubs should be avoided, since they generate noise. If the tap point is a translator to CMOS, place it as close as is practical to the CMOS logic to be driven.
4. Each termination should be built as a source-terminated input to the transmission line or the destination-termination should be structured as the Thevenin equivalent of the characteristic line impedance (50-100 ohms). Either method requires two resistors as a termination but eliminates the need for termination supply voltage (and its distribution plane).
5. At 3.3V, the termination may be a single 100 ohm resistor to ground, if 100 ohms lines are used.

Resistor Considerations

A distinction should be made between pull-down resistors, which simply provide a load current for the open emitter follower, and termination resistors.

For very short connections of low parasitic capacitance, 2 kohms to GND may be practical. If, however, a longer distance must be bridged by the interconnect, this interconnect will have to be terminated by its characteristic impedance in order to maximize power transfer and minimize reflections. The characteristic impedance of such interconnects generally lies between 40 and 120 ohms.

Given this range and the output drive capability of the emitter followers, the termination resistor can also serve the purpose of the pull-down resistor, but in several termination schemes, they are indeed kept as separate components.

The Benefits of PECL Technology

PECL differential logic output technology provides many advantages over more traditional logic systems, such as CMOS devices, in high speed systems.

Compared to CMOS, PECL offers the following benefits:

- Lower system jitter is produced by the lower slew rate of PECL. This technology has a smaller characteristic transition region compared to CMOS. PECL produces fast rise and fall times, which are important for accurate clocking. Since capacitively coupled noise currents are I=C dV/dt, CMOS (2V/ns) will produce six times the noise of PECL (0.34V/ns) if compared single ended. If PECL is used differentially, the advantage is even greater.
- PECL technology eliminates common mode noise (emissions) by offering differential inputs and outputs, not available in CMOS.
- Unlike CMOS, PECL further minimizes noise by using an emitter follower output stage which does not generate a large current spike when switching states. The power source and ground stay relatively noise free.
- PECL output devices deliver greater stability and reduced skew between outputs because they inherently have very little difference between T_{PLH} and T_{PHL} delays. (Clock driver signals need to be output simultaneously; delays produce skew and cause signal integrity problems).
- PECL technology is a better choice for driving transmission lines, due to its low impedance outputs (typically around 6 to 25 ohms) and high impedance inputs (typically 75 kohms). Its low impedance outputs are structured as open emitter followers, allowing for the maximum flexibility to terminate the interconnecting scheme (coax, twisted pair, PCB traces) appropriately to minimize reflections.
- PECL can drive 50 ohm transmission lines directly.
- PECL offers low power supply consumption at high frequencies (see Fig. 3). The power consumption stays constant with frequency. By contrast, CMOS power consumption starts low at low frequencies, but steadily rises as the frequency rises. CMOS power consumption is equal to PECL power consumption at 65 MHz, after which it continues to rise sharply.

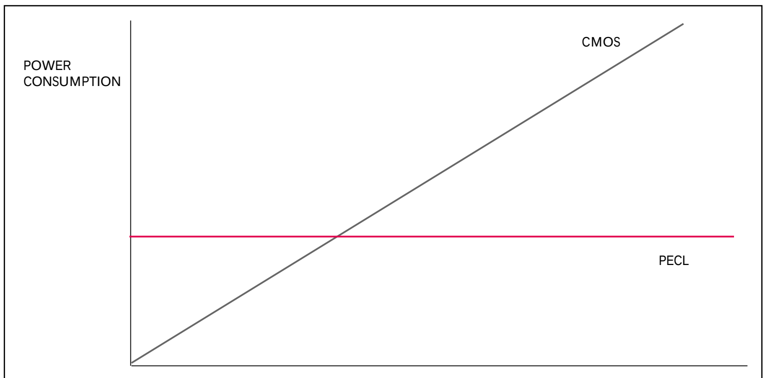


Fig. 3

PECL technology offers lower power consumption at higher frequencies, compared to CMOS technology.

Design Subtleties

Besides clock generation and distribution component considerations, there are other design subtleties to consider.

Ground plane. The most important statement that may not be intuitively obvious to the PCB or system designer when moving up to higher frequencies is the absolute requirement for a ground plane.

The ground plane is an integral part of a transmission line and cannot be omitted. It serves as the only absolute for all levels, including threshold and noise margins (excluding the power supply). It is required for shielding between critical sub-circuits and to the outside world.

The term ground plane may well refer to an AC ground, such as that represented by the +5V supply bus. The +5V plane may be the only solid plane on the PCB. That is acceptable as long as there is one which can serve the purpose described.

Circulating currents are generated even if fully differential signals are used. The loops swept by these circulating (output) currents must be minimized and voltage drops due to such currents must be taken care of by decoupling capacitors; usually one 0.1µF per IC, placed in close proximity.

Balance and symmetry. Balance and symmetry should be maintained for the clocking net and other time-sensitive data nets. Differential lines must be of equal length, contain equal loads and have similar surroundings.

Emissions and crosstalk. Emissions and crosstalk can be attributed to two major causes: voltage and current transients.

Voltage transitions, which are not locally compensated by an equal transition in the reverse direction, will capacitively couple a noise current of the magnitude C x dV/dt.

Current transients, which are not locally compensated by an equal transition in the reverse direction, will inductively couple a noise voltage of the magnitude L x dI/dt.

Simultaneous switching of address buses, for instance, can generate sufficient crosstalk into ill designed clocking systems to cause runt clock pulses which are extremely difficult to analyze, locate and eliminate.

Conclusion

The latest generation of high speed digital systems demand better signal integrity. By using the techniques covered in this design methodology, designers will greatly reduce system jitter, emissions, noise generation, and crosstalk. The primary steps to success are to utilize a PECL differential output logic clock oscillator that provides fast signal transitions; a PECL differential clock driver; dedicated PECL-to-CMOS translators for each load point; and impedance matched and properly terminated transmission lines.

To support this methodology, it is helpful to choose component manufacturers who will work with you, and with one another, in the shared goal of providing a complete solution. The result will be faster time-to-market, better product quality, and improved ability to pass EMI testing requirements.

About the Authors

This White Paper was coauthored by NEL Frequency Controls, Inc. and Arizona Microtek Inc. to assist designers in clock generation and distribution projects for high speed digital system applications.

NEL Frequency Controls, Inc., established in 1954, is a crystal oscillator manufacturer specializing in PECL Differential Clock Oscillators for use in high speed digital design applications. NEL is committed to helping its customers develop effective clock generation and distribution designs by collaborating with other supply chain partners to deliver complete solutions. Many of NEL's products are used in computer, data communication, and instrumentation applications where low jitter and low emissions are critical requirements. For additional information on frequency management technologies and methods, or to discuss a specific oscillator application, contact NEL Frequency Controls, Inc. at (414) 763-3591, fax (414) 763-2881, email sales@nelfc.com, or visit our web site at www.nelfc.com.

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References used: *High-Speed Digital Design*, by Dr. Howard Johnson; Motorola Application Note AN1406 – *Designing With PECL*; Motorola Application Note AN1405 – *ECL Clock Distribution Techniques.*